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TEXAS INSTRUMENTS

BEST OF...

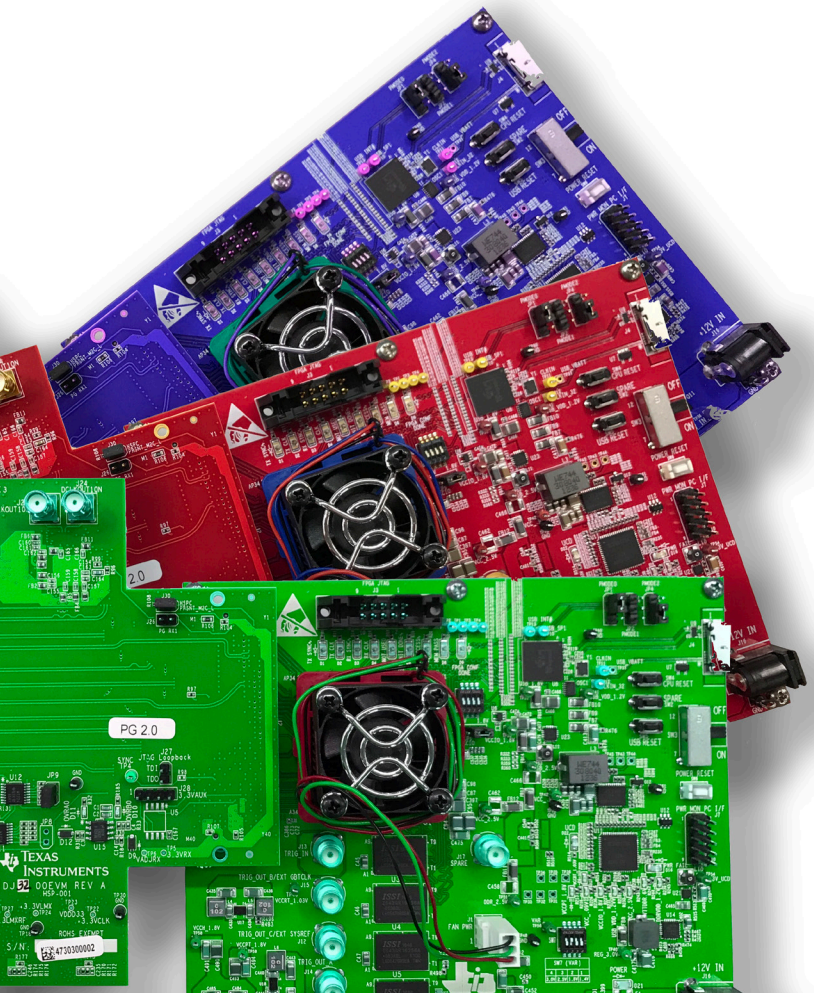
DATA CONVERTERS

BEST OF...
DATA CONVERTERS

INTRODUCTION

ANALOG-TO-DIGITAL CONVERTERS (ADCs), which convert analog signals to a digital representation for processing, are practically ubiquitous in the world of design engineering. Every engineer at some point or another will run into them, whether working on a low power design or a high-performance application. But given the fact that there is a growing number of options and ADC architectures available, that the performance of an ADC depends on the overall system design, and the ever-increasing demands on performance, designing with data converters requires a nuanced approach. This E-book is intended to as a rich resource to help engineers learn about the latest advances in the technology, gain a deeper understanding of how to select apply ADCs in their designs, and ultimately create better designs that rely on ADCs for their performance.

Karen Auguston Field,
Content Director



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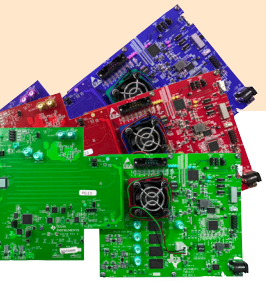

LOU FRENZEL, Contributing Editor

CHAPTER 1:

Learn ADC Design Now

If you're an electronics engineer, ADCs likely reside in your present designs, or will in the future. The time is as good as any to broaden your knowledge of them.

Practically every electronic product today contains one or more analog-to-digital converters (ADCs). As an engineer, you have no doubt already encountered the ADC in a design project. If not, then you will eventually.

ADCs are tricky—they have some design quirks that must be addressed in order to achieve design success. Where do you learn the fine points of ADC design? Many get it from experience. Others are lucky to learn from a colleague or mentor. Textbooks can be a big help with the basic theory, but sources of the real-world application particulars are harder to come by.

Not any longer. Texas Instruments offers some attractive learning alternatives about ADCs. And these are things that you definitely didn't learn in college.

TI PRECISION LABS

The TI Precision Labs offers an on-demand ADC curriculum that pairs theory and applied lab exercises to deepen the technical expertise of experienced engineers and accelerate the development of those early in their career. The ADC curriculum consists of a mix of videos, multiple-choice quizzes, and short answer exercises. The main topics are:

1. *Introduction to Analog to Digital Converters.* Covers dc and ac specifications and input types.
2. *ADC Drive Topologies.* Gets into how to determine the linear range of an ADC and front-end driver design with differential and instrument amplifiers.
3. *Error and Noise.* Covers statistical analysis of errors and determining the total noise.
4. *AC Specifications.* Addresses frequency-domain-related topics, fast Fourier transform (FFT), sampling and filtering for signal-to-noise ration (SNR) and total harmonic distortion (THD), and anti-aliasing filters.
5. *SAR ADC Input Driver Design.* Front-end design is the emphasis, including driver amplifier and component selection.
6. *Low-Power SAR ADC System Design.* Covers power scaling.

Since ADC design also typically involves related op-amp use and selection, you may be interested in learning more about that. TI Precision Labs offers a training series on op-amp design.

THE ANALOG ENGINEER'S CALCULATOR

The Analog Engineer's Calculator is a PC-based tool designed to speed up many of the repetitive calculations used regularly by analog-circuit design engineers. This software provides a graphical interface with a list of various common calculations covering a wide range of design needs. The tool covers both ADCs and digital-to-analog converters (DACs). Some of the features include noise calculations, gain selection, filter configurations, printed-circuit-board (PCB) parasitic calculations, and passive component selection.

In addition to being useful as a standalone tool, this calculator pairs well with the concepts described in the Analog Engineer's Pocket Reference.

CHOOSING THE BEST ADC ARCHITECTURE FOR YOUR APPLICATION

If you're at that design stage where you need to choose an ADC architecture, the available TI training materials can provide assistance. The company's four-part video training series will help you choose the best ADC architecture for your application. It focuses on the differences between the architectures of successive-approximation-register (SAR) types of ADCs, including delta-sigma ADCs.

Part 1 is an overview of the many different ADC architectures and highlights the advantages of each. Part 2 gets into the details of SAR-type ADCs. Parts 3 and 4 zero in on the delta-sigma ADC, explaining how this unusual converter works and its need for a digital filter. This is a quick way to get up to speed on ADC usage. It's definitely worth the time investment.

Keeping up-to-date is a priority for engineers in these fast-changing times. Why not take advantage of resources like these to fine-tune and expand your ADC knowledge, so that you can apply it now as well as down the road?

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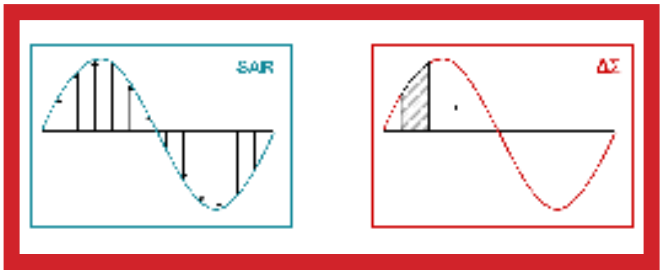
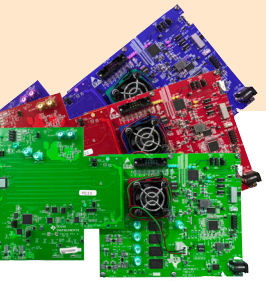
SAR converters (left) sample quickly to capture an instant in time, while delta-sigma converters (right) average many samples to improve system resolution.

☞ *Learn More!*





PAUL PICKERING, Contributing Editor

CHAPTER 2:

Do More with Less: Designing With Power-Efficient Data Converters

Efforts to get more "green" have led to several effective power-reducing techniques for data-acquisition designs, and they all start with a power-efficient data converter.

No matter your target application, it's desirable to make the design as "green" as possible in today's world. That means meeting the required performance goals with the minimum power consumption.

In data-acquisition design, an analog-to-digital converter (ADC) is available for just about every application. However, there can be considerable overlap, and high performance, low power consumption, and small size are often conflicting goals.

For example, higher-performance converter architectures tend to require more silicon and consume more power, which leads to larger packages. Prioritizing low power consumption and small size may require compromising the performance, perhaps reducing the resolution or sample rate.

The power consumption of the data-acquisition signal chain also depends heavily on two additional factors: the power dissipated by the input driver and the efficiency of the power supply. This can be challenging for systems that require a combination of high performance and low power.

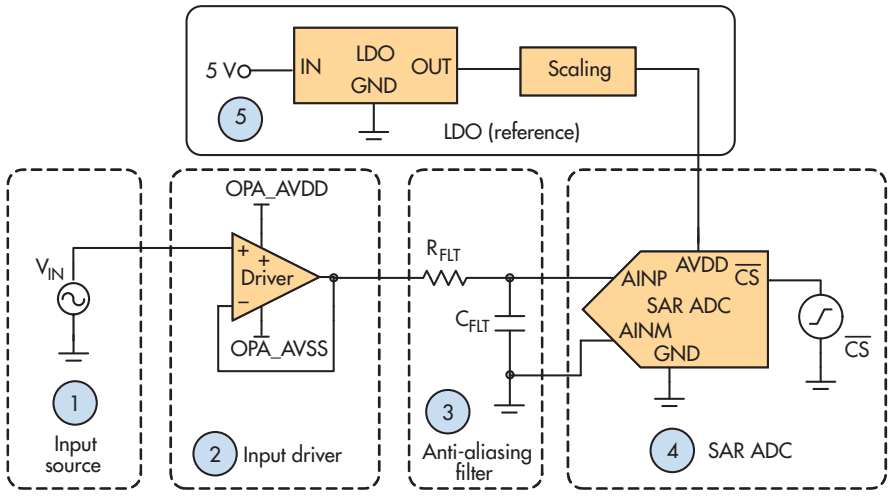
Let's look at some power-efficient data-acquisition designs targeting three very different applications and performance levels, and examine what steps we can take to reduce power consumption while maintaining performance.

LOW-SPEED APPLICATIONS

Many data-acquisition applications don't need blazing speeds because the physical quantities measured by the input sensors change relatively slowly. In this application space, battery-powered designs are common.

Examples of such systems include wearables (fitness bands, smart watches; CO_2 detectors, smoke detectors, or smart thermostats in home automation); industrial modules (remote sensors or data loggers; glucose meters, cardiac monitors, and similar portable or implantable medical devices); and security equipment (cameras or motion detectors).

These systems often must run for extended periods—months or even years—on a single battery charge. To minimize power consumption, each electronic component in the design should consume as little power as possible when performing its necessary function and go into a low power



1. A low-power data-acquisition node includes five main blocks.

state as often as possible. Reducing the power consumption translates into extended battery life and a market advantage.

Many low-power systems must also be very small. The size constraint might limit the number of suitable devices, and potentially force the selection of a converter with higher power consumption or lower performance than desired.

Design	#1	#2	#3
Resolution	12 bit	12 bit	12 bit
Throughput	100-500 ksps	500 ksps – 1 Msps	<10 ksps
Input driver	OPA314	OPA835	No driver
SAR ADC	ADS7042	ADS7042	ADS7042
Power dissipation	1000 µW	2.5 mW	<1 µW

2. These represent three design options for a low-power data-acquisition system.

Figure 1 shows the main building blocks in a low-power data-acquisition system. The characteristics of the input source (1)—output impedance, output voltage, frequency, etc.—determine the selection of the input driver (2) and the anti-aliasing filter (3). The driver output feeds the SAR ADC (4); the SAR power consumption scales with the sample rate. The LDO (5) provides low-noise system power and the voltage reference for the ADC.

Let's examine three separate designs optimized for three different sets of requirements. All three are based on the TI ADS7042, a 12-bit SAR converter optimized for extremely low-power, small-form-factor applications. The examples show some of the design tradeoffs needed to give the lowest power and smallest size for the given applications.

Design number 1 is a 12-bit, 500-ksample/s data-acquisition system optimized for applications such as current monitoring, battery monitoring, electromyography or EMG, skin impedance, and wearable fitness devices. If the input signal has a high-impedance output and low input frequency, it's important to isolate the ADC input by adding a low-power input driver. The device chosen is the OPA314, a low-power, low-noise op amp with rail-to-rail inputs and outputs (RRI/O) and a gain bandwidth (GBW) of 3 MHz. The device provides the output current drive needed to charge the internal switched-capacitor input of the SAR ADC. This design optimizes the drive amplifier and anti-aliasing filter for the required sampling rate and consumes 1 mW of power.

Design number 2 optimizes the drive amplifier and anti-aliasing filter for an application with a sampling rate up to 1 Msample/s. For example, a use case may have an input signal that's greater than 10 kHz and requires a response time of less than 2 µs. Compared to the previous design, this design uses an OPA835 for the input driver. With a unity-gain bandwidth of 56 MHz, this higher-bandwidth amplifier still satisfies the power requirements and ENOB for the application. This design consumes 2.5 mW of power.

Design number 3 suits low-sample-rate (<1 ksample/s) applications such as tilt, gyro, pressure, temperature, gas, chemical, or blood-glucose sensor measurements. The critical parameter in these cases is the output impedance of the input source. If the input is very slow moving, has a low output impedance, and the overall system ENOB isn't a critical parameter, it's possible to completely omit the input driver.

Figure 2 compares features and power consumption of the three designs.

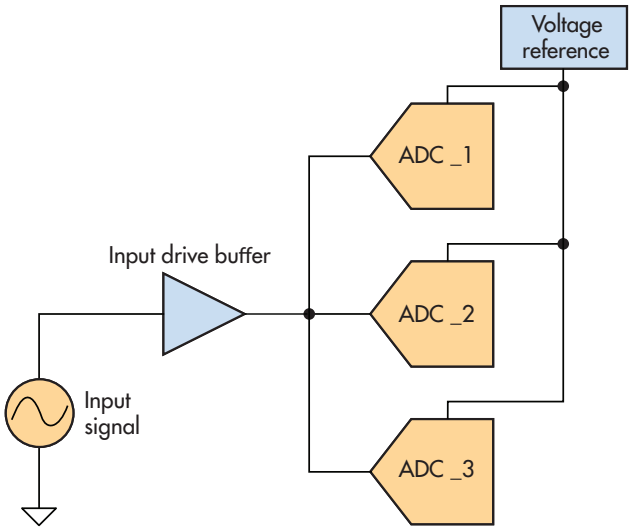
TI's TIPD168 is a verified Precision Reference Design that covers the three designs discussed. The package includes a detailed description of the design procedure, simulated results, and the actual test results of a discrete data-acquisition block.

POWER-EFFICIENT DATA CONVERTERS FOR HIGH-PERFORMANCE APPLICATIONS

What if your application requires higher converter performance than we've talked about thus far, but low power is still a requirement? The pipeline converter is the first option considered by many designers. It offers a high sample rate, but is a power hog because it requires a greater number of internal comparators and amplifiers than a successive-approximation converter of the same resolution.

Combining the output of multiple converters—a technique known as interleaving—enables a system to maintain resolution while increasing the effective sample rate, helping to bridge the speed gap between SAR and pipeline architectures. In an equivalent system, interleaved SAR ADCs can help reduce the overall power consumption, cost, and size of the design compared to pipeline ADCs.

An interleaved converter samples the input signal with multiple synchronized data converters running from a common clock with multiple phases. The sampling period for each converter is phase-shifted, and the results from each converter are then combined to form the output data



3. A single input buffer and voltage reference eliminate two error sources in an interleaved converter design.

stream, effectively increasing the system sampling rate while maintaining the resolution of the individual ADCs.

Phase-shifted versions of a single clock generate the conversion signals for all of the ADCs. The phase shift between clocks for an n-converter design is (360/n)°. Therefore, in a three-converter design, the clocks should be phased at intervals of 120°.

PAY ATTENTION TO ADC DIFFERENCES

Interleaving multiple ADCs may have advantages in power efficiency, but even with modern production techniques, the ADCs aren't completely identical, and this must be taken into account. For example, mismatches between external voltage references and driver amplifiers are potential sources of error. A single front-end driver amplifier for all ADCs eliminates these offset variations, and a single voltage reference eliminates input signal gain variations. *Figure 3* shows the resulting block diagram.

It's important to calibrate out mismatches in offset and gain errors between the individual ADCs to achieve the highest performance from the interleaved design. Otherwise, the offset error will appear as a noise spur at the sampling frequency of the ADC, and the gain error will appear as a noise spur at the sampling frequency plus or minus the input signal frequency. These errors will degrade the ADC's overall performance, reducing the signal to-noise ratio (SNR).

These errors can be calibrated out with post-processing, but this causes additional complexity for the host microcontroller. To eliminate this additional complexity, some SAR ADCs offer extremely low gain error and integrated offset-calibration circuitry.

	1x ADS7056	3x ADS7056
Resolution	14 bit	14 bit
Sampling rate	2.5 Msps	7.5 Msps
SNR (dB)	74.9	73
THD (dB)	–85	–83.8

4. Interleaving three ADS7056 SAR converters gives three times the sampling rate with only a slight degradation in SNR and THD.

TI's ADS7056, for example, is a SAR ADC with an integrated offset-calibration feature and a typical gain error of only ±0.01% (or 3.2 LSBs at 14 bits). As a result, the ADS7056 doesn't generally require gain-error calibration.

In a performance comparison, three 14-bit ADS7056 SAR ADCs with a sampling rate of 2.5 Msamples/s each were interleaved to achieve an effective system sampling rate of 7.5 Msamples/s. *Figure 4* compares the interleaved system performance compared to that of an individual ADC. The overall performance metrics of the ADC—including resolution, SNR, and total harmonic distortion (THD)—remain almost the same, but the sampling rate increases by a factor of three.

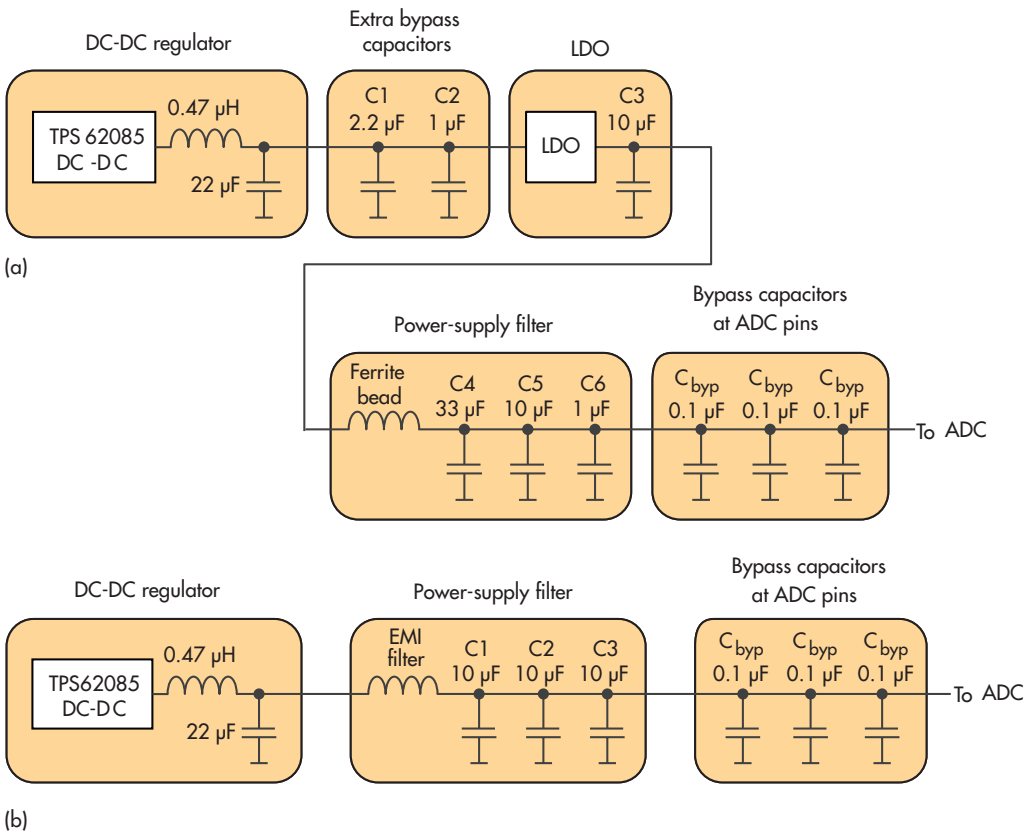
How does the performance of an interleaved SAR design compare to that of a pipeline converter with equivalent performance? *Figure 5* tells the tale. The resolution, sampling rate, and SNR are comparable, while the power, package size, and price are greatly reduced. The improvement in power consumption is particularly striking—a reduction of more than 93%!

AT HIGH SAMPLE RATES, TAKE A SYSTEM-LEVEL APPROACH TO LOWERING POWER CONSUMPTION

When dealing with gigabit-per-second sample rates, a low-power SAR architecture isn't an option, so we must cast our

	3x ADS7056	THS1408
Resolution	14 bit	14 bit
Sampling rate	7.5 Msps	8 Msps
SNR (dB)	73	72
Power consumption (mW)	17.5	270
Package area (mm^2)	6.75	81
Price (1 ku)	$6.00	$20.05

5. The chart compares the performance of an interleaved SAR design versus a pipeline design.



6. The traditional power supply design (a) includes an LDO to remove switching noise. Optimizing the power-supply filter (b) allows its elimination.

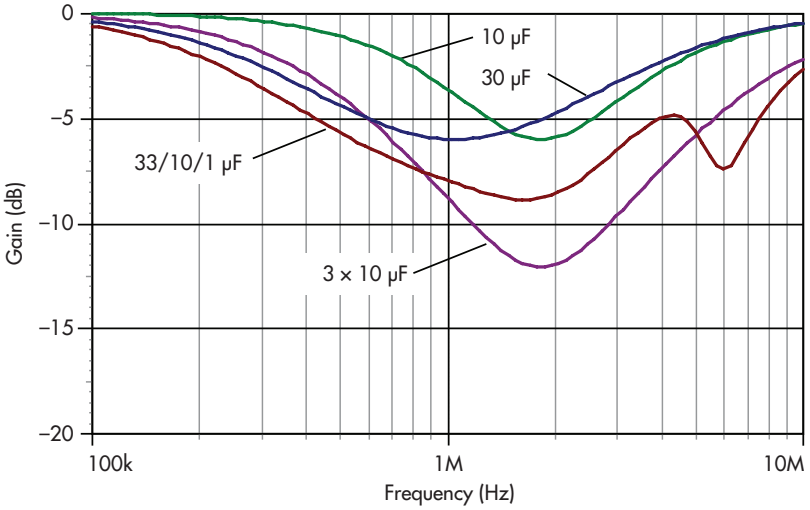
net a little wider. One valuable power-reduction technique is to pick an ADC that allows you to eliminate other devices for lower overall system power consumption, although the ADC itself might not be the lowest-power component available with the required performance.

The ADC32RF45 is a good example. It's a dual-channel, 14-bit, 3-Gb/s ADC for high-performance RF applications such as military radios, LAN/WAN test equipment, and signal analyzers. These applications aren't usually considered low power, but the ADC32RF45's high sample rate makes it possible to eliminate the entire RF downconversion stage. The result is a simpler signal chain with a much smaller footprint on the printed circuit board (PCB).

The power supply presents another opportunity to reduce power consumption. The traditional power supply for a high-current converter starts with a switching dc-dc converter. A switcher is an efficient means to generate the required voltage, but the output includes switching noise and flicker noise. Consequently, an LDO regulator is added to improve the power-supply noise rejection, followed by a power-supply filter. Capacitors at the ADC pins provide bypassing of the converter switching currents.

A modern dc-dc regulator such as TPS62085 uses a switching frequency of 2.4 MHz to reduce inductor size. At this frequency, though, the power-supply rejection ratio (PSRR) of the LDO may only be 20 to 30 dB. It's possible to eliminate the LDO and achieve a similar level of attenuation with an optimized power-supply filter that's tuned to provide 20 to 30 dB at the TPS60285's switching frequency.

Figure 6 shows the traditional and improved power-supply designs. The power-supply filter in the traditional version has several different capacitors to try and filter a wide range of spur frequencies. The tuned filter uses three parallel 10-µF capacitors to achieve a 6-dB performance improvement at 2 MHz. *Figure 7* compares the responses of the two capacitor combinations, plus the single-



7. A simulation shows the improved response of the 10-µF parallel capacitor combination versus the 33-µF/10-µF/1-µF combination, including package parasitics.

capacitor responses.

The optimized design also replaces the ferrite bead with an electromagnetic-interference (EMI) suppression filter. To be effective against switching noise, the ferrite bead should have a high impedance at the 2-MHz frequency of interest. Most ferrite beads have high impedance around 100 MHz, but very little impedance at low frequencies, so they're not effective at attenuating switching spurs. An EMI suppression filter such as Murata's NFM31PC276B0J3 has an insertion loss of approximately 85 dB at 3 MHz and can provide as much as 25 dB of rejection in the application.

Read more about power supply design for high-speed data converters in this article from TI's Analog Applications Journal. For more information on Texas Instruments' deep portfolio of ADCs, check out this product overview.

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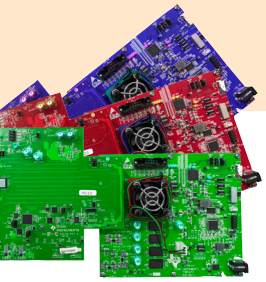


PAUL PICKERING, Contributing Editor

CHAPTER 3:

Behind the ADC Veil: Demystifying Common DC Specifications

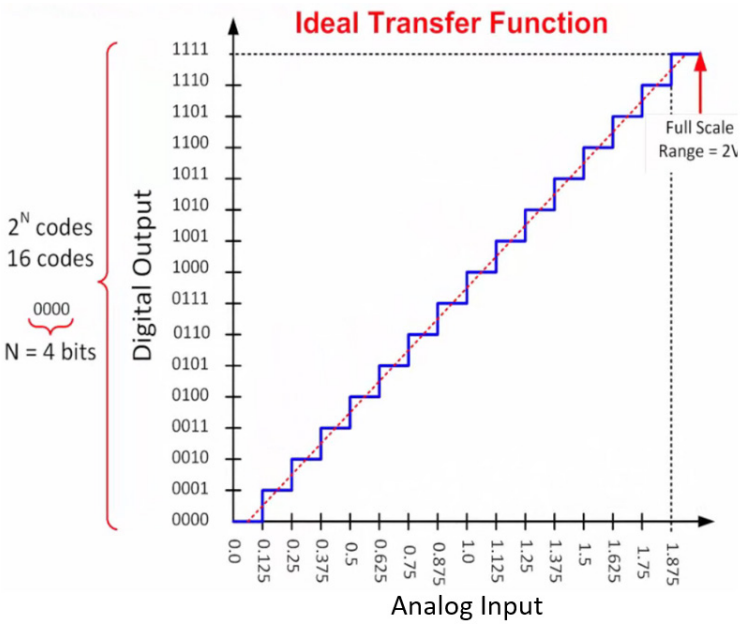
What are the real-world numbers? Though many datasheet specifications are guaranteed, certain parameters are listed as typical values without minimum and maximum values.

As its name implies, the function of an analog-to-digital converter (ADC) is to convert analog signals to digital representations for processing by a microcontroller (MCU), field-programmable gate array (FPGA), digital signal processor (DSP), or similar device.

In this article, we'll review one of the most popular ADC architectures and how the dc specifications of a practical device differ from the ideal ADC model.

WHAT DOES AN IDEAL ADC LOOK LIKE?

Regardless of how it accomplishes the task, an ADC produces a digital output from an analog input signal, a process known as quantization. Quantization error results from this process since a digital signal can only have discrete values, whereas an analog signal may have any value within the dynamic range of the signal.



1. The transfer function of an ideal ADC.

The quantization process leads to stair-step transfer function: *Figure 1* shows this characteristic appearance in the transfer function of an ideal 4-bit ADC. This ADC divides the input voltage into 2^4, or 16, possible output codes, from 0000 to 1111.

In general, an n-bit ADC has 2^n output codes. For a full-scale output of 2 V, each increase or decrease of 0.125 V (= $2/2^4$) at the input (V_{IN}) causes an increase or decrease of 1 count at the output. V_{IN} = 0 gives an output of 0000; V_{IN} = 0.125 V gives 0001, and so on.

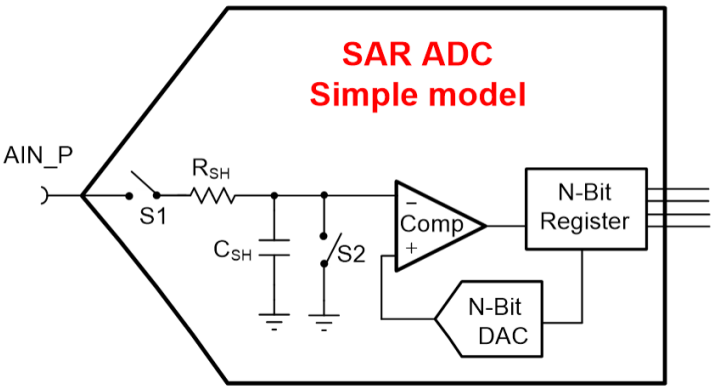
Each change from one code to the next takes place precisely at 0.125-V increments, so all of the steps are identical. Plotting the center points of each step yields a straight line.

THE SAR ADC: A DATA-CONVERSION WORKHORSE

Of course, although the performance of a real ADC comes very close to perfection (especially one of ours, LOL), several sources of error show up as deviations from Fig. 1's ideal transfer curve.

There are many ways to convert an analog signal into its digital counterpart. All of them have different characteristics, but we'll use the successive approximation register (SAR) as an example in this article because it's suitable for a wide range of applications and is the default choice for general-purpose use.

SAR sampling rates typically range between 1 ksamples/s to 5 Msamples/s; resolutions can range up to 20 bits. SAR ADCs have very low power consumption, so they're suitable for use in battery-powered applications. In addition, the



2. The SAR is a widely-used general-purpose ADC architecture.

power consumption scales with the sampling rate, so the SAR can achieve ultra-low power consumption at slow sampling rates.

A basic SAR topology *(Fig. 2)* consists of a sample-and-hold structure, an analog comparator, a SAR, and an *n*-bit digital-to-analog converter (DAC), where *n* is the resolution of the ADC.

The SAR conversion cycle has two stages—the sample phase and the conversion (or hold) phase:

1. During the sample phase, the ADC captures the input voltage to be converters. S1 is closed and S2 is open. An internal sample-and-hold capacitor (C_{SH}) charges to AIN_P through R_{SH}.
2. S1 opens; C_{SH} stores the input voltage sample; and the conversion phase can begin. This has several steps:

a. A comparator compares the sampled AIN_P to the output of the internal DAC; the DAC takes its input from the SAR. The most significant bit (MSB) of the SAR is initialized to 1 and all other bits are 0, so the DAC output voltage $V_{CDAC} = V_{REF}/2$.

b. The output of the comparator feeds the SAR: if AIN_P > V_{CDAC}, the bit remains at 1, otherwise it's set to 0.

c. The next most significant bit is then set to 1 and AIN_P is compared to the new V_{CDAC}. This bit is set to the comparator output.

d. Step c repeats until every bit in the SAR has been tested; the SAR then contains a digital representation of AIN_P.

The result is now available for use and a new sample phase can begin.

The *n*-bit DAC forms the heart of the SAR ADC. The standard architecture uses an array of capacitors with binary-weighted values to form a capacitive DAC (CDAC). *Figure 3* shows a typical CDAC; a 5-bit converter is shown. Note that there are six capacitors: the MSB capacitor is on the left and there are two LSB capacitors so that the total capacitance is 2C.

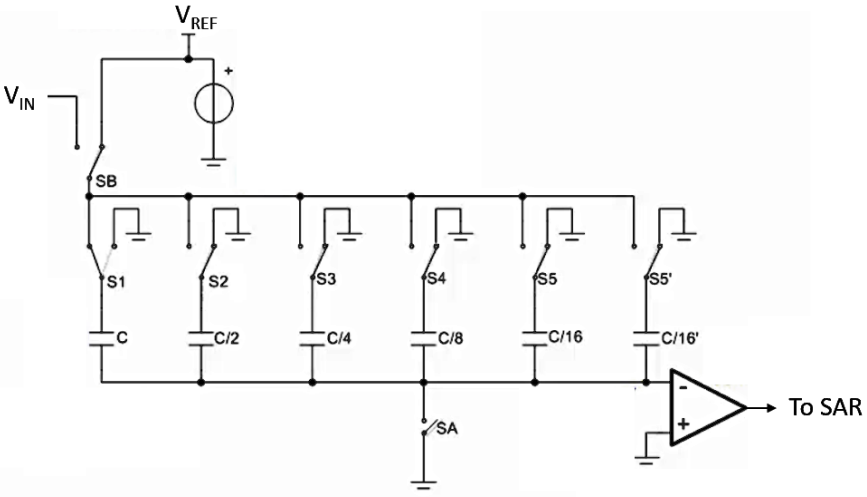
The operation of the CDAC is based on the principle of charge redistribution. A detailed description of its operation in the SAR can be found in this TI training video.

REAL-WORLD ADC CIRCUIT CHARACTERISTICS AFFECT DC PERFORMANCE

Nonlinearities in any block directly affect the ADC's performance. Let's look at some circuit characteristics of a real device.

Input Capacitance

The value of the input capacitance (C_{IN}), which is typically specified in the datasheet, depends on the mode of operation. For example, the ADS9110, an 18-bit SAR, has C_{IN} = 60 pF when in sample mode, and C_{IN} = 4 pF when in hold mode.

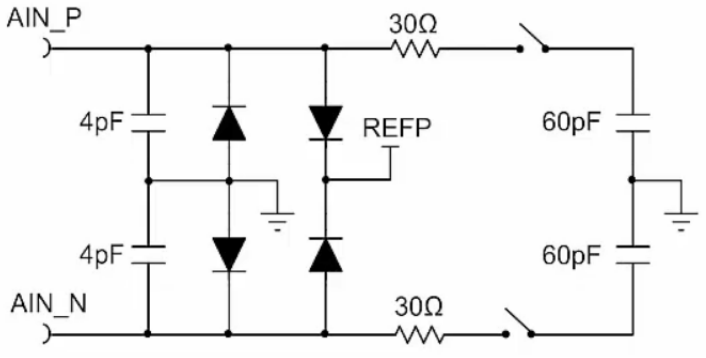


3. A 5-bit CDAC architecture.

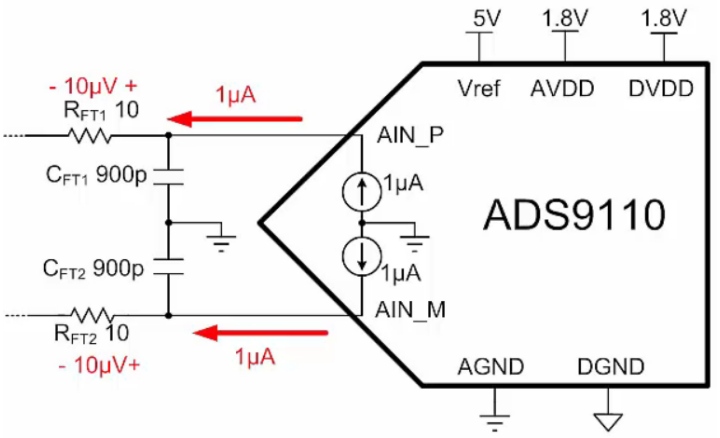
Why is this? *Figure 4* shows a more detailed model of the ADS9110 sample-and-hold (S&H) circuit. The part has a differential input: it samples both AIN_P and AIN_N, so there's an S&H circuit for each one with R_{SH} = 30 Ω and C_{SH}= 60 pF.

In sample mode, S1P and S1N are both closed; therefore, $C_{IN} \approx C_{SH}$: 60 pF typical. In hold mode, C_{SH} is disconnected from the input pins. C_{IN} then equals the parasitic capacitance of the input ESD diode structure, a typical value of 4 pF.

In a real-world device, the ESD structures and



4. The model of the ADS9110 sample-and-hold circuit includes ESD structures and protection diodes.



5. The ADS9110 input model for leakage current.

input parasitics also give rise to an *input leakage current* (I_{IL}): a dc current that flows into or out of the ADC input pins. As shown in *Figure 5*, I_{IL} can be modeled as a dc current source on AIN_P and AIN_N. The typical magnitude can range from nanoamps to microamps, and the current flow can be positive or negative; both magnitude and polarity can vary between devices.

As shown in Fig. 5, the leakage current can generate an offset error when it flows through any source impedance. For the 18-bit ADS9110 with a 5-V reference, a 1-μA leakage flowing through 10 Ω equates to an offset of 10 μV. That's only 0.5 LSB for the ADS9110 but remember that ±1μA given in the datasheet is only a typical value (see below for a discussion), so it could be considerably higher and still meet the specification.

Input Impedance

An unbuffered ADC has a switched-capacitor input stage, so its input impedance varies with frequency. The dynamic impedance depends on input leakage currents as well as the switching and charging of the input capacitance. The capacitive element doesn't affect a dc input voltage, but it does affect the settling time when the input changes.

Some data converters include a front-end amplifier input that has a fixed input impedance set by the resistance of the gain-setting resistors. The ADS8681 in *Figure 6* is one example: It's a SAR ADC with an integrated programmable gain amplifier (PGA) and has a 1-MΩ input impedance.

Adding an external resistance will change the gain of the amplifier. If this resistance is unknown or a dynamic impedance, it will introduce a system gain error, as discussed below.

REAL-WORLD TRANSFER CURVES

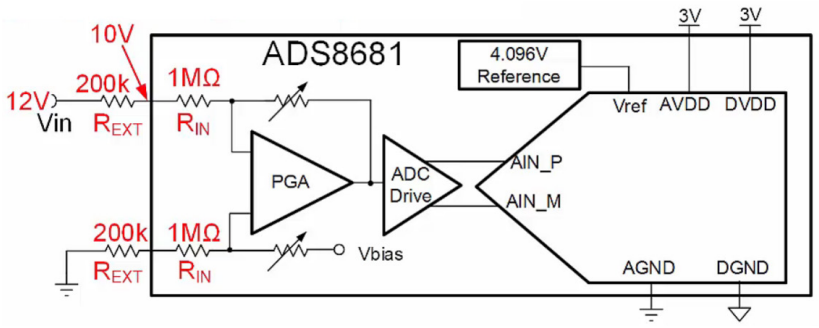
The differences discussed above, and others, give the real SAR ADC a transfer curve that's different from the ideal in Fig. 1. For example, mismatches in the CDAC—mismatches in the weighted capacitors, for example—are one of the leading contributors to nonlinearities in the transfer curve.

Since the ADC transfer function isn't perfectly linear, one common means of evaluating it is to apply a linear fit curve to the specification being considered. The most common technique is an end point linear fit, in which the first and last points on the ADC transfer function define the straight line.

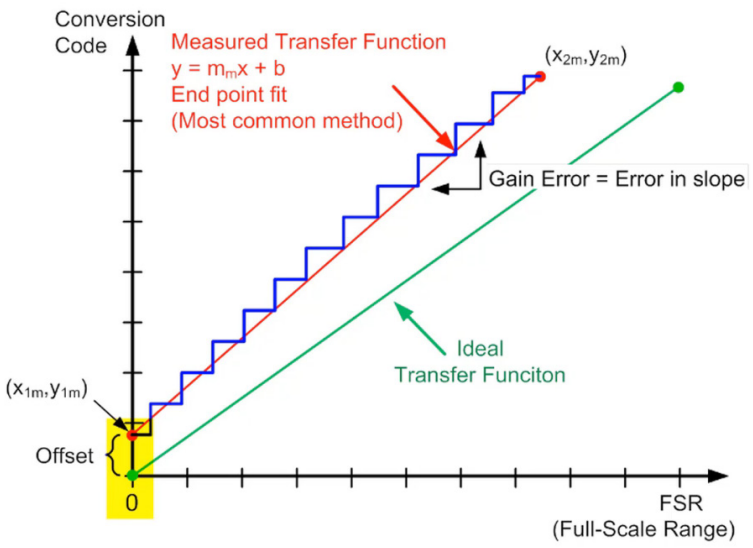
Figure 7 illustrates this approach applied to two common dc errors: offset error and gain error.

A straight line has the equation $y = mx + b$, where m is the slope of the line and b is the intercept on the Y-axis. The constant b is the value of the transfer function when x equals 0. In this case, it's the offset error.

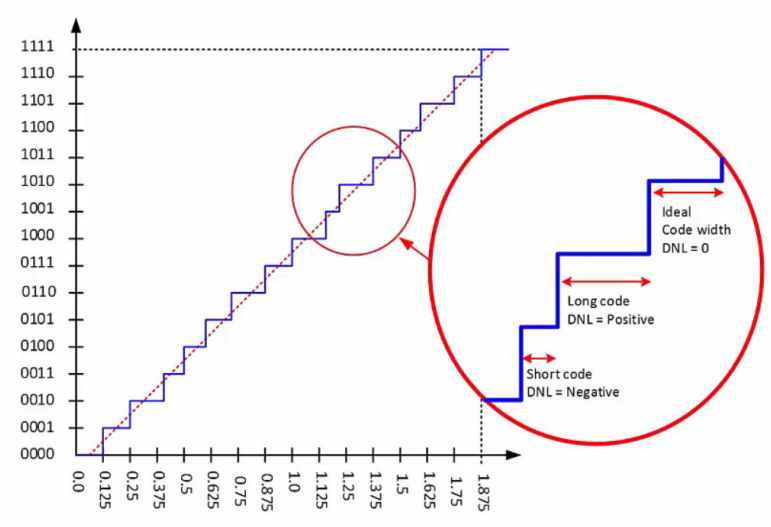
The offset error limits the available range for the ADC. A large positive offset error causes the ADC to output the maximum output code before the input voltage reaches the maximum limit. Conversely, a large negative offset error



6. The ADS8681 has a 1-MΩ resistive input impedance courtesy of its PGA buffer.



7. The linear fit method applied to the offset and gain errors.



8. An ADC can exhibit both positive and negative DNL at different locations on the transfer curve.

will cause the ADC to output all zeros before the input has reached the minimum limit.

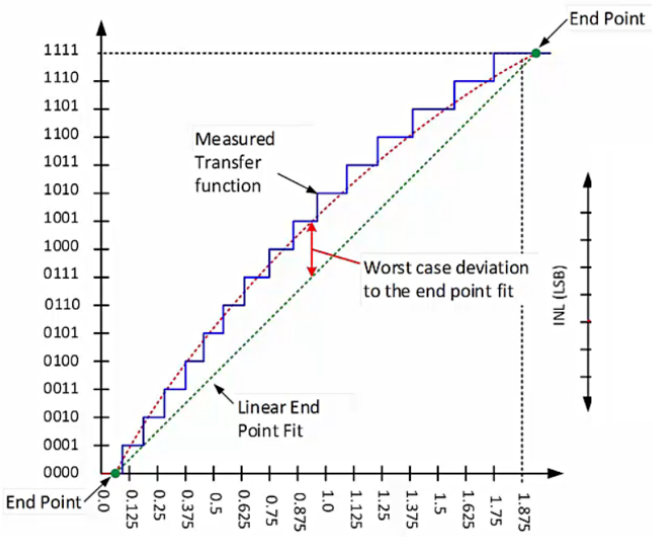
The gain error is the difference between the ideal slope and the measured slope, expressed as a percentage. In many cases, this error can be eliminated with a simple two-point calibration. If an external resistance is added *(Fig. 6, again)*, its value can be taken into account. You can find out more about this topic in the application note "*Reducing Effects of External RC Filter on Gain Error and Drift in SAR ADC with Integrated AFE.*" Or consult TI's Analog Engineer's Circuit Cookbook, free to download.

Differential Nonlinearity

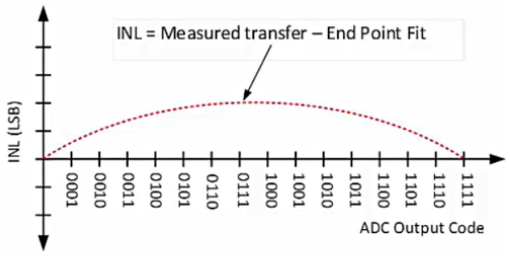
Differential nonlinearity (DNL) is defined as the maximum and minimum difference in the step width between the actual transfer function and the ideal transfer function.

As shown in *Figure 8*, DNL produces quantization steps with varying widths, some wider than the ideal value (positive DNL) and some narrower (negative DNL). An ideal device, of course, has a DNL of zero: All of the steps are the same size.

In severe cases, the DNL can be large enough to cause a missing code. A code transition is completely skipped and that particular bit combination never appears on the output. Most modern ADCs are designed and tested to ensure that they will not have this problem. Datasheets often provide a no-missing-code (NMC) specification to highlight that the



9. These two methods are used to specify INL.



11. The statistical variation of many datasheet parameters shows a Gaussian distribution.

SYSTEM PERFORMANCE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			12		Bits
NMC	No missing codes		12			Bits
INL	Integral nonlinearity	AVDD = 3 V	–1	±0.7	1	LSB[2]
		AVDD = 1.8 V	–2	±1	2	
DNL	Differential nonlinearity	AVDD = 3 V	–0.99	±0.5	1	LSB
		AVDD = 1.8 V	–0.99	±0.7	2	
E_O	Uncalibrated offset error	AVDD = 1.65 V to 3.6 V		±12		LSB
	Calibrated offset error[3]	AVDD = 3 V	–3	±0.5	3	
		AVDD = 1.8 V	–4	±1	4	
dV_{OS}/dT	Offset error drift with temperature			5		ppm/°C
E_G	Gain error	AVDD = 3 V	–0.1	±0.05	0.1	%FS
		AVDD = 1.8 V	–0.2	±0.1	0.2	
	Gain error drift with temperature			2		ppm/°C

10. A summary of the dc performance specifications for the ADS7043 12-bit SAR ADC. (Source: TI: "ADS7043 SAR ADC" PDF)

converter will not have missing codes.

Integral Nonlinearity

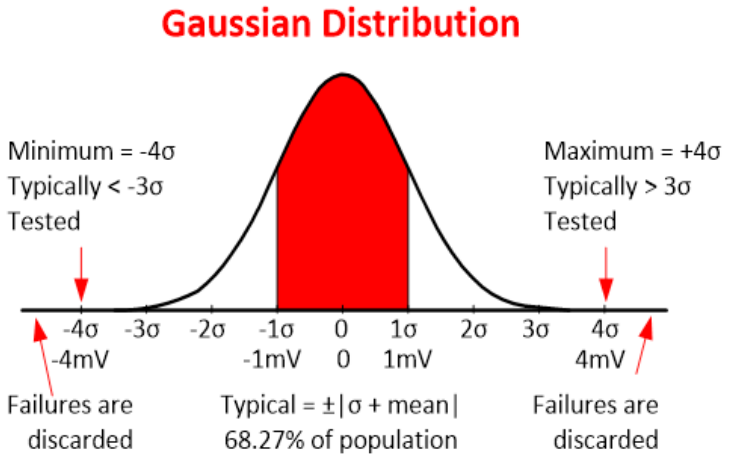
Integral nonlinearity (INL) is a measurement of how close the real-world ADC transfer function compares to a straight line. To eliminate the effects of gain and offset error, the measured transfer function is compared to an ideal straight line that's fit to the endpoints of the ADC transfer function. The deviation between the ideal line and the measured function is the INL error. Again, the performance of the CDAC has a direct effect on the ADC's overall INL performance.

In the 4-bit example shown in *Figure 9*, the green dashed line is the end-point fit of the transfer function. The green line starts at the first code, 0000, and ends on the last code, 1111. For a perfectly linear ADC, the straight-line fit would be directly down the middle of the ADC transfer function. The measured function, in blue, deviates away from the linear fit, so the ADC has a positive INL error.

As with DNL error, the INL can be displayed versus the ADC output code in terms of LSBs *(see Fig. 10 for an example)* or stated as a percentage of the full-scale range.

DECODING THE DATASHEET: THE STATISTICS BEHIND THE NUMBERS

The dc specifications we've discussed above are summarized in a table in the datasheet, plus several graphs that show their variation with temperature, reference voltage, and other parameters. *Figure 10* illustrates the summary table for the



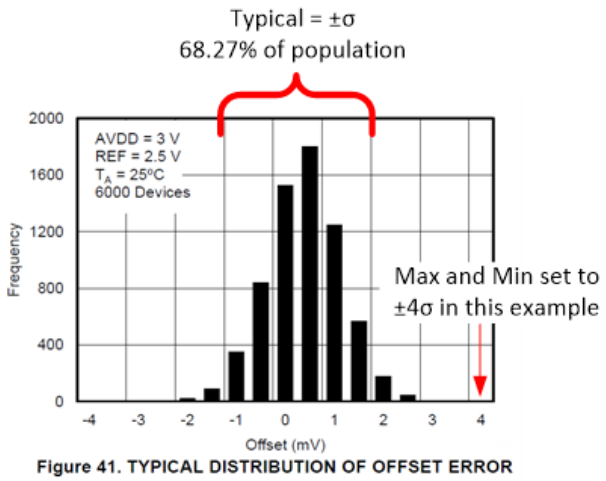


Figure 41. TYPICAL DISTRIBUTION OF OFFSET ERROR

ADS7043, a 12-bit SAR ADC.

The semiconductor manufacturing process is tightly controlled, but there's still a slight part-to-part variation. How do manufacturers ensure that the values given in the datasheet remain valid?

The minimum and maximum values are tested during production. To calculate a typical value, we turn to statistics. The Gaussian (or normal) distribution describes the distribution of physical quantities (e.g., datasheet parameters) that result from the combination of many independent processes, such as the steps in a semiconductor manufacturing process.

Figure 11 shows the Gaussian distribution applied to the offset error of an ADC. For a zero-centered specification, the typical value is the absolute value of one standard deviation plus the mean of the distribution. In this example, the mean is zero and the typical offset is ±1 mV; this corresponds to ±1 standard deviation. Since parts with values outside the minimum and maximum are discarded, the distribution is actually a truncated Gaussian distribution.

It's shown that 68.27% of the population falls within one standard deviation of the mean, but the other parts do not, so it's wise to treat typical values with caution when performing design calculations. The maximum and minimum limits are set to minimize yield loss during manufacturing. Typically, the maximum is set above three standard deviations; 99.7% of the population is within this limit. In this example, the maximum was set to four standard deviations.

CONCLUSION

The SAR architecture is widely used for analog-to-digital conversion, but the performance of a real-world device deviates in several ways from that of an ideal model. This article has provided insight into some of the common dc specifications in the SAR datasheet.

In addition, even though many datasheet specifications are guaranteed, certain parameters are listed as typical values without minimum and maximum values. This article has also reviewed the statistics behind these parameters.

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Comparing the ideal ADC transfer function to the measured result that includes gain and offset error effects

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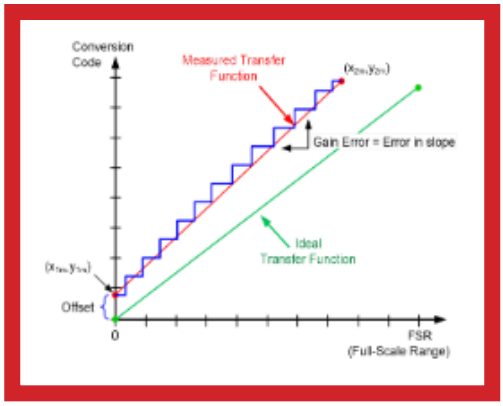
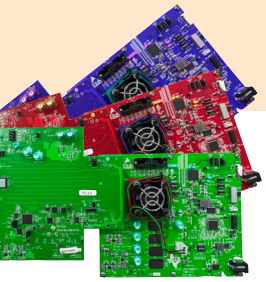




PAUL PICKERING, Contributing Editor

CHAPTER 4:

Small IS Beautiful: Tiny Packages Help Designers Do More with Less

Such miniaturized packages, from die-size ball grid arrays to extra-small outline no leads, are the way of the future in practically all portable and wearable applications. So, yes, "size does matter."

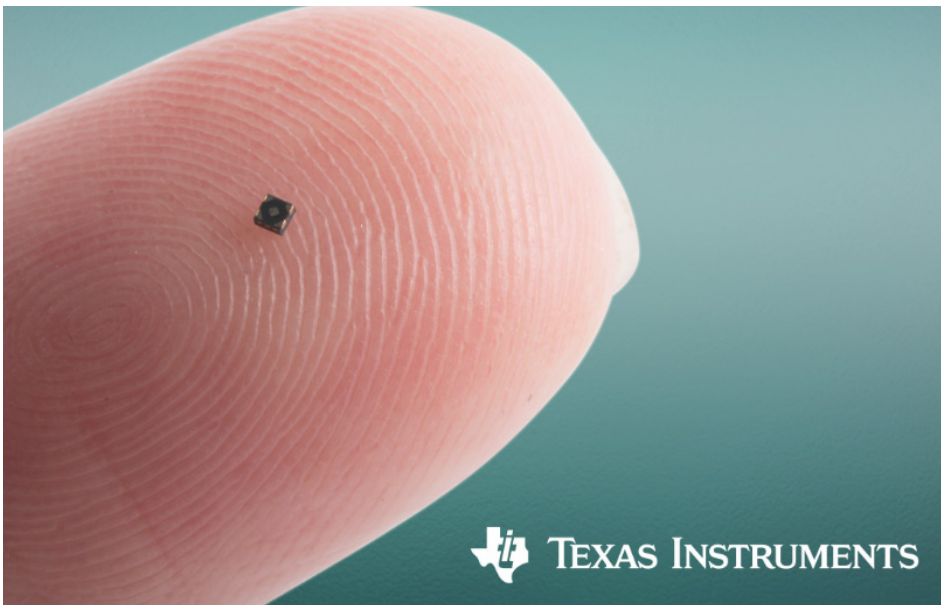
It'll come as no surprise to any savvy buyer, and certainly not to any design engineer, that each new generation of electronic products packs more performance into a smaller package than the product it replaced. No matter whether it's a remote industrial sensor node or the next smart wearable device, space is becoming an increasingly scarce resource.

Something's gotta give. In this case, many things. Fitting the increased capability into a smaller volume requires the designer to make improvements in multiple areas. The three biggest keys to succeeding, however, are to reduce the overall power consumption to allow the use of a smaller battery; integrate multiple functions into a single package to cut down on the number of devices; and choose individual components in the smallest available packages.

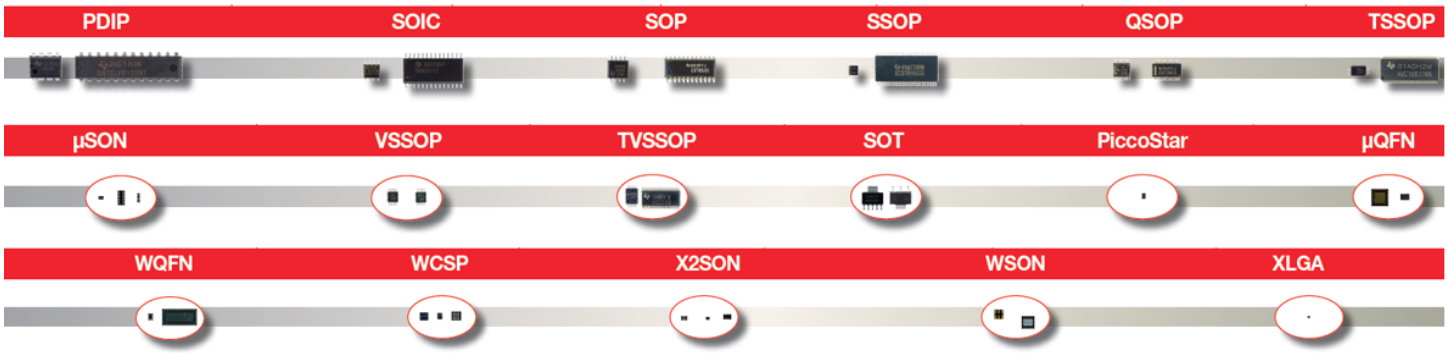
Manufacturers of both active and passive devices are keenly aware of the push toward smaller sizes. Just look at resistors, for example. Back in the old days before surface-mount technology (SMT), the standard small-signal resistor was a 1/8-W axial through-hole device measuring about 1.8 mm in diameter and 3.0 mm long, plus extra for the leads. The equivalent now is the 0201 surface-mount resistor. Yes, it only handles 50 mW, but it measures 0.3 × 0.6 mm, a reduction in area of 96%.

Integrated circuits are following a similar path. In some cases, manufacturers can reduce the overall size of their products by integrating more functions into a single part. Even single-function devices, though, such as op amps and LDO regulators, are undergoing some serious shrinkage—from leaded dual-inline packages to SOICs to SOT, and below. Traditional packages are much larger than the die they contain, as they must also house the lead frame, the bond wires, etc.

In a chip-scale package, the size of the package approaches the size of the integrated circuit itself. This package requires specialized manufacturing techniques, but brings benefits in addition to smaller size. For instance, the



1. Better not sneeze: Aimed at IoT and personal electronics applications, the TLV9061 consumes only 0.64mm2 and is the world's smallest op amp. (Source: Texas Instruments)



2. Here are some of the package options available for a single-function device.

shorter interconnections reduce parasitics, giving improved performance.

Figure 2 shows a selection of packages for devices from 4 to 81 pins, ranging from the plastic dual inline package (PDIP), first introduced in 1964, to current-generation chip-scale offerings. Of course, this isn't the complete list. It doesn't include specialized packages, high-power packages, or packages with higher pin counts. The plastic ball-grid-array (PBGA) package can have up to 976 connections!

A REAL-WORLD EXAMPLE: DATA ACQUISITION

At the most basic level, a data-acquisition system takes in analog information from the real world, converts it to digital form, and uses the data to produce a desired result. Variations are found everywhere: in the factory, strapped to your wrist, at home, and in the doctor's office, for example. A data-acquisition signal chain has several distinct blocks:

- An analog front end (AFE) captures data from one or more sensors and converts it to digital form. This AFE typically includes pure analog components like op amps, and mixed-signal components such as analog-to-digital converters (ADCs).
- A microcontroller receives the data, processes it, and acts on the information.
- A mixed-signal output device such as a digital-to-analog converter (DAC) converts the microcontroller digital output back into analog form, perhaps to power a loudspeaker or actuator
- A power circuit takes input power and provides regulated supplies for all the devices

Although each one of these blocks has benefitted from the move to tiny packages, let's examine the op-amp and data-converter portion of the signal chain and see how new package options allow designers to dramatically reduce size while simultaneously increasing performance.

TINY OP AMPS FILL MANY ROLES

As fundamental building blocks in the signal chain, op amps must keep pace with emerging electronic design trends, including the move to successively smaller packages.

How do manufacturers add smaller package options to a part? For existing parts, they simply repackage the device without changing the underlying circuit. The venerable TL071 low-noise JFET op amp, for example, now comes in five different packages. While adding packages, older devices will typically still offer the original package options until the device itself is discontinued—nobody likes a manufacturer who forces them to re-layout their design. But newer devices offer both smaller packages and improved performance.

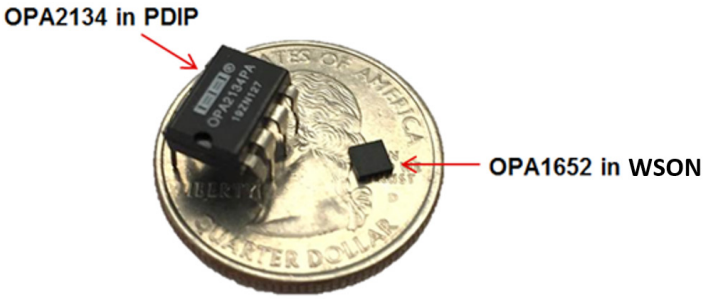
Portable audio requires tiny devices to produce high-quality sound for smartphones, Blu-Ray players, and headsets. Traditionally, designers have used precision audio op amps in DIP packages for audiophile products. The OPA2134 from the legacy Burr-Brown product line is one such device. It has low distortion, low noise, and has been a professional audio staple over the years.

But its PDIP and SOIC packages are an issue for portable applications with severe space constraints. Designers can now choose the OPA1652, which features upgraded performance and a smaller package compared to the OPA2134.

Performance-wise, the OPS1652 has lower noise (4.5 nV/√Hz at 1 kHz) and lower THD + N (0.00005%) than the OPA2134 (8 nV/√Hz and 0.00008%, respectively).

The OPA1652 is available in several packages, including the WSON no-lead package that features a thin profile for handheld applications. The OPA1652's version (DRG package code) has an exposed thermal pad and measures 3.0 × 3.0 mm- much smaller than the OPA214's standard PDIP package (6.35 × 9.81 mm).

For general-purpose use, the OPA171 is worth considering. It's is one of the first micropower 36-V op amps offered in



3. In addition to a dramatic size reduction, the OPA1652 audio op amp provides superior THD+N performance over the classic OPA2134.

both a single SOT553 (1.6 × 1.6 mm) package and a dual, very-thin shrink small outline package (VSSOP) (2.0 × 3.1 mm).

In addition to changing to tiny packages, new op amps are adding specialized features for new applications. Many battery-powered products spend much of their time in sleep mode and wake up periodically to perform scheduled operations, process an incoming message, or respond to an interrupt. A fitness band, for example, only wakes up to measure biometric data; when the user presses a button; or when pinged by a paired smartphone.

Conserving battery life is a top priority in these applications. In sleep mode, it's important to shut off as many devices as possible. While awake, the device must only power the blocks that are needed for the operation being performed.

These requirements have led to low-power op amps with a shutdown feature. The OPA2316S, for example, is a low-power CMOS op amp with a bandwidth of 10 MHz. The part operates down to 1.8 V and offers rail-to-rail input and output (RRIO) operation, making it suitable for low-voltage battery-powered devices. In shutdown mode, the OPA2316A consumes 0.01 µA typical. For the smallest size, it comes in a quad flat-pack no-lead (X2QFN) package measuring 1.5 × 2 × 0.4 mm.

DATA CONVERTERS: LINKING THE ANALOG AND DIGITAL WORLDS

The ADC and the DAC are two important blocks in the signal chain. Analog-to-digital conversion occurs on the input side; tiny packages are appearing in this category as well.

Numerous data converters are available in tiny packages. Here are a couple of examples.

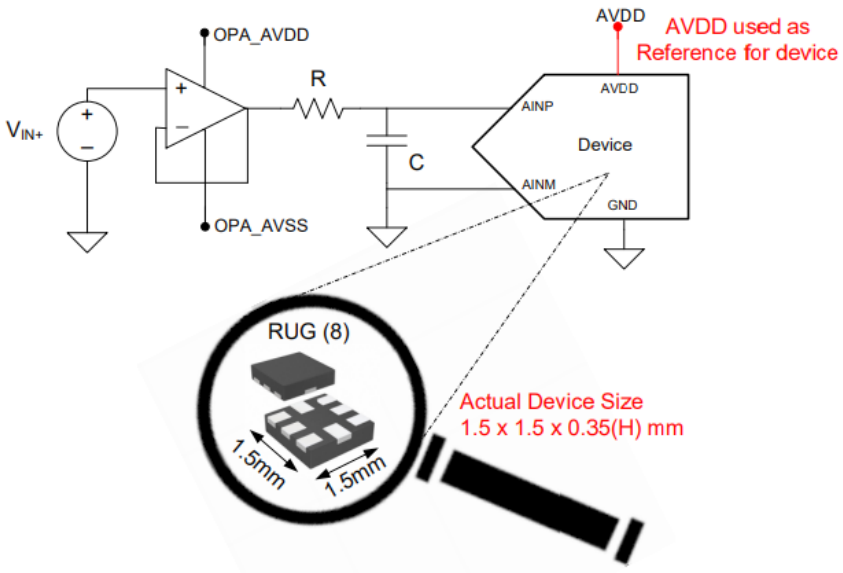
The ADS7040 is an ultra-low-power, 8-bit ADC that targets low-power data-acquisition, portable medical, and wearable applications, among others. This device also comes in the X2QFN package. Although it uses the successive-approximation register (SAR) architecture to achieve 1 Msample/s, the ADS7040 consumes only 171 µW when powered by a 1.8-V battery cell.

On the output side of the house, the DACx0504 is a pin-compatible family of low-power, four-channel DACs with 16- and 14-bit resolution and buffered voltage outputs. The DACx0504 includes a 2.5-V, 5- ppm/°C internal reference, eliminating the need for an external precision reference in most applications.

The device operates from a single 2.7- to 5.5-V supply, is monotonic, and provides ±1 LSB integral nonlinearity (INL) performance. The DACx0504 communicates via a 4-wire SPI-compatible serial interface at up to 50-MHz clock rate. Best of all, the DACx0504 is available in a 16-pin WQFN package (package code RTE) that measures 3.0 × 3.0 mm.

LAYOUT GUIDELINES FOR SMALL PACKAGES

Using tiny packages allows you to shrink the size of the design, but the small package dimensions leave very little room for error. It's important to follow manufacturer's recommendations when laying out the printed-circuit board (PCB) and later during manufacturing. Texas Instruments offers application notes that provide guidance for many tiny packages.



4. The ADS7040 shrinks a 1-Msample/s SAR ADC down to 2.25 mm2.

Three primary factors can make the difference with regard to package size and pitch: PCB manufacturing, solder application, and component placement.

Here are some general rules, using the Extra Small Outline No-Lead (X2SON) package as an example. This package comes in 5-pin (code DPW) and 6-pin (DTB) versions that measure 0.8 × 0.8 mm and 0.8 × 1.0 mm, respectively. These packages are used by both logic and analog devices including the TLV9061 shown in Fig. 1, a 10-MHz CMOS op amp that finds homes in many consumer and industrial applications.

PCB MANUFACTURING

The PCB footprint for the X2SON packages requires a spacing of 0.208 mm (8.2 mils), which is well within the limits of most established PCB manufacturers. The primary manufacturing concern comes from the method used to connect to the center pin(s).

There are two layout options for the center pin: place a trace on the same layer as the other pins; or use a via to connect to a trace on another layer. *Figure 5* shows recommended clearances in each case. Consult the guidelines in the application note for more information.

SOLDER-PASTE APPLICATION

Solder-paste application is an area of concern when the pads are very small. For instance, the correct amount of solder needs to be placed on the pads. There are several variables, including stencil thickness, solder type, and aperture size and shape. However, the X2SON packages maintain a 0.4 mm (15.7 mils) pitch, which allows for more error in the assembly process while maintaining a high yield. When following recommended guidelines, industry-standard Type III solder paste can also be used.

COMPONENT PLACEMENT

Using a one-third pad placement error as a guideline, the X2SON-5 package requires a minimum placement accuracy of ±83 µm (3.28 mils) to seat the part properly; the X2SON-6 requires an accuracy of ±72 µm (2.94 mils). The one-third pad error tolerance enables all pins to make good contact with the solder paste and be in reasonable alignment with their pads. During the solder process, the surface tension of the melted solder will align the part. Pick-and-place machines can typically place a component with an accuracy of ±30 µm, well within the requirements for the X2SON.

RESOURCES AND INFORMATION

Application guidelines are available for many of the newer tiny packages. AN-1112, for example, covers the die-size ball-grid-array (DSBGA) wafer-scale package. The complete list can be found here, including information on older through-hole and power packages.

For analog and logic devices, you can browse through the Analog and Logic Packaging guide. It lists all of the available packages by pin count, with photographs of each one. Find out more about TI's broad packaging portfolio at this link.

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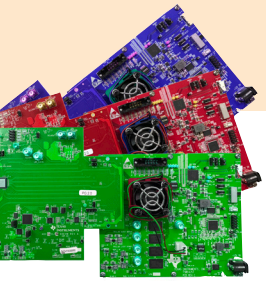


LOU FRENZEL, Contributing Editor

CHAPTER 5:

Fast ADC Facilitates Direct RF Sampling at Higher Frequencies

Simple in nature, the new RF-sampling receiver architecture yields major benefits at VHF, UHF, and microwave levels.

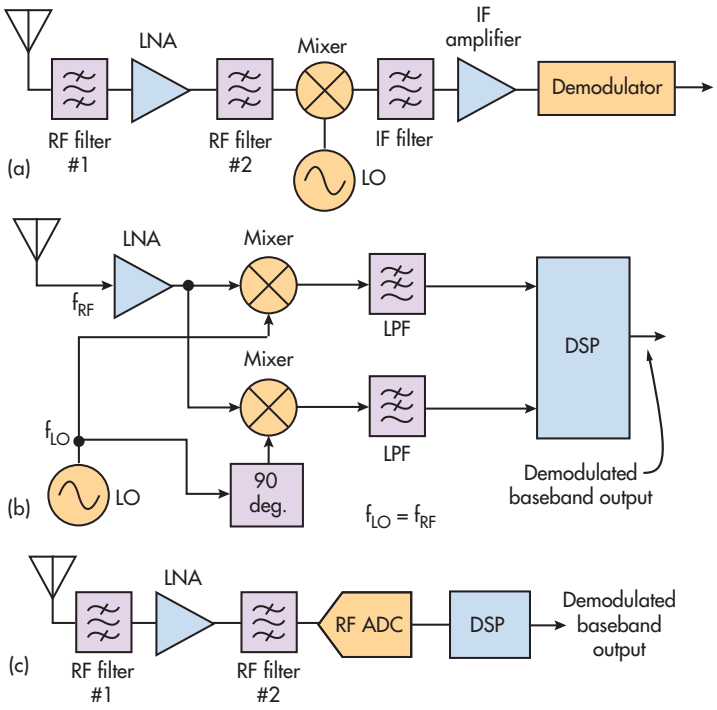
The critical component in all digital communications receivers is the analog-to-digital converter (ADC). The ADC sampling rate, bandwidth, and noise tolerance establishes the specifications and performance of the receiver. However, receiver architecture also plays a major role in its performance. An architecture that significantly improves performance over previous designs is direct RF sampling—and it's become more practical than ever thanks to the availability of fast wideband ADCs.

RECEIVER ARCHITECTURE REVIEW

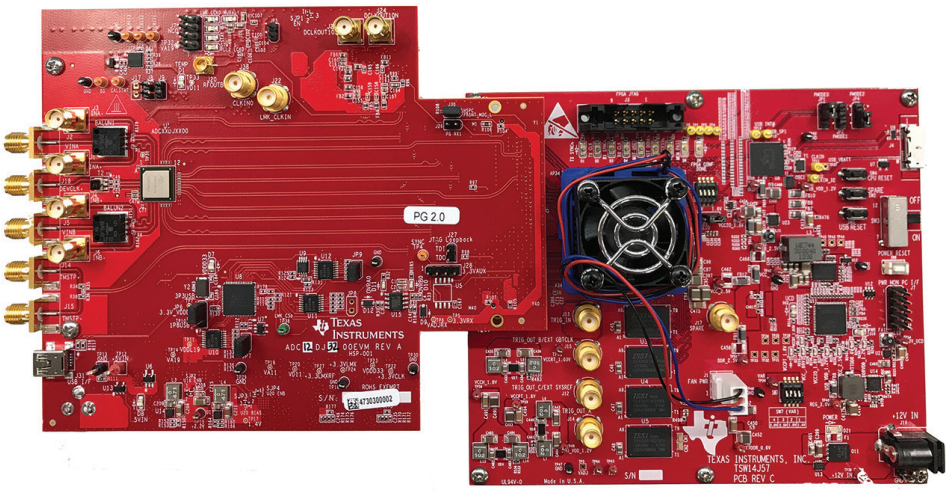
Perhaps the most widely used receiver architecture is the superheterodyne, where the received signal is downconverted to a lower intermediate frequency (IF) by a mixer before filtering and demodulation. In a typical arrangement *(see the figure, a)*, the bandpass filter (BPF) narrows the bandwidth and the low noise amplifier (LNA) boosts the signal level. The local-oscillator (LO) frequency mixes with the incoming signal to produce a lower IF. The signal modulation, bandwidth, and data are retained. A demodulator recovers the original data.

One major disadvantage of the superhet is that it uses many circuits and filters, increasing the cost. In addition, the local oscillator (LO), often a PLL synthesizer, adds phase noise and jitter. Perhaps the biggest downside is that the mixing process generates images that can cause interference to the signals being received. Some designs are dual- or triple-conversion types, where two or three downconversions (or an upconversion in some cases) are used to provide image rejection.

Microwave and millimeter-wave signals in the 1- to 300-GHz range are routinely mixed down to an IF in the 70- to 500-MHz range. That's been done primarily due to the speed limitations of available ADCs and fast DSP processors. However, the availability of faster ADCs and DSP/FPGAs is changing that scenario.



1. The classical superheterodyne receiver architecture is still widely used but has some disadvantages at the very high frequencies (e.g., images are a perpetual problem) (a). The direct conversion receiver mixes the incoming signal with a local oscillator of the same frequency, resulting in the direct recovery of the baseband data being transmitted (b). The direct RF sampling receiver architecture is simple and offers multiple advantages at VHF, UHF, and microwave frequencies (c).



2. The TIDA-01442 reference design implements and demonstrates a direct RF-sampling receiver for a radar receiver operating in HF, VHF, UHF, L-, S-, C-, and part of X-band.

Another popular architecture is the direct conversion receiver *(see the figure, b)*. The LO frequency is equal to the incoming signal frequency, and the mixing of the two produces an intermediate frequency of zero. This zero IF architecture downconverts the RF signal directly to baseband. The positive result is less circuitry, lower cost, and complexity, and a more accommodating ADC sampling rate. No images are generated, but the zero IF receiver presents a dc offset problem and LO leakage to the input. Nonetheless, it is widely used.

A receiver architecture that's gaining in popularity is direct RF sampling. RF sampling is the process of directly digitizing the received signal with no downconversion *(see the figure, c)*. Some filtering and RF amplification typically occurs prior to the ADC. For this to work, the ADC must be fast enough to sample the input signal within the Nyquist limits of the device. A sampling rate of at least 2.5 times the highest frequency content is required. A common minimum sampling rate is greater than twice the *bandwidth* of the signal to be received, otherwise known as oversampling. Oversampling offers the benefit of reducing the quantization noise produced by the sampling process. This greatly improves the signal-to-noise ratio (SNR).

BENEFITS OF RF SAMPLING

The simpler receiver signal chain offers some significant benefits. Fewer stages generally mean lower cost and better noise figure. Higher RF gain may be needed to offset the gain of the mixer and any IF amplifier, but the overall noise figure will be improved. An image problem does not exist.

The local-oscillator feedthrough and spur issues are also vanquished. It eliminates a local oscillator, but is essentially replaced by the ADC sampling clock. This architecture typically offers greater flexibility for frequency planning in design, a modern necessity because of the wide range of potential interference sources and targets.

APPLICATIONS

A super-fast ADC potentially opens up a lot of application doors, particularly in RF communications. Some examples are software-defined radios (SDRs) of all types, satellite communications, radar, communications test equipment, forthcoming 5G radios, and digital sampling oscilloscopes.

Fast ADCs can be a major benefit in electronic-warfare (EW) equipment, where the core component is one or more receivers in radars, military radios, and signal-intelligence devices. For example, expect major performance strides to be made in phased-array radars, where each antenna element in the array has its own receiver chain and ADC. Wide-bandwidth receivers let radars detect and process more targets, ultimately providing an advantage over the enemy. Another forthcoming use is large-scale MIMO systems for cellular basestations.

AN EXAMPLE ADC

Typical of the fast new ADCs is Texas Instruments' ADC12DJ3200, a dual-channel 12-bit converter. It offers a sampling rate of 3.2 Gsamples/s per channel or 6.4 Gsamples/s in an interleaved single-channel application. The differential analog inputs are buffered and the −3-dB bandwidth is an impressive 8 GHz. This makes the device suitable for use with L-, S-, and C-band radar, in addition to other applications. Another key feature is a noise floor in the −151.8- to −154.6-dBFS/Hz range. Some other important specs are a signal-to-noise ratio (SNR) of 56.6 dB and a spurious-free dynamic range (SFDR) of 67 dB. The ADC outputs are JESD204B serial data interfaces with a maximum lane rate of 12.8 Gb/s.

Dual digital downconverters (DDCs) are also included

on-chip. Four 32-bit numerical-controlled oscillators allow decimation by 2x, 4x, 8x, or 16x. Decimation removes samples from the ADC output at regular intervals to decrease the sample rate so that the data can be accommodated by the processing circuits.

To evaluate the capabilities of the ADC12DJ3200, Texas Instruments offers the TIDA-01442 reference design that uses the ADC12DJ3200 evaluation module (EVM) *(Fig. 2)*. It demonstrates a direct RF-sampling receiver for a radar receiver operating in HF, VHF, UHF, L-, S-, C-, and part of the X-band. The wide analog input bandwidth and high sampling rate (6.4 Gsamples/s) of the ADC provide multiband coverage with a single or dual ADC. The direct RF-sampling capabilities of the ADC reduce the component count by eliminating several downconversion stages, thereby reducing overall system complexity.

CLOCKING CONSIDERATIONS

High-speed multichannel ADC applications require precise clocking solutions capable of managing channel-to-channel skew to achieve optimal system SNR, SFDR, and ENOB. That makes the clock for the ADC a critical component if the desired benefits are to be achieved. TI offers the solution in the form of its LMX2594, a wideband RF phase-locked-loop (PLL) IC with integrated VCO.

This PLL supports both fractional-N and integer-N modes, and provides an on-chip 32-bit fractional divider that permits fine frequency tuning of clock frequency. This IC offers critical specifications such as −110-dBc/Hz phase noise at 100-kHz offset with a jitter of 45 fs rms at 7.5 GHz. Support is provided for a JESD204B interface and SYDREF.

TI also offers a reference design for this device. Designated the TIDA-01021, the reference design uses the ADC12DJ3200 ADC evaluation module. It supports two high-speed channels on separate boards by using the LMX2594 wideband PLL. Representative performance indicates a board-to-board clock skew of <10 ps with an SNR of 49.6 dB using a 5.25-GHz input signal.

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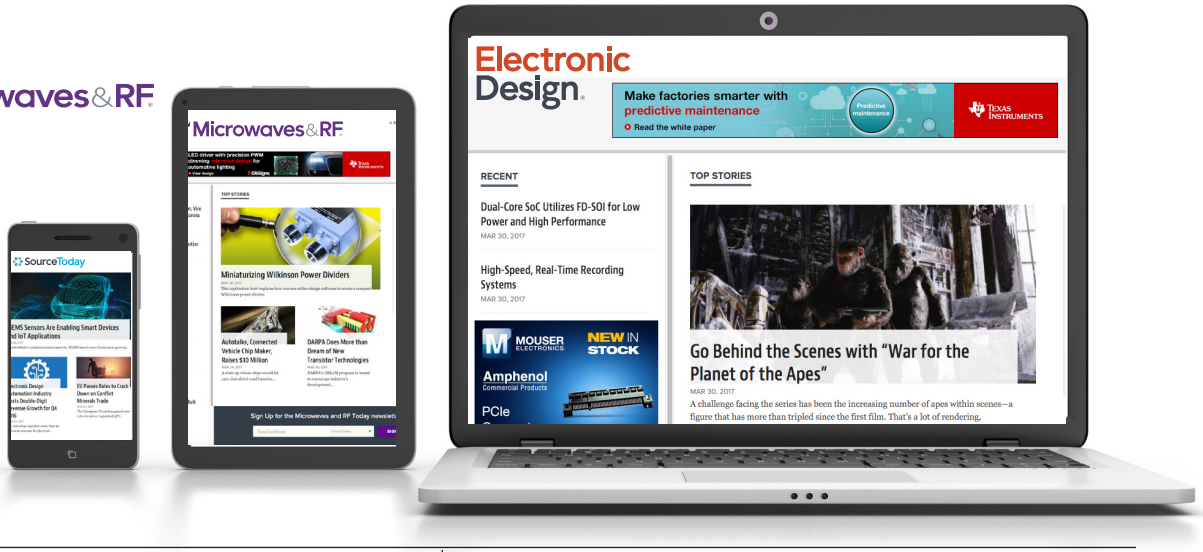

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