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A compendium of articles from *Electronic Design*

SPECIAL REPORT:

# Sensors and AFES





## INTRODUCTION

ANALOG FRONT ENDS (AFE) improve the signals from analog sensors that provide information for electronic systems, especially the internet-of-things for applications like smart factories. AFE design, selection and testing is a challenge because of the tradeoffs designers need to address to meet requirements such as power and stability. This ebook takes a look at many different aspects of sensor and AFE design and integration from using artificial intelligence (AI) to optimize circuit design to AFE design tradeoffs for power applications.



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## CHAPTER 1:

# Bringing High Power Density to Energy Harvesting

STEVE TARANOVICH, Contributing Editor

**A free-standing magnetic field energy harvester (FSMFEH) can provide isolation and effectively power remote sensors in high-voltage grid and busbar applications.**

This article explores innovations in [energy harvesting](#) in conjunction with wireless systems. Free-standing [magnetic field energy harvesters](#) (FSMFEHs) open the door to optimized designs, leading to increased power and density levels. This capability can result in smaller PCB footprints by using a more optimized magnetic force. Designers will discover how FSMFEH technology will forever improve sensor power in the power grid.

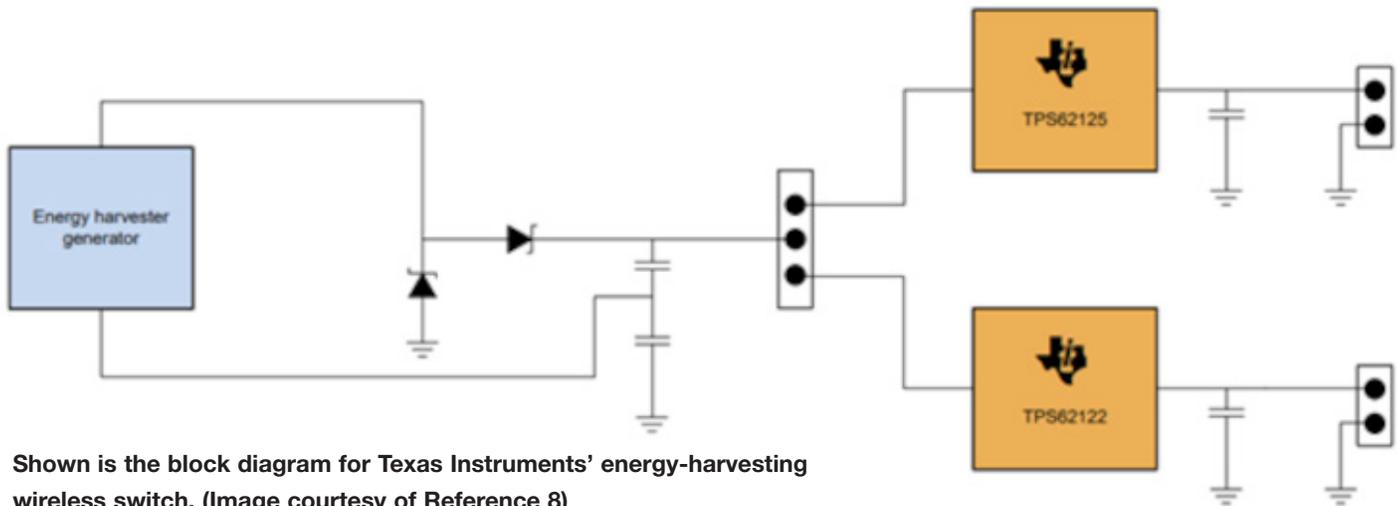
### What is Energy Harvesting?

Energy harvesting is also referred to as energy scavenging, power harvesting, or ambient power. It's the process in which energy is taken from external sources (such as solar energy, thermal energy, wind energy, and kinetic energy, also known as ambient energy). This energy can be stored for use by small, wireless autonomous devices, such as wearable electronics, and wireless sensor networks (WSNs). WSNs can measure environmental conditions such as temperature, sound, pollution levels, humidity and wind.

[Energy harvesters](#) usually provide a very small amount of power for low-energy electronics, utilizing the energy that's present in ambient background. For example, temperature gradients exist from the operation of a combustion engine, and in urban areas, a large amount of electromagnetic energy in the environment is due to radio and television broadcasting.

### Wireless Sensor Networks in Industrial Automation

Wireless sensor communications, deployed within industrial applications, have virtually taken over plant and factory process automation. One of many good reasons to use wireless sensors is the rapid increase of smart devices and the expanding ecosystem of the Internet of Things (IoT) coupled with the unstoppable surge in demand for bandwidth-in-



Shown is the block diagram for Texas Instruments' energy-harvesting wireless switch. (Image courtesy of Reference 8)

tensive applications. Wi-Fi 7 finds itself charged with the formidable challenge of enabling a far more efficient and responsive wireless experience for all users.

WSNs often cost much less than wired solutions, especially in industrial applications. Using wireless sensors enables a far easier means of tracking down a defect/fault within a wireless sensor network. That's because a wired factory floor is frequently burdened with miles of buried wiring.

In addition, wireless is far more flexible than wired options. It allows for faster and easier reconfiguration of a network to meet constantly changing plant needs, which leads to adjusting to newer product varieties and models.

### The Free-Standing Magnetic Field Energy Harvester (FSMFEH)

A magnetic field energy harvester (MFEH) will directly generate electricity via capturing the energy from a magnetic field that's surrounding busbars. An FSMFEH<sup>2,4,8</sup> can be mounted at any position on power busbars that carry current with an alternating magnetic field. The core of an FSMFEH rarely will saturate, leading to a very reliable system.

On the negative side, two issues must be addressed for the FSMFEH:

- The power density of the FSMFEH system is only at a  $\mu\text{W}/\text{cm}^3$  level
- Because the output power of the FSMFEH system is directly related to each parameter of the coil and core, the mathematical model for the output power of the FSMFEH system needs to be derived. The specific effects of every parameter of the core and coil on the output power of the FSMFEH system require a more detailed analysis.

### Improving the FSMFEH System Output Power

The FSMFEH system output power is closely linked to the magnetic flux collection capability of the core.<sup>7</sup> Consequently, the structural design of the core is crucial.

The influence of the coil and core parameters on the output power is quite significant for the FSMFEH. When the FSMFEH gets applied to busbars, the optimization of these coil and core parameters will be critical for the improvement of the output power.

The design of the corresponding coil parameters along with the specific parameters of the core will be difficult to analyze through simulation. This is because the simulation will take a great deal of time to analyze the data and summarize the rules. So, we find that it's

not clear whether the influence of every parameter of the FSMFEH on the output power will be monotonically linear or if there will be an optimal value, and the parametric design basis of FSMFEH is missing.

To solve this issue, an accurate mathematical model output power of FSMFEH will be established and derived below.

This accurate mathematical model of the output power, regarding the core and coil parameters, is based on an H-shaped core. According to this mathematical model, every core and coil parameter may be analyzed in detail. The optimal choice of these parameters is easily obtained; it will be able to provide the theoretical basis for the power improvement of the FSMFEH. Optimizing these parameters greatly improves the power density.

### **Key Contributors for an Accurate FSMFEH Mathematical Model**

The leading technical contribution here establishes and derives, for the first time, an accurate power output mathematical model of the FSMFEH through the quantification of the coil mutual inductance, along with its internal resistance as core and coil parameters.<sup>7</sup> In conformity with the mathematical model, the importance of each parameter, like the length of the core column, the side length of the core column, the number of turns in the coil, and the diameter of the coil wire, on the power density may now be analyzed. This will provide a design basis for optimization of the core and coil parameters.

The second most important contribution here is that the following design rules are discovered through analysis to create a higher power density under the set conditions:

- The thickness of the core lamination should be designed as thin as possible.
- The number of turns should be designed as much as possible.
- The values of the coil diameter and side length of the core column exist as optimal choices.

The third most important contribution is based on the optimization design of every parameter, with an H-shaped core having a volume of  $3.168 \text{ cm}^3$ , and the quantity of turns in its coils are designed. This can lead to a power density of  $4.182 \text{ mW/cm}^3$  with a busbar current of just 100 A.

### **Energy Harvesting for Wireless Switches**

Energy-harvesting switches (**see figure**) are able to transform the mechanical input energy of the switch actuation into electrical energy.<sup>8</sup> This design is suitable when lower installation and maintenance costs, better flexibility, along with system uptime are needed, and when wiring doesn't work in some designs.

Energy-harvesting wireless switches are an excellent a possible solution for explosion-proof applications due to their inherent low-power operating characteristics. This makes it possible to avoid the usage of intrinsically safe barriers, encapsulation, or other expensive protection methods.

### **Energy-Harvesting Modules for Low-Power Designs**

Advanced Linear Devices' EH300/EH301 Series EPAD ENERGY HARVESTING Modules are specifically designed for low power applications,<sup>9</sup> with intermittent duty use and a long storage time for energy-harvesting apps. These modules are completely self-powered and will always be in the active mode.

This device series has excellent onboard features that enable energy accumulation and capture, storage of that energy, power conditioning, and energy management from such energy sources as:

- Solar cells
- PZT piezoelectric ceramic composite elements
- Inductive elements
- Micro thermo-electric generators

### Going Wireless in Energy Harvesters

Improvements in low-power and reliable wireless communications, along with growth in sensor and energy-harvesting technologies, are leading to more practical and more efficient use of wireless communications instead of using a wired infrastructure.

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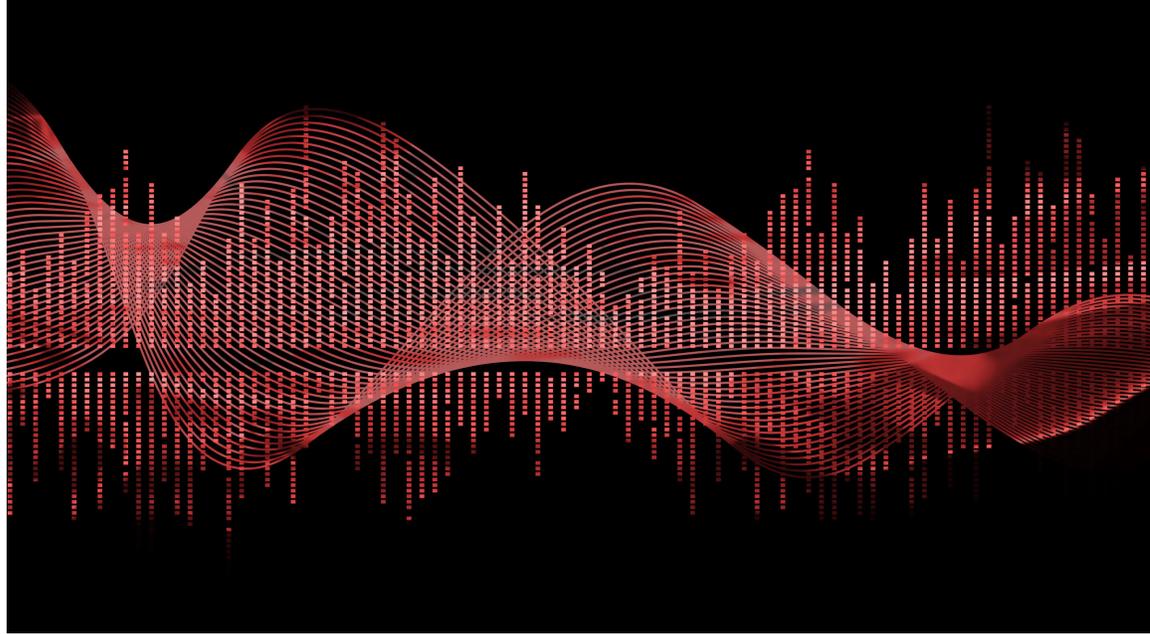


Image credit: O. S., Dreamstime

## CHAPTER 2:

# How RF FDAs Enhance Test Systems with RF Sampling ADCs

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This article discusses how integrating DC-coupling and RF sampling ADCs boosts linearity and bandwidth in RF systems, which impacts overall performance.

Higher data rates in wireless communication systems and the use of narrower pulses in radars to resolve close targets require greater performance and bandwidth requirements in test and measurement instruments. Radio-frequency (RF) test-and-measurement instruments such as high-bandwidth oscilloscopes and RF digitizers use RF sampling analog-to-digital converters (ADCs) that simultaneously digitize signals from DC to multiple gigahertz.

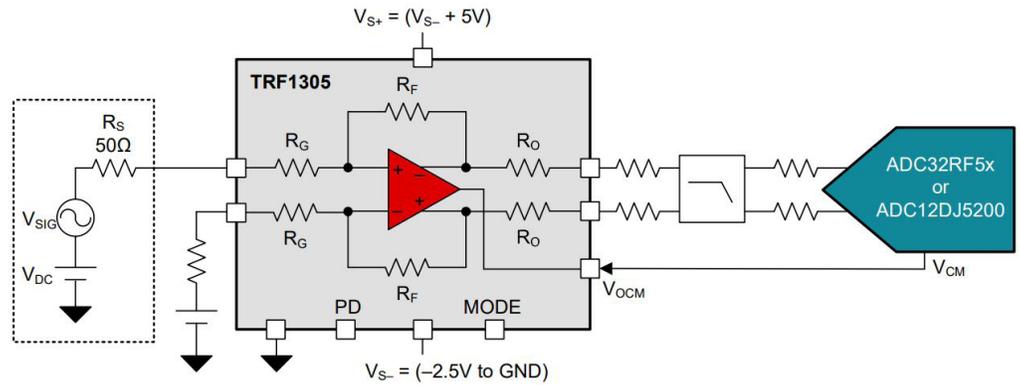
RF sampling ADCs replace mixers followed by narrowband ADCs to reduce system complexity and improve the performance of wideband test and measurement instruments, radars, and wireless transceivers.

Designers typically use a single-ended gain block in cascade with a passive balun to drive RF sampling ADCs. However, there are drawbacks to this approach that limit the achievable performance. In this article, we discuss these drawbacks and illustrate how an RF fully differential amplifier (FDA) can help you maximize the performance of your RF sampling ADCs.

### Introduction to DC-Coupling in RF Sampling ADCs

RF sampling ADCs accept differential inputs to reject common-mode noise and interference and improve second-order distortion. Because of their wide bandwidth, system designers use transformer-based passive baluns to convert single-ended RF signals to differential signals to drive RF sampling ADCs.

However, passive baluns operate from hundreds of kilohertz or tens of megahertz on the low-frequency side based on the bandwidth that they support. Thus, the use of a passive balun to drive RF sampling ADCs in test and measurement instruments limits the lowest



1. This schematic shows a TRF1305 RF FDA DC coupled to an RF sampling ADC. (Source: Texas Instruments)

frequency that can be digitized.

The DC-coupled [TRF1305](#) RF FDA developed by [Texas Instruments](#) performs single-ended to differential conversion with a usable large-signal bandwidth that covers DC to 6.5 GHz, while providing gain. **Figure 1** shows the TRF1305 RF FDA driving an RF sampling ADC in a DC-coupled application. RF sampling ADCs have a narrow input common-mode range, and operation outside this common-mode range degrades ADC performance.

Single or split flexible power supplies, along with output common-mode control, make it easier to match the TRF1305's output common mode to the ADC's input common mode. Such features make this amplifier versatile in DC-coupled RF test and measurement instruments like high-bandwidth oscilloscopes, arbitrary waveform generators and RF digitizers.

### Improving System Linearity in Wideband Systems

Nonlinearity of components in a signal chain affects the detection of small signals in the presence of large interfering signals. Second-order nonlinearity isn't very important in narrowband systems because the nonlinearity created falls outside the frequency band of interest and is generally filtered out.

However, such is not the case with wideband systems. When the input signal bandwidth covers multiple octaves, the second-order nonlinearity of the signal appears in band. For example, consider an RF sampling ADC used with an RF bandwidth of 0.5 to 2 GHz. The second-order nonlinearity of a signal at 0.5 GHz occurs at 1 GHz, which is twice the frequency. But this second-order nonlinearity is less than the 2-GHz maximum frequency of interest and must be minimized since it's not possible to filter it out.

RF sampling ADCs are designed to minimize second-order nonlinearity when their inputs are driven by balanced differential signals. Wideband passive baluns may have poor gain and phase imbalance on their differential output, leading to unbalanced signaling and degradation of the linearity performance of ADCs.<sup>1</sup> And RF gain blocks used to amplify the signal before the passive balun have poor second-order nonlinearity given their single-ended operation.

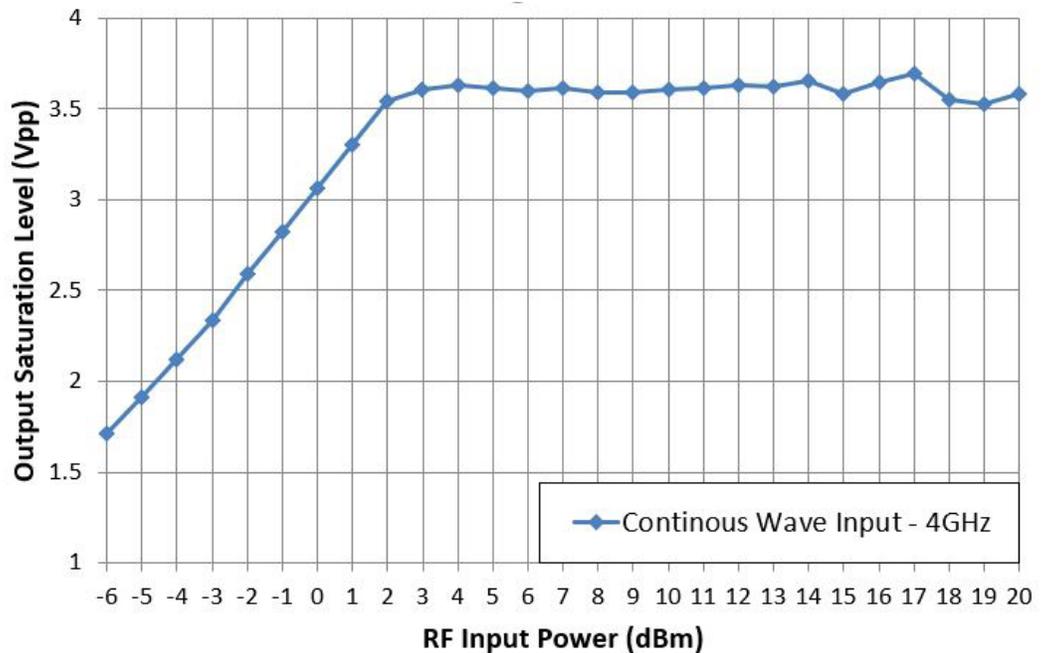
RF FDAs such as the TRF1305 and TRF1208 incorporate feedback techniques that help

achieve improved gain and phase imbalance on the differential outputs. The differential nature of the amplifiers minimizes second-order distortion and enhances linearity of the overall system while providing signal amplification.

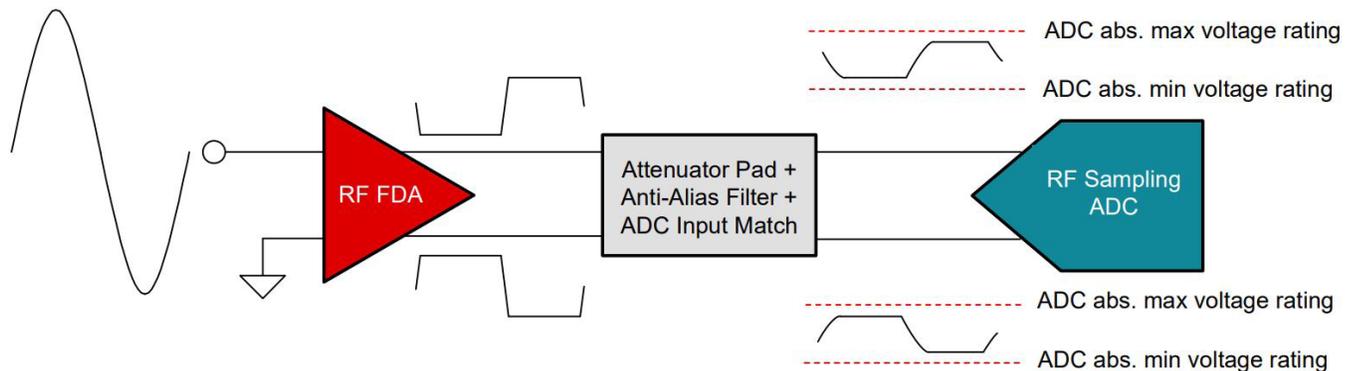
### Protecting ADCs from Damage in High-Power Applications

In many test-and-measurement and aerospace and defense systems, the user inputs are unknown. The RF ADCs at the core of these systems are sensitive to high power levels and overdrive. These ADCs also tend to be high performance and are often one of the most expensive components in the signal chain. That's why it's important to carefully design the signal chain so that the preceding components don't damage the ADC. RF FDAs are designed to be linear when driving RF sampling ADCs to full scale.

Figure 2 shows the output saturation level when the TRF1208 FDA is overloaded with



2. The differential output of the TRF1208 FDA clamps at 3.6 V p-p when overloaded with a continuous wave input at 4 GHz. (Source: Texas Instruments)



3. Shown is the output of RF FDA clips when overloaded, limiting signal power into the ADC. (Source: Texas Instruments)



continuous-wave input at 4 GHz. The TRF1208 has 16 dB of gain and its output saturates to 3.6 V p-p at about 2 dBm of input power into the FDA. Therefore, using RF FDAs to drive the ADCs inherently limits power during an overload caused by output clipping.

Designing an attenuator pad between the FDA and the ADC bounds the voltage swing at the ADC pins (**Fig. 3**). This protects the ADC from damage and simplifies system design considerations while offering more design flexibility.

### Conclusion: Streamlining RF System Designs

The advancement and adoption of RF sampling ADCs simplifies the system architecture of RF test-and-measurement instruments by reducing the number of components and board size. RF FDAs such as the TRF1305 tailored for ADC drive applications further simplify system architectures with single-ended to differential conversion of signals from DC to over 6.5 GHz.

The use of wideband RF FDAs paired with RF sampling ADCs in receive signal chains offers enhanced system performance while lowering component count, board size, and system cost.

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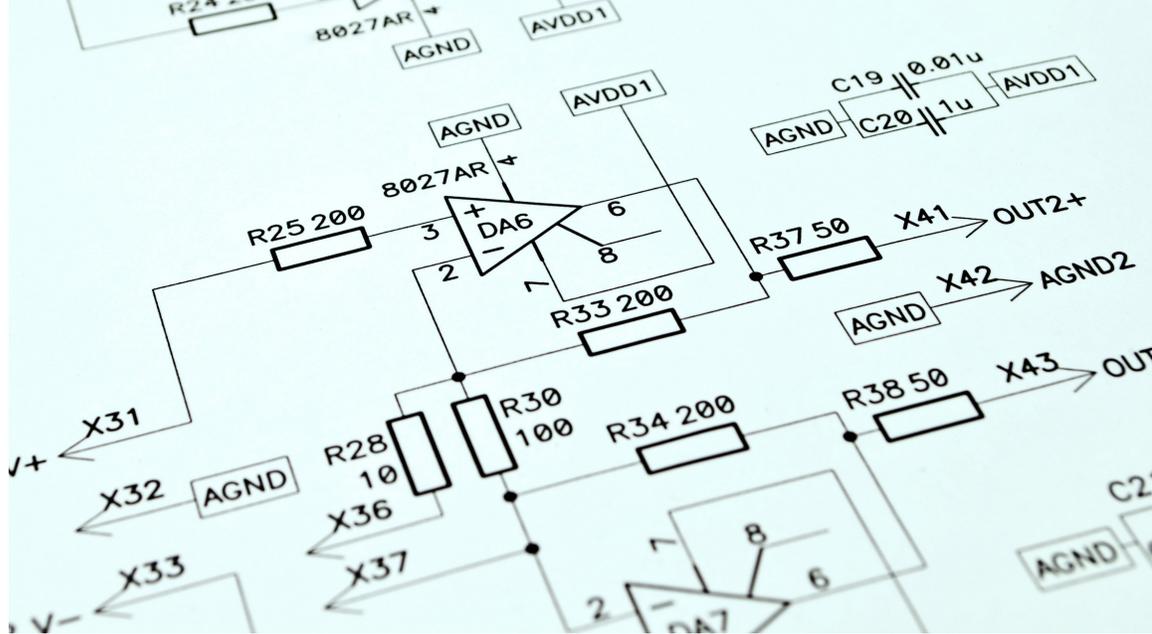


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## CHAPTER 3:

# Tradeoffs in Analog Front-End Architectures for Power Applications

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Microchip Technology

As the semiconductor industry pushes toward higher levels of integration, designers often turn to SoCs or use discrete components as solutions. Another option, though, is to adopt AFE-based implementations, which offer a balance of performance, size, and flexibility.

Sensors provide analog signals that need to be converted to digital values via analog-to-digital converters (ADCs). The challenge is the sensitivity of the ADCs. Typically, an analog front-end (AFE) is needed to make the sensor's signal suitable for conversion.

### What's an Analog Front-End (AFE)?

Fundamentally, any device that performs an analog interface function for a separate digital controller could be called an analog front-end (AFE). Even something as simple as an operational amplifier (op amp) arguably does the job.

In practice, the term is usually reserved for a more integrated device, combining multiple functions or multiple channels to create a comprehensive interface for a specific application. Most contain a combination of one or more programmable gain amplifiers (PGAs), ADCs, and digital interfaces (SPI, I2C, or similar standards).

The amplifiers condition the analog signals, the ADCs transform them to a digital representation, and the interface communicates it to another device on the board. This simple-sounding operation is critical in most electronics, but the silicon implementations behind it can be very difficult.

### Capabilities of AFEs: What Does an AFE Do?

Signal conditioning an application-specific problem, AFEs are often designed with a single application in mind. The details may vary, but the theme is the same: Take the special-

ized analog circuitry required for a function and put it in one integrated device to work with a digital controller. Both the AFE and digital controller can be selected separately based on what's ideal for the circuit requirements.

In one case, the signal chain may start with an antenna, and the AFE may need to band-pass-filter the signal of interest, gain it up, and center it in the range for an analog-to-digital conversion. It would then perform that conversion, serialize the result, and send it by SPI to a digital signal processor (DSP).

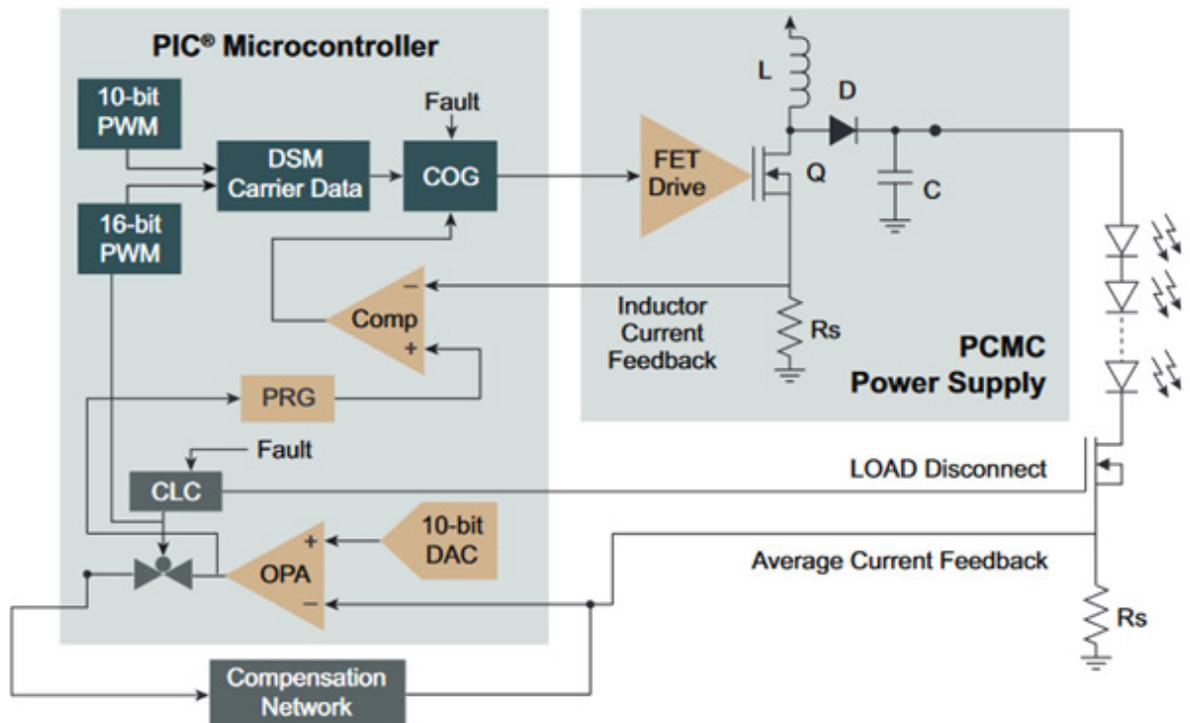
In a different application, the input may be a sensor, with specific voltage and current capabilities that aren't compatible with a typical digital GPIO input. In this case, the AFE could need to accept the sensor output on a low capacitance input or at an unusual voltage range, filter it, scale it, convert it to a digital representation, and relay that information to a microcontroller (MCU) using an I2C interface.

Some applications may require galvanic isolation between the system inputs and the digital processor making the decision, adding a different requirement to the AFE signal chain. In every case, the AFE role is the same: Analog inputs are turned into digital outputs.

### Benefits of AFE-Based Solutions: Why Use an AFE?

The system benefits of this approach aren't necessarily obvious. From a system designer perspective, a single-chip solution will often look like a quicker implementation, and integrated solutions do exist. Some MCUs or digital signal controllers (DSCs) are perfectly capable of being their own analog-front-end using integrated components.

One example is a PIC16F1769, an 8-bit MCU with a 12-channel, 10-bit ADC and two 10-bit digital-to-analog converters (DACs). This device was obviously intended to do its



1. This PIC16F1769 LED drive implementation only needs to be run through a MOSFET driver. No AFE was required, and the external analog discrete components were minimal.

own analog interfacing, and the part can control a switch-mode power supply for an LED drive with all of the analog control signals routed directly into the MCU. Only the power FET drive output signal needs to be run through a MOSFET driver. For this circuit, no AFE was required, and the external analog discrete components were minimal (**Fig. 1**).

However, in many systems, there's no MCU or DSP that can directly handle the analog signals because it would be cost-prohibitive to try to make one. To understand this, think about how these devices are designed and manufactured.

Analog chips are manufactured on analog wafer process technologies. Fabs and foundries create technologies that may not be the smallest or the fastest, but they have both CMOS and bipolar transistors, precise resistors, and capacitors that can be matched to each other. They also possess higher voltage withstand capabilities on specialized transistors, and isolation wells or SOI layers to prevent noise propagation between circuits. These features increase the wafer cost but benefit the analog structures on the chip with improved performance or smaller area requirements.

Such analog characteristics are generally independent of the process lithography, e.g., size. For instance, the area required to create a matched resistor network may depend more on the resistor material available than the smallest drawable line—a larger geometry thin-film resistor may outperform a small lithography polysilicon resistor in accuracy, matching, and silicon area required.

Digital devices, on the other hand, benefit from the smallest possible transistor and have historically scaled with Moore's Law. Each generation outperforms its larger predecessor on a cost of performance basis.

Sometimes, do-it-all wafer technologies can make system-on-chip (SoC) solutions for a specific application, but this approach may suffer from both the high layer count of analog wafer processes and the high per-layer cost of advanced digital nodes. As a result, often the 'best' system solutions are achieved with specialized die, a separate controller, and analog front-end.

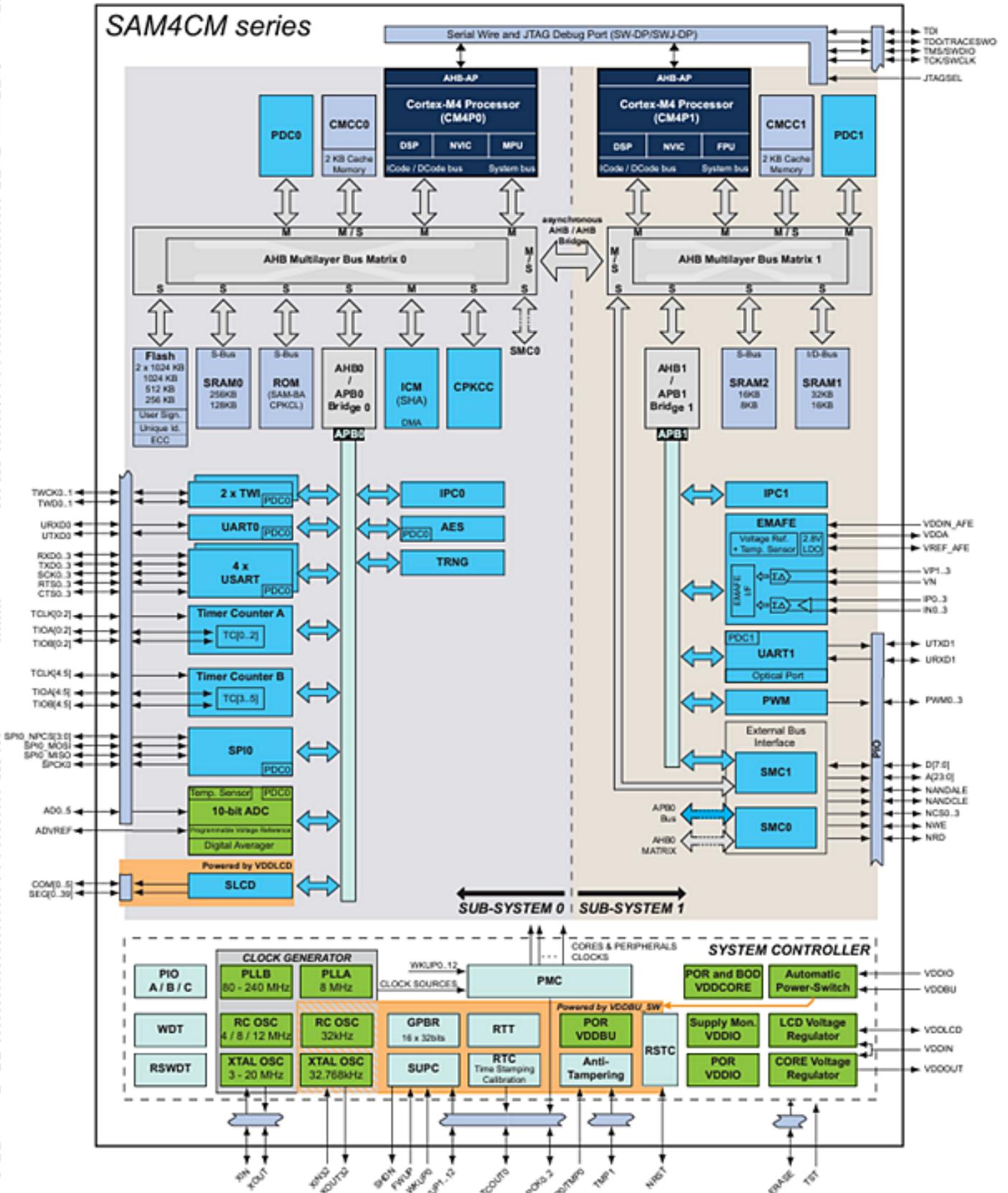
### Tradeoffs in Energy-Meter Designs

Energy-metering applications can illustrate this tradeoff. Solutions for that application are wide-ranging, from integrated SoCs and multichip approaches using AFEs to discrete component implementations.

At the top of the food chain, something like an ATSAM4CM (**Fig. 2**) will include a dual-core Arm Cortex-M4 processor, combined with all of the relevant analog circuitry to produce a class 0.2 utility meter (basically, a 0.2% accurate measurement). It embeds public key cryptography to prevent anyone from hacking the meter, and existing software libraries for that SoC can speed up product development. If the integrated features are all required, this is an excellent solution, and it comes in a 14- × 14-mm package.

However, a well-designed circuit designed using a standalone MCP3910 (analog front-end for metering applications) can produce a class 0.1 meter (0.1% accurate meter). The device sits in a significantly smaller 4- × 4-mm package (**Fig. 3**).

Comparing the specifications on those two devices: the temperature drift on the reference in the AFE chip is lower (9 ppm/°C vs. 10 ppm/°C), the resolution on the ADC is higher (24 bits instead of 20 bits), the dynamic range on the ADC is wider (112 dB vs. 102 dB), and the gain range on the integrated PGAs is wider (up to 32X vs. up to 8X). In every analog-specification, the dedicated AFE chip outperformed the SoC device.



2. The ATSAM4CM Energy Metering SoC includes a dual-core Arm Cortex-M4 processor, combined with all of the relevant analog circuitry, to produce a class 0.2 utility meter.

This obviously isn't a fair comparison, as the standalone AFE would need an additional microcontroller to match the capabilities in the SoC, and the multichip solution has some additional board-level design requirements that the SoC would avoid (like the security implementation). While it may be less accurate, some applications will be completely satisfied with the analog capabilities of the SoC, and the ease provided by the integration may outweigh any performance improvement from a dedicated analog AFE.

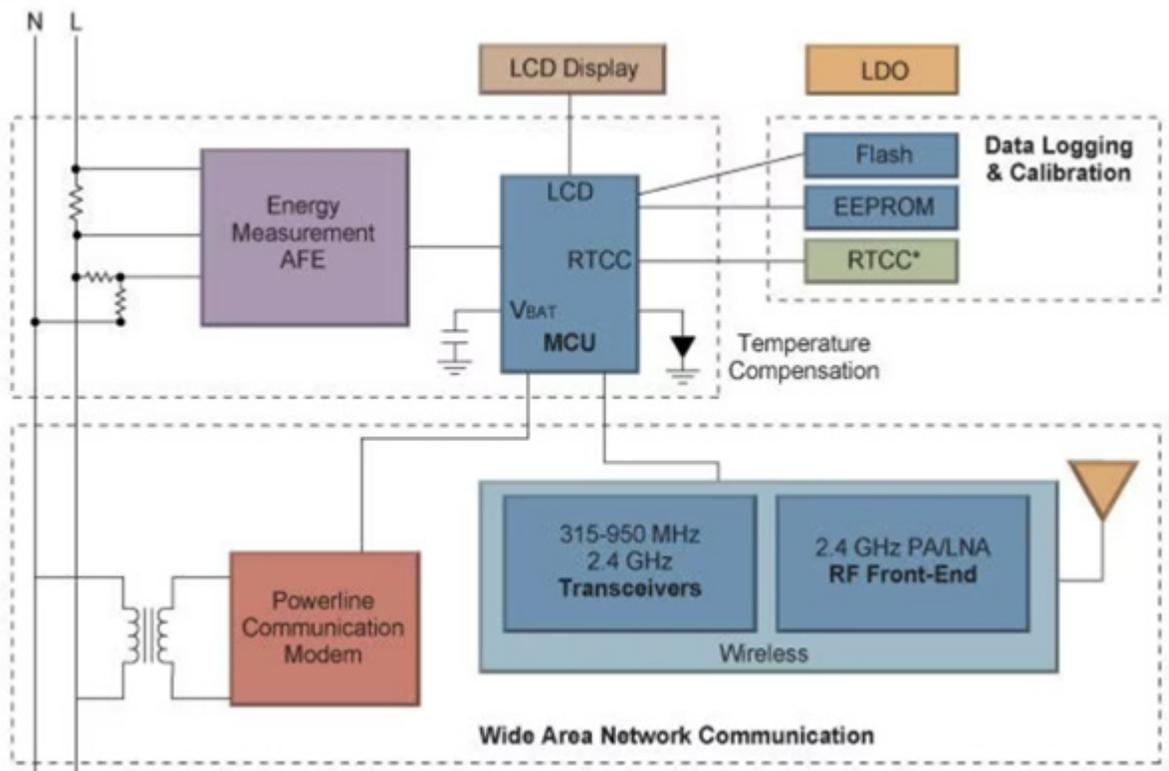
### Discrete Solutions: When There's No AFE

In addition to those integration tradeoffs, many applications benefit from or require completely discrete solutions for signal conditioning. One example is an on-board charging (OBC) circuit. This is a common module in electric vehicles that takes power from a typical residential 120- or 230-V AC outlet and converts that to DC to recharge the battery.

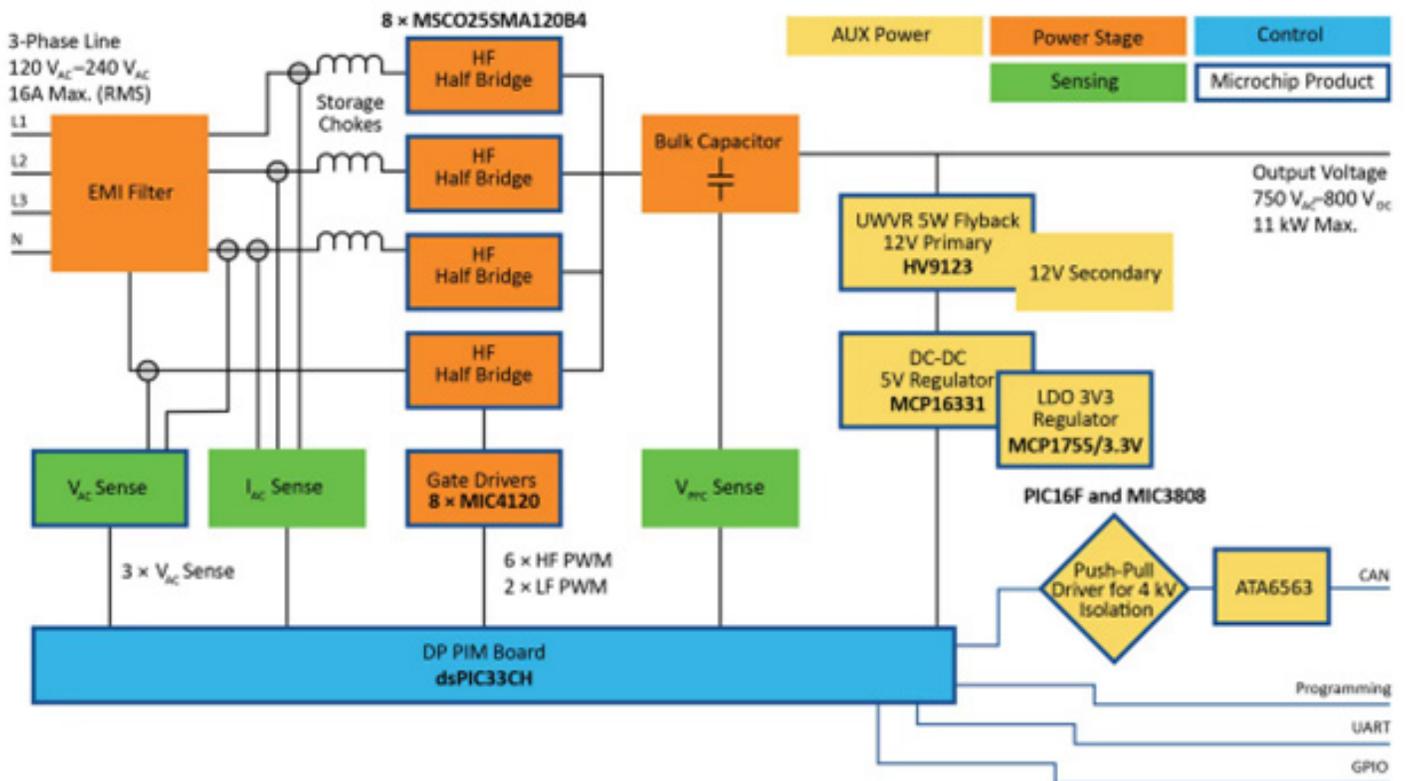
That's separate from, and lower power than, a charge pile (fast-charging station) that provides DC power directly to the battery charging circuit. However, despite being "lower power," a typical module converts more than 10 kW of AC power to a ~800-V DC output. Sometimes, it's even desirable to create OBC modules capable of bidirectional power conversion. Therefore, the battery energy can be used to provide AC power back to the residence, which significantly complicates the power conversion.

The input AC voltage and battery voltage need to be properly isolated from each other, and from everything else as well. Still, the controller requires measurements on these analog signals to provide regulated outputs. The input voltage, output voltage, current, and temperature all must be measured and the sensors need to be galvanically isolated.

In the case of the Microchip reference design (Fig. 4) for this application, there's a



3. The MCP3910 can be used to build a class 0.1 meter (0.1% accurate meter) solution.



4. This block diagram shows the PFC stage for an on-board charging system.

measurement circuit that uses resistive dividers and amplifiers to condition the voltage signal for a DSP, on a physically separate board from the other control circuitry. In addition, opto-isolators are used on the digital communications between the measurement board and the control circuitry.

The current-sense circuit is also in a different place, directly in the current path on the main circuit board. Even the communication out of the module is implemented with an isolated CAN bus. In this application, it would be very difficult to make an AFE to handle such signal conditioning—the voltages are high enough to require physical separation and the isolation capability is difficult to integrate.

### Summary

There's undoubtedly a trend in the semiconductor industry toward increasing levels of integration. For many applications, SoC solutions can be cost-effective or easy to design with. In other cases, system designers may prefer to use discrete components and manage every signal at every stage across the board. In between those two extremes, many applications can apply AFE-based implementations that offer a balance of performance, size, and flexibility.

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## CHAPTER 4:

# Adopting AI-Based Circuit Optimization and Migration

TOBIAS BJERREGAARD, Sr. Director of AI, *Synopsys EDA Group*

Analog designs are challenging, but artificial-intelligence optimizations are improving and speeding up the design process.

The use of artificial intelligence (AI) has gained significant traction in many domains of EDA, and for good reason. AI learns from experience, adapts, and converges on a solution while considering conflicting goals with complex tradeoffs.

Such characteristics make AI highly valuable in tackling many of EDA's hardest challenges, where traditional optimization approaches—either manual or algorithmic—are either sub-optimal, too slow, or fail altogether. AI has the potential to revolutionize the way we design, optimize, and, in particular, migrate analog designs.

### Traditional Optimization Approaches Fall Short

Advances in EDA algorithms have made it possible to scale digital chips to the size of billions of transistors. The scaling of digital design automation builds on abstractions of digital signal levels (1s and 0s) and synchronous operation (discrete time), allowing for a divide-and-conquer approach.

Analog design, on the other hand, doesn't benefit from such abstractions. Individual elements of the design influence each other in complex interactions, making it impossible to optimize one part of the circuit without affecting others. Also, the design metrics are complex, as designers need to consider dozens of metrics, such as supply current, signal-to-noise ratio, jitter, hysteresis, slew rate, CMRR, DC gain, and more across hundreds of process corners.

Due to these inherent complexities, analog design has remained a largely manual process. This puts severe limits on the potential to exploit the multitude of specialized sub-nodes made available from foundries to take advantage of market opportunities. To understand why this is so, let's look at where traditional optimization approaches fall short.

The purpose of optimization is, in essence, to deduce circuit characteristics (e.g., tran-



sistor sizes, layout placement, routing topology, etc.) that fulfill a desired outcome in terms of circuit behavior or performance (i.e., power consumption, noise margin, signal duty cycle, slew rate, etc.).

If the desired outcome can be modeled in a simple manner, with a model that's at least rank order correct, then a traditional optimization algorithm can be created. This has been done successfully in many of the individual steps of the digital implementation flow, leading to a highly automated optimization process.

For example, digital circuit performance can be modeled because circuit behavior is able to be simplified to timing delays—that is, optimization of static timing delays is essentially a linear problem. Analog circuits contain much more complex behavior. They build on nonlinear device models, with no simple proxy function.

Physically accurate models of analog circuits will simulate the exact behavior across all metrics, given the detailed circuit topology and parameters. However, due to the complexity of the underlying models, and of the interactions between the various elements in a design, even the simulation itself is an iteratively converging process. There's no sufficiently accurate, simplified way to emulate the outcome, and no way to move backwards from desired outcome to circuit characteristics.

Hence, analog design optimization has remained a largely manual process, which requires advanced designer expertise, time, and patience. **Figure 1** illustrates how the optimization step is a manually intensive and key step in a traditional analog design flow for migrating an analog design.

### AI-Based Analog Optimization

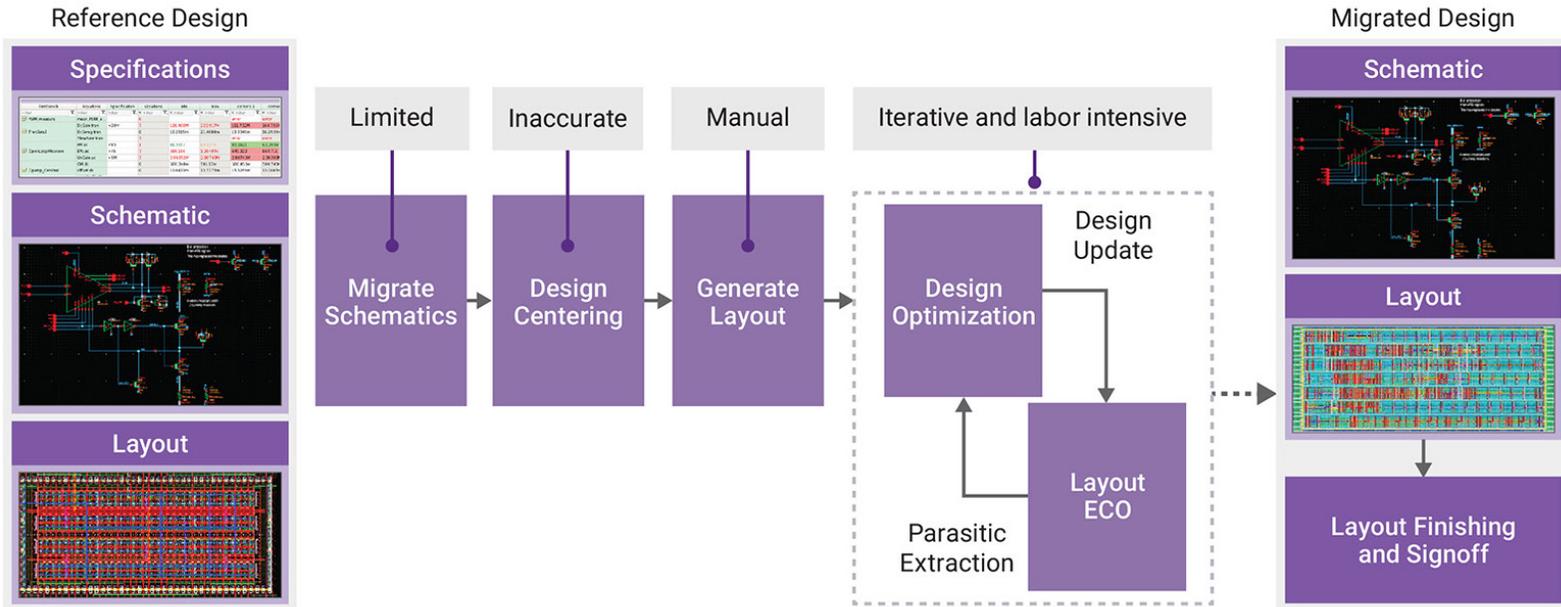
AI-based approaches do well in addressing optimization problems where traditional algorithmic approaches fall short. AI holds the potential to automate the manual loops in the design process. Much like a human designer, AI performs and learns from experiments, combining learnings across each of the experiments to understand and navigate in the solution space. In general terms, this approach is called sample-based optimization.

Sample-based approaches such as grid search, i.e., parameter sweeping, and random search, i.e., Monte Carlo simulation, have traditionally been used to aid designers during the analog design process. However, these approaches don't scale well. The number of samples required for sufficient solution space coverage scales exponentially with design complexity.

More efficient general methods do exist, such as Bayesian Optimization, which is widely used in machine-learning applications. A Bayesian Optimizer builds a probability model of the objective function and uses it to select new sample points with high probability of scoring well in the metric space. As such, it takes learnings from previous samples to build a model that helps select future samples.

An AI-based approach represents an even more focused, intelligently directed way to navigate a large and complex solution space to find sample points that meet the specification. An AI capability can be devised as a sample-based optimization system that dynamically learns about the problem it's tasked to solve.

Such an AI approach can use actual, multi-corner/multi-testbench simulations to drive exploration of complex corner and testbench dependencies. It can dynamically navigate process corners to reduce the number of simulations required, while converging across all corners. Through this process, the AI tool learns from its simulation experiments, using a



**1. The optimization step is a manually intensive and key step in a traditional analog design flow for migrating an analog design.**

live feedback loop to converge toward a solution that meets the specification.

A key advantage of such an AI system is that it doesn't depend on any specific form of the problem it's optimizing. However, unlike less efficient sample-based approaches, it will more efficiently self-adapt to the underlying objective. It also doesn't optimize a proxy, but rather is driven by the actual circuit simulation.

Such a system is possible because the AI system makes informed decisions based on the experiments that it runs, reinforcing its internal perspective of the problem and objectives, which enables fast convergence.

### AI-Based Analog Migration

Macro trends, including the slowing of Moore's Law, manufacturing capacity constraints, and a challenging geo-political climate, are driving the need for newer capabilities to rapidly move designs between process nodes.

To take advantage of market opportunities and be resilient to supply-chain challenges, it's essential for semiconductor companies to maneuver the supply-chain landscape with agility, including porting products from one foundry to another and from one technology node to another. While AI can help accelerate and automate circuit optimization in general, it holds a particular advantage during design migration.

As illustrated in **Figure 1**, the analog design migration process starts with a reference design, with specification, schematic, and layout in a given technology node, and ends with a completed and functional layout in the target node. The challenge of migrating an analog circuit from one node to another differs from general analog circuit design, in that the circuits are based on a prior version of the design.

This is good news for AI: Any design that's been optimized in one context holds valuable learnings which are useful, even if the context, such as the technology node, has changed.

**Figure 2** illustrates an AI-driven, automated design migration process. The first step is to migrate to the target node. Circuit elements and transistors are mapped to equivalent elements in the target node, the specification is adapted to the target, and the design is parametrized with parameters required to adjust the circuit to the specifications.

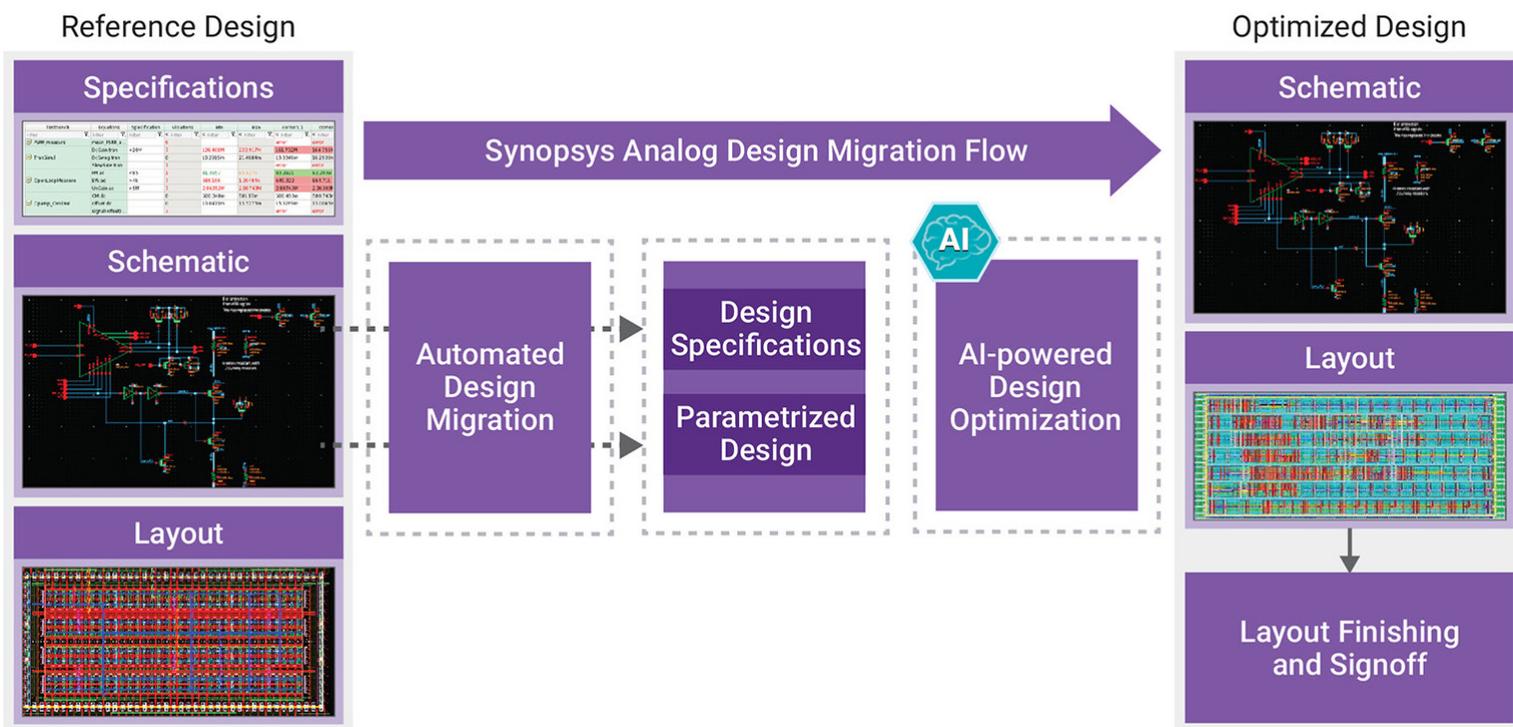
After the basic migration to the target node, the circuit typically isn't functioning according to the specification. The migration process has moved it *off center*. The next step is for the AI-driven optimizer to tune the design parameters to recenter the circuit to meet the specification in the target node.

In addition to recentering a schematic, AI can be used to recenter a circuit as it moves through the design phases, from schematic optimization to layout and ECO. The AI doesn't have to start from scratch at each stage. When adding estimated layout parasitics, the design will be off again and needs recentering, which the AI can do. This can also be handled at the final stages of optimizing with extracted layout parasitics in the optimization loop.

Used properly, AI can significantly accelerate the design process, with fast recentering of a new or incremental design version, the same design in a different technology node, or at later stages of the design process.

### How EDA Algorithms Are Enhanced Using AI Optimization

As advances in EDA algorithms have enabled tremendous scaling of digital design complexity and designer productivity, via optimization algorithms, analog design has remained a largely manual process. This is due to the complexity of the circuit functionality and characteristics together with limitations of traditional optimization approaches. It places



2. This diagram highlights an AI-driven, automated design migration process. The first step is to migrate to the target node.

limitations on the potential for design companies to quickly take advantage of market opportunities.

The use of AI has gained significant traction across EDA. In turn, AI-based optimization has emerged as necessary to address the complexity of the analog design challenge.

As mentioned, AI-based circuit optimization uses actual, multi-corner/multi-testbench simulations to drive exploration of complex corner and testbench dependencies. It learns from its simulation experiments, using a live feedback loop to converge toward solutions. Thus, it's ideally suited to automate the analog circuit design process.

While AI offers clear value during optimization in general, it also enables advanced new use-models. Recentering during node-migration of analog circuits is fast, as the learnings from the prior design implementation can be retained and exploited. Similarly, AI can quickly recenter a design as it moves through the design process, from schematic to layout and ECO.

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Image credit: O. S., Dreamstime

## CHAPTER 5: The Building Blocks of Smart Factories

ALEC MAKDESSIAN, Marketing and Business Development Director, *NXP*

Analog front-ends help boost smart factory efficiency, enabling quick reconfiguration and advanced diagnostics.

In the 21st century, the industry entered its fourth revolution: Industry 4.0. While this is an incredible improvement over previous industrial revolutions, it's still inefficient and fragile.

For example, nearly half of global waste is caused by manufacturing inefficiencies: building the wrong mix of products; building products too early, expiration of products or components; lack of connection between supply chains, manufacturing, and ordering; and even inefficient delivery routes. The [World Economic Forum](#) estimates that up to 15% of trucking miles are currently driven with no load, wasting fuel and time.

Inefficiency isn't the only issue facing the manufacturing industry. Ransomware remains a top threat for all companies. These [attacks have increased 278% since 2019](#), with both costly and deadly consequences.

Global supply chains are bearing the brunt of ransomware attacks, according to a [new report](#) that found manufacturing was the most targeted industry during 2021. For example, when attackers went after the largest pipeline system for refined oil products in the U.S. in 2021, it caused a five-day shutdown and \$4.5 billion ransomware payment, wreaking havoc across the supply chain.

Safety is another concern. Ensuring workers go home safely each night, and want to return to work the next day, is essential for any industry. The [National Safety Council estimates](#) the total cost of work injuries in 2022 to be \$167.0 billion. This figure includes wage and productivity losses of \$50.7 billion, medical expenses of \$37.6 billion, and administrative expenses of \$54.4 billion.

Factory downtime and inefficiencies create additional costs for the manufacturing industry. A [report from Siemens estimates](#) that the cost of downtime for an average large plant is \$129 million per year.

### Key Enablers of Smart and Efficient Factories

It's no surprise that the above challenges are driving the need for more intelligence at the factory. Flexible and smart factories are the path to resiliency and efficiency.

What do we need to build intelligent automation? To enable a smart factory, some of the basic required elements include:

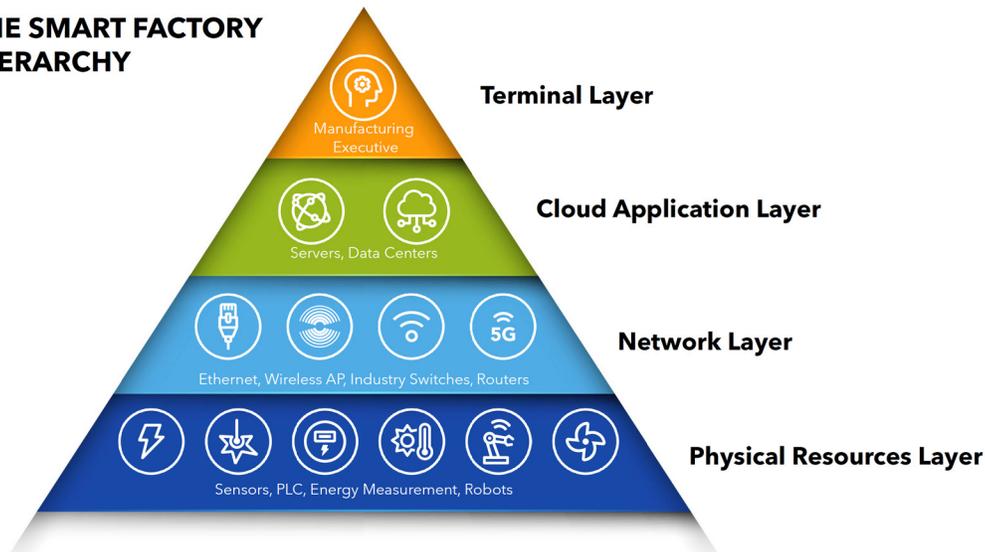
- *Edge computing*: Scalable platforms that can be deployed in different applications that enable real-time analytics and decision-making at the edge, unhampered by network latency and reducing data center and network cost.
- *Machine learning*: Ability to teach machines to take on more complex tasks under changing conditions.
- *End-to-end security*: Required to protect data and assets from external attack, as everything will be connected to allow for collaboration across and between manufacturing sites.
- *Real-time communication*: Separating operational technologies that need real-item control, while enabling larger datasets to be exchanged between machines at the edge.

Though the above features are a necessity, they don't solve the problem of reconfiguring the factory floor every time the market's or the customer's requirements change. To deal with the high level of end-product variance, it's highly desirable that the manufacturing equipment be flexible and configurable.

While flexibility and configurability are achievable at the higher levels of the smart factory hierarchy (Fig. 1), which are already designed to be modular (e.g., servers, routers), it's much more complicated when going to the physical resources layer. There- the factory equipment need to interface with the sensors that collect the real world physical quantities.

For example, one requirement for flexibility is the possibility to accept any sensor output without having to change the analog front-end that converts the analog sensor signal into the digital processing world.

### THE SMART FACTORY HIERARCHY



1. Sensors and analog front-ends provide the base of a smart-factory hierarchy. (Credit: NXP)

In every factory, there are hundreds, if not thousands, of sensors with their associated analog front ends (AFE). Each AFE is optimized to its sensor and could be measuring a voltage, current, or resistance. For instance, an AFE could be measuring a temperature, with its very small millivolt signal, while another AFE could be measuring a  $\pm 25\text{-V}$  large voltage.

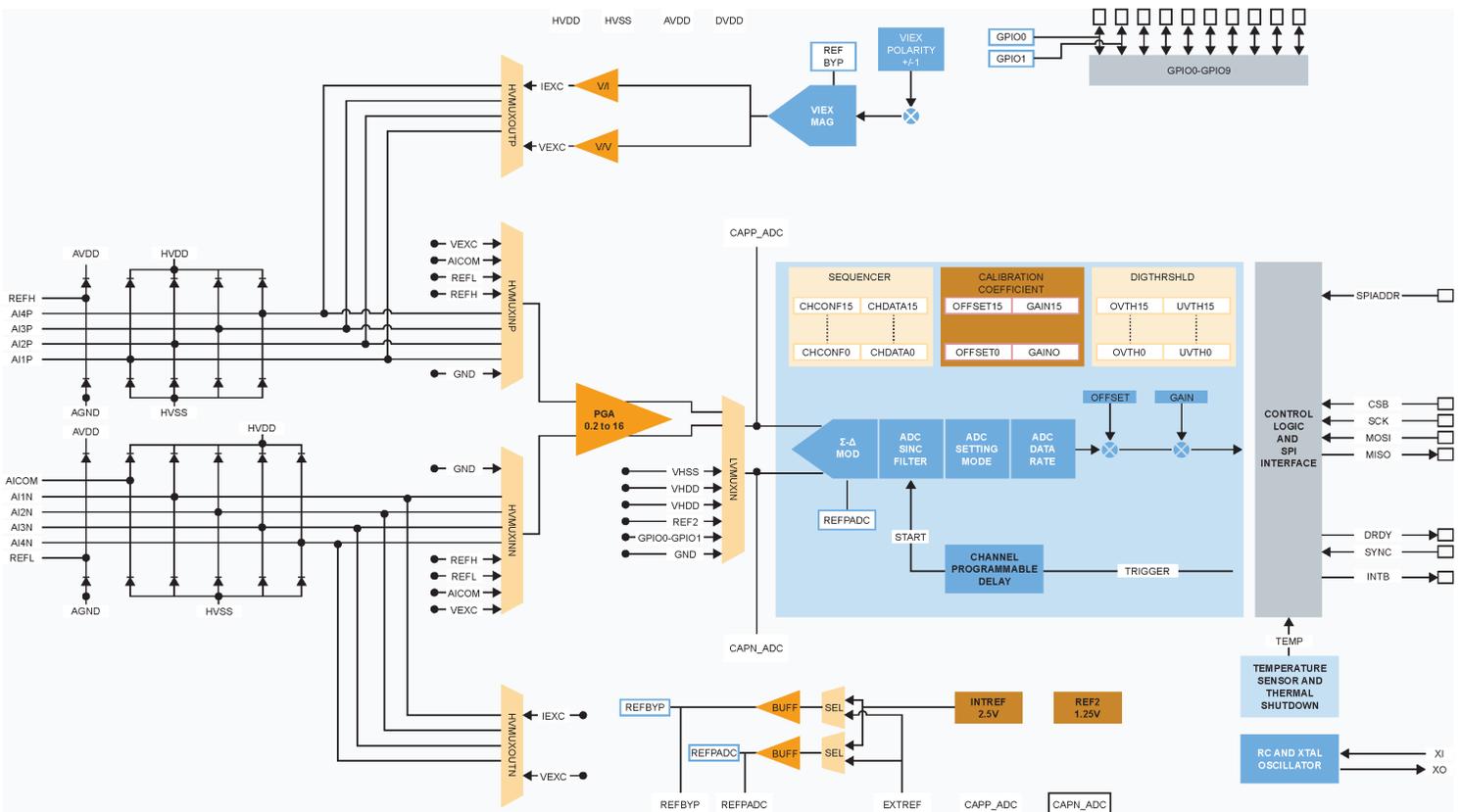
When some of the sensors need to be replaced, say, due to reconfiguring the factory floor, the measurement unit that includes the AFE will also need to be replaced. This means halting the production process while the factory floor is being reconfigured.

The obvious solution to the problem of replacing the AFE for every sensor change is to have software-configurable universal AFEs. Such an AFE can measure a voltage one day and then, if the sensor output is a current, the AFE can be reprogrammed to measure a current.

### Reconfigurable Analog Front-Ends Lead to a Smarter Factory

How does this work in practice? NXP's NAFE family of analog front-ends illustrates one example. With its universal reconfigurable inputs, the AFE can be connected to most available sensors, whether the measurement is a voltage, current, or resistance. In addition, the wide 180-dB dynamic range means that the AFE can measure voltages as low as nanovolts and as high as  $\pm 25\text{ V}$  with the same 0.01% accuracy.

Not only does the AFE measure a variety of sensor signals with 24-bit resolution and 0.01% accuracy, it includes many of the discrete components that are usually on the



2. Shown is a block diagram of NXP's analog front-end. (Credit: NXP)



measurement board. These include high voltage protection, high-voltage fast multiplexers, sensor voltage and current excitation, and low-drift voltage references, in addition to a slew of diagnostic and supply supervisory circuitry for condition monitoring and anomaly detection (**Fig. 2**).

Because the inputs of the NAFE are software-programmable, reconfiguring the factory floor is as simple as reprogramming the measurement unit remotely. This eliminates the time needed to replace the various measurement units, as well as the downtime of the factory.

### **NXP Smart Sensors Support Predictive Maintenance**

The advanced diagnostic features integrated within the NAFE family enable factory operators not only to detect small anomalies, but also to predict and prevent any issues before they occur to avoid unexpected downtime and plan timely maintenance. Some of the advanced diagnostic features include open and short detection, cable and mounting degradation, temperature, power supply, reference clock, input signal anomalies, component aging, reference drift, and others.

Detecting the small anomalies in the presence of large signals is only possible due to the wide dynamic range of the NAFE family, in addition to its high accuracy. These advanced diagnostic features also facilitate the implementation of functional safety.

Predicting failure requires the diagnostics features mentioned above, as well as powerful edge processors with the right algorithms, models, and artificial intelligence. The NAFE family of AFEs, coupled with NXP's crossover MCUs such as the RT1080 family, or MPUs like the i.MX family, address reliability, security, and safety concerns.

### **Conclusion: Smart Manufacturing Efficiency Improved by Flexible AFEs**

Spending on smart manufacturing is expected to grow from \$345 billion in 2021 to more than \$950 billion in 2030, [according to ABI Research](#). Flexible automation offers manufacturers much-needed resilience in an ever-changing environment. The right analog front-end can help increase efficiency by allowing quick reconfiguration of the factory floor based on shifting needs.

On this front, the NAFE family of AFEs featuring fully software configurable inputs allows the measurement of various sensors without hardware changes. Coupled with NXP's processors, security, and functional-safety solutions, the built-in diagnostic features of the NAFE family help facilitate implementation of predictive maintenance, anomaly detection, and failure prediction, in addition to the required safety and security.

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CHAPTER 6:

# What's Next in Remote Monitoring for Digital Healthcare?

ENRICO ALESSI, Research and Development Application Manager and Senior Member of technical staff, and LUCA GUBELLINI, Product Marketing Manager, *STMicroelectronics*

Many of the latest advances in remote monitoring for digital healthcare revolve around non-invasive devices and innovative technologies that reduce patient care costs while improving health outcomes.

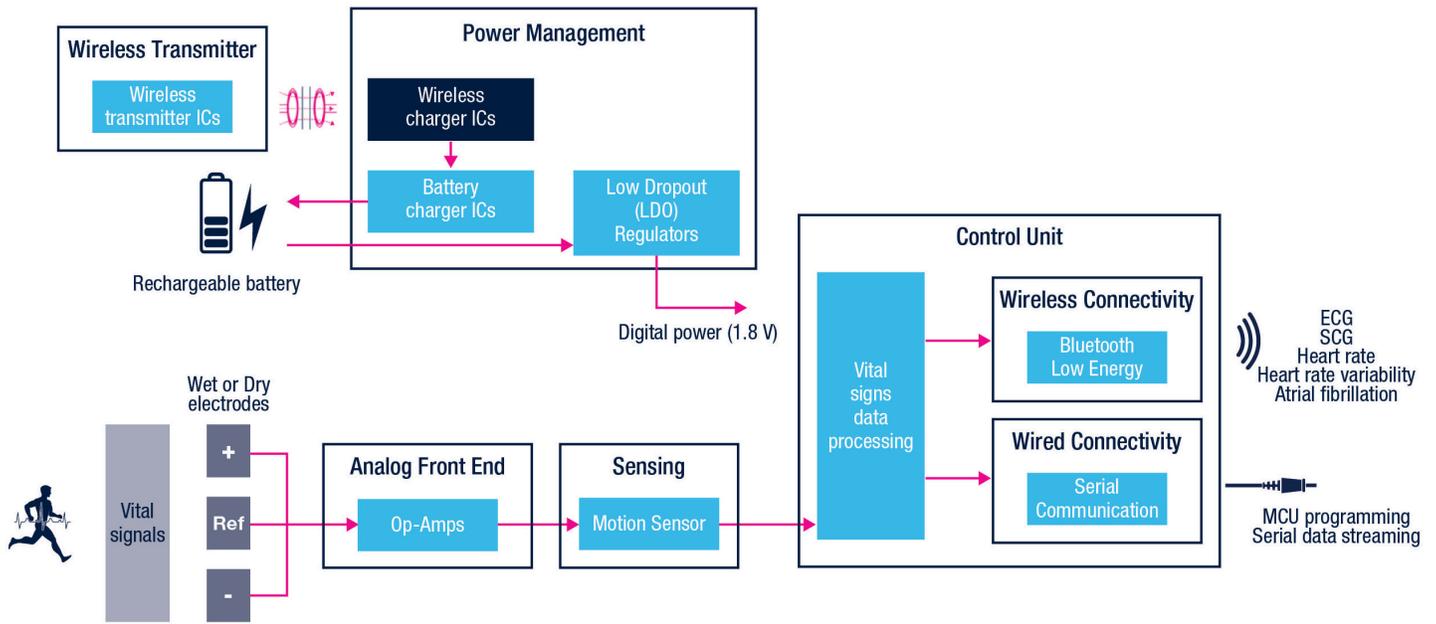
Digital transformation puts the roles of the user and the patient at the center of the healthcare revolution. In digital healthcare, [remote patient monitoring](#) is intended to measure vital signs and other key parameters with non-invasive devices that wirelessly transmit patient information to their healthcare providers or other health stakeholders, while guaranteeing confidentiality (Fig. 1).

Monitoring of vital signs is the process of measuring and tracking important physiological parameters to assess the overall health and wellbeing of an individual. It's paving the way to new opportunities for both wellness/fitness and medical applications, ranging from heart analysis, respiration rate, and oximetry to blood pressure and body temperature.

Nowadays, common practice is to sample periodic snapshots of vital signs by electrocardiograms, glycemia level, oximetry, and blood pressure through examinations using bulky devices. New technologies enable continuous measurement of the different health parameters to infer and predict malfunctions of organs/tissues and metabolic pathways.

The new technologies help healthcare providers detect and manage health conditions remotely. This can save time and costs as well as increase success in predicting and managing emergency cases. Use of medical-grade devices such as cardiac bands, electronic skin patches, and other wearable devices is increasing to accelerate de-hospitalization without compromising patient safety. This benefits national healthcare systems significantly by reducing costs while maintaining the high quality of healthcare services.

Smart watches and wrist bands, smart hearables and headsets, smart rings, fitness trackers, cardiac bands and other wearable personal electronic devices embed new technologies for monitoring and improving user condition and performance. People can



1. This an example of a remote monitoring system based on ST components. (Credit: STMicroelectronics)



2. Smart watches and wrist bands, smart hearables and headsets, smart rings, fitness trackers, cardiac bands, and other wearable personal electronic devices provide information to improve user condition and performance. (Credit: Dreamstime)

become aware of their health status in different contexts, and athletes' performance can improve since the devices provide insights into factors such as heart rate, hydration levels, and muscle activity (Fig. 2).

These wearable products represent a point of convergence of multiple technologies such as materials science, sensing and sensors, biosensors, electronics, microfluidics, and artificial intelligence. They're revolutionizing the consumer healthcare segment by providing real-time monitoring and data collection in a non-invasive and convenient way.

### Technical Challenges in Developing Remote Monitoring Systems

Beyond the well-known technical challenges such as ergonomics, user convenience, patient safety, data security, and connectivity, semiconductor manufacturers should address other critical aspects. Critical points are power consumption and battery life, big-data management, and medical reliability of extracted health indicators.

By addressing these critical points, the development of health monitoring technologies can lead to reliable, user-friendly, and medically approved devices that can play a significant role in preventive healthcare, chronic disease management, and overall health and wellness.

For instance, continuous monitoring of the heart—electrocardiography (ECG)—is a power-consuming process. It produces a large quantity of data that commonly needs to

be managed, processed, and transmitted to the cloud for analysis. Moreover, the extracted data must be transmitted back to the wearable device for advising or alerting the user.

All of these factors represent technical challenges that the semiconductor industry needs to address to ensure devices' on-field efficacy and deliver satisfactory user experiences.

### **Semiconductor and Biosensor Solutions for Healthcare Wearables**

A variety of medical and consumer biosensors is now available to enable the design of wearable devices. Most of these sensors come with analog front-end components to simplify signal conditioning. However, they're usually driven by an external microcontroller to perform data processing and health-indicator extraction. System complexity increases with the incremental use of multiple sensors for deducing more health-related outcomes.

STMicroelectronics (ST) is approaching this market with a new family of biosensors that offer on-chip analog sensing, the vertical analog front-end (vAFE) for ECG and electro-neurography (ENG), a highly sensitive motion sensor (accelerometer and gyroscope) for seismocardiography (SCG), analog-to-digital conversion, features for human-body motion tracking, and embedded digital processing with artificial-intelligence resources that offload the microcontroller.

These unique semiconductor chips combine motion and bio-signal sensing in one device. They create multipurpose platforms where, for instance, ECG signals can be extracted and processed for computing heart rate and heart-rate variability, SCG signals can be extracted for computing the diastolic and systolic period to verify the opening and closure of the aortic and mitral valves (valvular heart-disease detection), and where both ECG and SCG signals can be processed for deriving further health indicators with the great advantage of full time synchronization. In other applications, ENG signals can be used for cognitive-readiness analysis, e.g., for athletes after concussion.

ST's new biosensors, exploiting the integration of motion and bio-signal sensing, can enable novel features such as motion-artifact compensation and context-aware bio-signal measurements. The latter is valuable for increasing battery life since the biosensor understands the user context and activity, and the system can thus adapt the bio-signal acquisition setting and frequency accordingly.

ST MEMS biosensors are helping enable the following applications in the field of health-care wearable devices:

- *Home monitoring:* ECGs and SCGs can be used by individuals to monitor their heart health at home. This can help identify potential problems early on and seek medical attention if necessary.
- *Activity tracking:* ECGs and SCGs can track heart-rate variability (HRV), which is a measure of how well the heart responds to stress. HRV can be used to assess overall health and fitness, as well as to detect early signs of stress and anxiety.
- *Athletic training:* ECGs and SCGs can monitor athletes' heart health during training and competition. This helps prevent overtraining and identifies potential cardiovascular problems. In addition, ENGs can monitor the readiness to play sports again after a trauma event like concussion.
- *Remote patient monitoring and telehealth:* ECGs and SCGs can be used for telehealth appointments, allowing patients to have their ECGs taken remotely by a healthcare provider.



### Future Trends in Remote Monitoring Systems

Recent studies<sup>1,2</sup> have demonstrated how the combination of these two sensing channels, ECG and SCG, can enable the indirect measurement of blood pressure. Further, more connectivity functionalities are able to be added, such as NFC, NB-IoT, and secure connections. On that front, ST offers low-power and high-performance STM32 microcontrollers, high-precision operational amplifiers, and a variety of AC-DC and DC-DC power-management and supply ICs, in addition to wireless-connectivity solutions.

In the semiconductor industry, there's a growing trend toward developing more sophisticated biosensors. These sensors are specialized in detecting and measuring vital human-body analytes, including glucose, sodium, lactate, and calcium. Such advances are significant for healthcare, as they promise to enable continuous monitoring of these analytes in a less invasive way, which is essential for managing various health conditions and improving patient outcomes.

The semiconductor sector is also seeing investment and research efforts directed toward the next generation of low-power sensors that can continuously monitor human body temperature, which is a critical vital sign. The development of such technology is part of a broader initiative to enhance sensor portfolios for health and wellness applications, enabling more comprehensive and non-invasive monitoring of vital signs.

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