Electronic Design

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MIPI DSI-2 Features that Will Make Your Gamers' Heads Spin

Learn about new functionality available with MIPI DSI-2 that makes it the ideal interface for small panel displays.

The MIPI Alliance's MIPI DSI-2 protocol is the most widely adopted interface for small-form-factor display panels such as those found in mobile phones or augmented-reality (AR) headsets. Originally optimized for mobile terminals, this display specification features ultra-low-latency and ultra-low-power operation. In this article, we describe how these features are combined with other high-performance options in the latest MIPI DSI-2 versions.

What is MIPI DSI-2?

The MIPI Display Serial Interface DSI-2 protocol is a packet-based communication protocol between an application processor acting as the source of video and a display panel acting as a peripheral or a sink of the video. The panel typically has a display-driver integrated circuit (DDIC) that receives the MIPI DSI-2 packets and converts them to visible light on the panel *(Fig. 1)*.

Because it's packet-based, the MIPI DSI-2 protocol can sometimes be challenging to implement and debug. However, at the same time, this level of sophistication makes it robust and rich in features.

Key MIPI DSI-2 Features

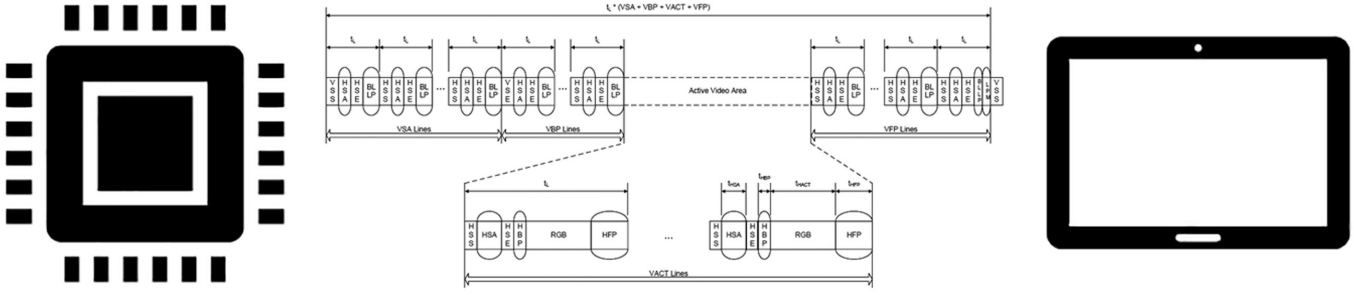
Low Latency

Instant gratification, instant touch responsiveness, or perceptually stable AR interactions: Whatever the case may be, low latency is fundamental to any display technology. Such latency is largely determined by the physical layer (PHY), and the MIPI DSI-2 PHY is, by far, the fastest PHY in the world in terms of latency. It takes just tens of nanoseconds for a MIPI DSI-2 display driver to go from deep sleep (low power) mode to streaming high-resolution content.

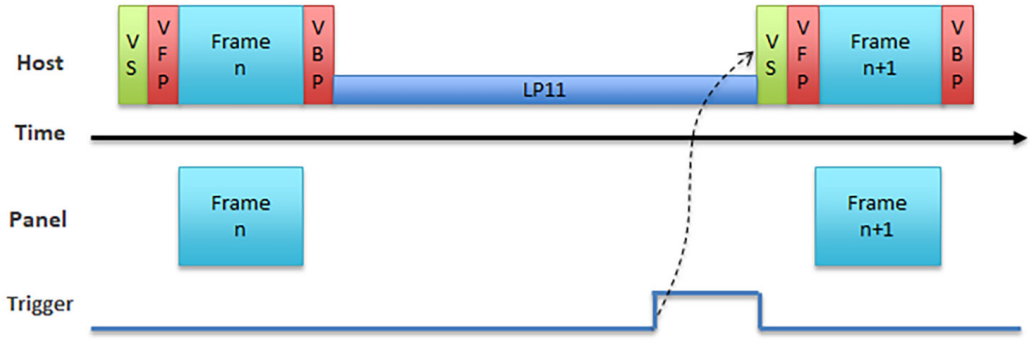
One of the ways that MIPI standards achieve low latency is through the use of synchronous clocking or self-clocking. These solutions offer near-instant clock recovery and adaptation.

Peripheral to Controller Communication—Also Known as Feedback

The best display solutions are those that enable a peripheral device (i.e., a display panel) to notify the controller of events that require a change in behavior. For example, a sensor in the display can tell the controller to change brightness. MIPI DSI-2 enables this feedback through carefully tuned protocol mechanisms. Here, we describe a couple of such mechanisms.



1. MIPI DSI-2 is a packet-based communication protocol. (Source: Introspect Technology)



2. The DSI-2 display can adapt its own refresh rate by sending triggers. (Source: Introspect Technology)

• *Trigger from panel: Adaptive refresh panel (ARP)*

Whether it's for gaming, for saving power, or for optimizing user experience, modern display technologies offer a feature called adaptive refresh rate. Imagine enjoying a still image of the Mona Lisa. You probably want to gaze at the painting for a long time, so it's beneficial for the display screen to slowly refresh its image. On the other hand, if you're participating in an e-sport tournament, then you want your screen to refresh at the fastest rate possible.

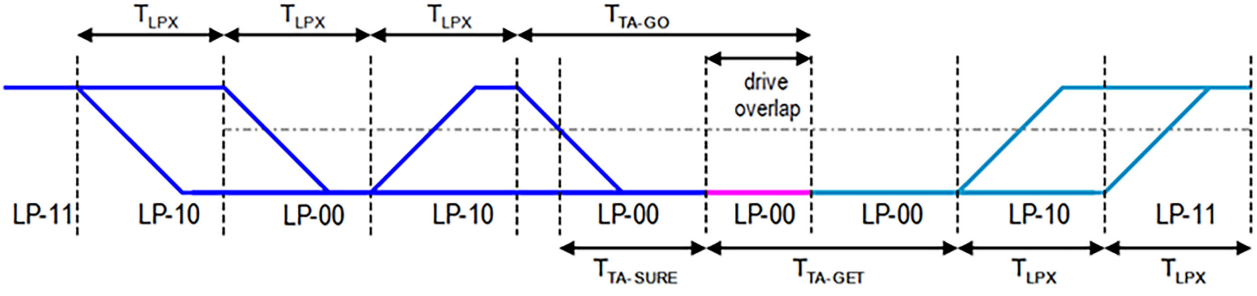
The MIPI DSI-2 protocol implements an adaptive refresh feature, which is probably a little-known fact about the protocol. Interrupts are exchanged in MIPI DSI-2 to enable the feature of dynamically or adaptively changing the display's refresh rate *(Fig. 2)*.

• *Acknowledge and error report: An automatic pass/fail response*

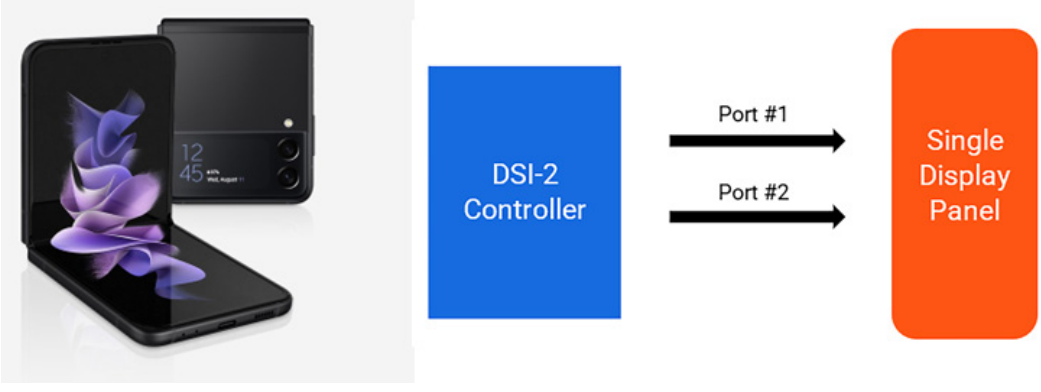
The MIPI DSI-2 protocol enables bidirectional communication through a half-duplex mechanism that doesn't require any additional input/output pins *(Fig. 3)*. Apart from the obvious benefit of saving pins on the application processor, this bidirectional communication includes automatic error reporting, which is an incredibly useful feature for designers of advanced display solutions. The protocol, for example, enables a DDIC to tell the controller if a packet error has occurred or if incomplete video lines were received.

• *General-purpose read operations*

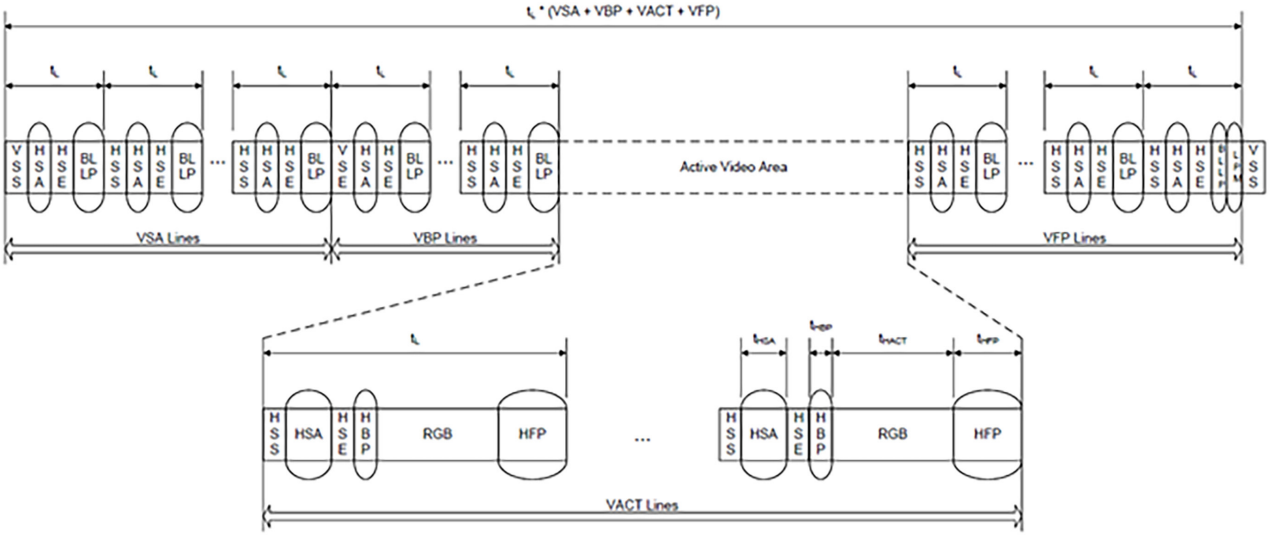
As DDICs become more complex, they contain more and more register settings. The MIPI DSI-2 protocol defines a range of display command sets (DCS) that help designers use a standards-based implementation of these register settings. The controller can simply read a register address from the DDIC and deduce characteristics about its state. This



3. This is an example of a half-duplex communication in MIPI DSI-2. The blue waveforms are driven by the controller, and the cyan waveforms are driven by the display. (Source: Introspect Technology)



4. Folding phones are a good example of multi-link display implementations. (Source: Samsung)



5. The DSI-2 video-mode packet communication mode enables the video timings to be encoded in the protocol, thus saving memory in the DDIC. (Source: Introspect Technology)

standards-based approach to display commands results in a shorter time-to-market for chip designers as well as system integrators.

Sub-Links and Multi-Links

Folding phones are a good illustration of display solutions that require separate communications links to be perfectly synchronized. Referring to *Figure 4*, the physical constraints of folding the phone can result in a separation of the electrical wiring harnesses between the two halves of the folding screen.

Nonetheless, MIPI DSI-2 is able to create a perceptually perfect solution in which the human eye sees the panel as a single continuous panel. It does so by including protocol-level features for dividing a single video stream into two separate PHYs and automatically synchronizing these PHYs together.

Apart from smartphones, AR headsets also require intricate synchronization between two links. If you have two microdisplays projecting images onto your retina, these images better be perfectly synchronized. Otherwise, the headset could present a health and safety hazard.

Video-Mode Timing Generation and Streaming

The MIPI DSI-2 protocol enables the microcontroller to generate all video timing information in the packets being sent, as shown in *Figure 5* with different packet types such as VSS, VSE, HSS, and HSE. These are timing packets that

6. The streaming example shows where the video is constantly being transmitted from the controller to the DDIC. (Source: Mercedes-Benz)

tell the DDIC when to refresh individual lines or complete frames, which is typical in video-mode display solutions.

Most importantly, video-mode features such as that shown in *Figure 5* help reduce the cost of DDIC and panel solutions because they eliminate the need of implementing a frame buffer (memory) inside the DDIC. Frame buffers are physical memories that reside inside the DDIC, and they can be costly in terms of size and overall implementation price.

An example of an application that can benefit from video-mode timing in the controller is a streaming application in, say, a car. Streaming means that the controller is continuously sending video to the display to inform the user of important real-time information such as navigational instructions augmented on top of the real scene while driving *(Fig. 6)*.

Other Features of the MIPI DSI-2 Protocol

The MIPI DSI-2 protocol is replete with other incredible features that make it a truly high-performance protocol for displays of any size. These include flexible packet construction resulting in ultra-high frame rates, compression algorithms based on multiple VESA (Video Electronics Standards Association) standards, and even functional-safety and security extensions for automotive applications.

The MIPI DSI-2 protocol originally started in mobile phones almost 20 years ago. It then moved to the tiniest of displays that project images on the human retina, and now it's finding use in safety-critical automotive applications.

Mohamed Hafed is the Chief Executive Officer of Introspect Technology, a leading manufacturer of innovative test and measurement products for high-speed digital applications. A test industry pioneer, Dr. Hafed has published numerous articles on the topic of analog test and built-in test, and he's a contributing member of the MIPI Alliance, the standards organizing developing the MIPI DSI-2 specifications.