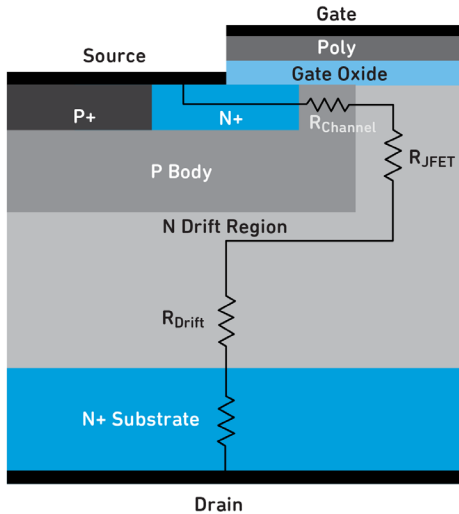
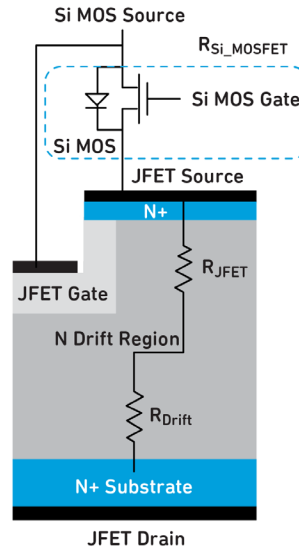


## Power MOSFET



## Qorvo Cascode JFET



2. Cross-section view of a planar SiC MOSFET (left) and a cascode SiC FET (right). The channel resistance of the SiC MOSFET is replaced by a low-voltage silicon MOSFET in a cascode design. (Image credit: Qorvo)

optimize high-frequency switching, silicon MOSFETs and IGBTs have evolved to deliver higher power density and efficiency. But existing approaches can only go so far.

SiC is taking over in [EV powertrains](#) and other power systems where traditional silicon is struggling. As one of several [wide-bandgap semiconductors](#), SiC is changing the tradeoffs of soft switching and giving power designers more incentive to optimize their approach to power-converter circuit design. A key advantage of SiC lies in its ability to handle [high breakdown voltages](#) with very low on-resistance ( $R_{DS(on)}$ ) per unit area ( $R_{DS}A$ ).

These benefits are a result of its wider bandgap and higher carrier mobility compared to traditional silicon. This combination makes it easier to design power electronics that can handle distribution voltages reaching 800 V, which is high enough to prevent excessive resistance losses through power-carrying cables, and above. Higher bus voltages also demand transistor designs that can resist strong voltage surges (*Fig. 1*).

Thanks to the wider bandgap of the underlying semiconductor material, SiC power FETs can use a thinner drift layer that presents less resistance compared to the thicker layers required in traditional silicon devices. The net result is considerably higher conductivity in the on-state.

Using a different transistor design allows you to leverage more of [the power of SiC](#) and approach the theoretical limit of on-state resistance versus breakdown voltage. The [junction field-effect transistor \(JFET\)](#), for instance, is designed to deliver a lower intrinsic on-resistance.

In a standard MOSFET, the carriers must pass across the surface of the p-base, or p-well, region through a resistive inversion channel at the MOS interface before entering the n-type drift region. However, in a JFET, there's no such inversion channel.

SiC-based JFETs have a power transistor with a greater safety margin with respect to breakdown voltage compared

to MOSFET designs, while reducing the on-state resistance per unit area by as much as 50%.

The tradeoff is that, as a normally-on device, the JFET requires a negative voltage to be completely turned off. This is not uncommon in SiC circuitry and may be required for MOSFETs as well to prevent the accidental turn-on of the transistors at temperature extremes where the threshold voltage may fall below nominal levels. However, there's a way to integrate SiC devices into circuitry that delivers both performance and ease of design.

A cascode configuration enables the SiC JFET to operate in series with a low-voltage silicon MOSFET. In the cascode, a gate driver controls the drain-to-source voltage of the Si MOSFET, which indirectly drives the high-voltage SiC JFET. This configuration gives you a gate-control voltage range that's compatible with silicon IGBTs, superjunction MOSFETs, and SiC power FETs. As a result, SiC power FETs can be driven with the same gate drivers that are traditionally used to control silicon MOSFETs and IGBTs.

The silicon MOSFET, which exhibits a reduced operating voltage, or the drain-to-source voltage ( $V_{DS}$ ), contributes less than 10% to the overall on-state resistance of the SiC-based cascode. Coupled with the inherently fast switching speed of SiC, the lower  $R_{DS(on)}$  of the JFET enables very high efficiency even at high switching frequency. To simplify power designs, [Qorvo](#) is supplying its unique cascode configuration in a single package (*Fig. 2*).

### The Benefits of Zero-Voltage Switching (ZVS) Architectures with SiC

The cascode's advantages are most apparent in soft-switching circuit architectures, which are already widely used in power designs based on silicon MOSFETs. The key difference between hard and soft switching is that hard switching has loss contributions from voltage and current overlap during the turn-on and turn-off phases of power transistors.