

# CMOS Analog and Mixed-Signal Circuit Design

Practices and Innovations

Arjuna Marzuki



**CRC Press**

Taylor & Francis Group

Boca Raton London New York

---

CRC Press is an imprint of the  
Taylor & Francis Group, an **informa** business

---

# Contents

Preface.....	xi
Acknowledgments.....	xiii
Author .....	xv
<b>Chapter 1</b> CMOS Analog and Mixed-Signal Circuit Design: An Overview .....	1
1.1 Introduction .....	1
1.2 Notation, Symbol, and Terminology .....	1
1.3 Technology, Circuit Topology, and Methodology .....	2
1.4 Analog and Mixed-Signal Integrated Design Concepts .....	3
1.5 Summary .....	4
<b>Chapter 2</b> Devices: An Overview .....	5
2.1 Introduction .....	5
2.2 The PN Junction .....	5
2.2.1 Fermi Level .....	5
2.2.2 Depletion Layer Capacitance.....	5
2.2.3 Storage Capacitance .....	5
2.3 Photo Devices.....	8
2.4 FETs .....	9
2.4.1 Long Channel Approximation.....	9
2.4.1.1 MOS Structure .....	9
2.4.1.2 MOS with External Bias .....	10
2.4.1.3 MOS Operation .....	13
2.4.1.4 Current-Voltage Characteristics .....	19
2.4.2 MOSFET Scaling .....	28
2.4.2.1 Full Scaling .....	29
2.4.2.2 Constant-Voltage Scaling .....	30
2.4.3 Weak Inversion .....	31
2.4.4 Short-Channel.....	31
2.4.4.1 Carrier Drift Velocity Models .....	32
2.4.4.2 $V_{DSAT}$ .....	33
2.4.4.3 Current-Voltage Equation for Short Channel Transistor .....	34
2.4.5 MOSFET Capacitor.....	35
2.4.5.1 Oxide-Related Capacitance.....	36
2.4.5.2 Junction Capacitance.....	37
2.4.6 MOSFET Transition Frequency .....	40
2.4.7 Noise.....	41
2.4.7.1 Thermal Noise.....	41
2.4.7.2 Flicker Noise .....	42

2.5	Process Fitting Ratio .....	43
2.5.1	150–90 nm Design Transfer .....	44
2.6	MOSFET Parameter Exercise .....	46
2.7	SPICE Example .....	54
2.8	Summary .....	58
	References .....	59
<b>Chapter 3</b>	<b>Amplifiers.....</b>	<b>61</b>
3.1	Introduction .....	61
3.1.1	CMOS Amplifier .....	61
3.2	Input Voltage Range .....	61
3.2.1	Theory .....	61
3.2.2	Example.....	62
3.3	Signal Path of CMOS Operational Amplifier .....	64
3.3.1	Overall Signal Path.....	64
3.3.2	Load.....	65
3.3.3	Cascode Current Source.....	66
3.3.4	Example.....	66
3.4	CMOS Amplifier Parameters .....	70
3.4.1	Input Offset.....	70
3.4.2	Common Mode Input Voltage Range.....	70
3.4.3	Current Consumption .....	70
3.4.4	Common Mode Rejection Ratio (CMRR).....	73
3.4.5	Power Supply Rejection Ratio .....	73
3.4.6	Slew Rate and Settling Time .....	73
3.4.7	DC Gain, $f_c$ , and $f_T$ .....	75
3.4.8	Noise.....	75
3.4.9	Distortion.....	77
3.5	Common Mode Feedback.....	79
3.6	Compensation in Amplifier .....	81
3.6.1	Loop Response .....	81
3.6.2	Pulse Response .....	82
3.7	Wideband Amplifier Technique .....	84
3.7.1	Source and Load.....	84
3.7.2	Stages and Feedback.....	86
3.8	Noises in Amplifiers.....	90
3.8.1	Noise in Circuits.....	90
3.8.2	Noise in Single-Stage Amplifiers .....	92
3.8.3	Noise in Differential Pairs.....	96
3.8.4	Noise in Amplifier with Resistors in the Feedback.....	97
3.8.5	Noise Bandwidth .....	98
3.9	Current Density Design Approach .....	100
3.10	Layout Examples .....	100
3.11	Summary .....	101
	References .....	102

<b>Chapter 4</b>	Low Power Amplifier .....	103
4.1	Introduction .....	103
4.2	Low Voltage CMOS Amplifier.....	103
4.2.1	Body or Bulk Control .....	103
4.2.2	Circuit Technique .....	104
4.3	Subthreshold .....	104
4.4	Current Reuse CMOS Amplifier .....	107
4.5	Other Techniques.....	109
4.5.1	Common-Gate with Gain-Boosting Wideband Differential LNA .....	110
4.6	Spice Example .....	111
4.7	Summary .....	114
	References .....	115
<b>Chapter 5</b>	Voltage Regulator, References and Biasing.....	117
5.1	Introduction .....	117
5.2	Current Sources .....	117
5.3	Self-Biased.....	119
5.4	CTAT and PTAT .....	119
5.5	Bandgap Voltage Reference.....	121
5.5.1	Bandgap Reference .....	121
5.6	Diode-Less Voltage Reference .....	122
5.7	Cascode Current Source .....	124
5.8	Regulated Power Supply .....	125
5.9	Design Example.....	127
5.10	Spice Example .....	129
5.11	Layout Example.....	133
5.12	Summary .....	134
	Problems.....	134
	References .....	134
<b>Chapter 6</b>	Introduction of Advanced Analog Circuit.....	135
6.1	Introduction .....	135
6.2	MOSFET as a Switch .....	135
6.3	Basic Switched Capacitor .....	136
6.3.1	Switching Capacitor Sensitive to Parasitic Capacitances.....	136
6.4	Active Integrator.....	138
6.4.1	Non-inverting Switching Capacitor Non-sensitive to Parasitic Capacitances .....	139
6.4.2	Inverting Active Integrator without a Delay.....	141
6.4.3	Inverting the Switching Capacitor with a Delay, Non-sensitive to Parasitic Capacitances .....	142

6.4.4	SC Behavior in Discrete Points of Time .....	142
6.4.5	Non-inverting Active Integrator with a Delay .....	144
6.5	Sample-and-Hold Amplifier .....	145
6.6	Programmable Gain Amplifier.....	146
6.6.1	Timing .....	149
6.6.2	Common Mode Feedback.....	149
6.6.2.1	AMP and CMFB .....	150
6.7	Chopper Amplifier.....	152
6.8	Dynamic Element Matching Technique.....	153
6.9	Resistor-Less Current Reference .....	155
6.10	Switch Mode Converter .....	156
6.11	SPICE Example .....	158
6.12	Layout Issue.....	164
6.13	Summary .....	164
	References .....	164
<b>Chapter 7</b>	<b>Data Converter .....</b>	<b>167</b>
7.1	Introduction .....	167
7.2	Digital-to-Analog Converter .....	168
7.2.1	Resistor String Topology .....	168
7.2.2	Current Steering .....	169
7.2.3	Hybrid Topology.....	169
7.2.4	DAC Trimming or Calibration .....	173
7.2.5	Glitch .....	175
7.3	Analog-to-Digital Converter .....	176
7.3.1	Slope ADC.....	176
7.3.2	SAR ADC.....	177
7.3.3	Flash ADC.....	178
7.3.4	Pipelined ADC .....	179
7.3.5	Delta Sigma ADC.....	183
7.4	SPICE Example .....	186
7.4.1	DAC Example .....	186
7.4.2	ADC Example .....	186
7.5	Layout Examples .....	190
7.6	Summary .....	193
	References .....	193
<b>Chapter 8</b>	<b>CMOS Color and Image Sensor Circuit Design .....</b>	<b>195</b>
8.1	Introduction .....	195
8.2	Technology and Methodology .....	195
8.2.1	General Comments on Technology or Process for CMOS Image Sensor .....	195
8.2.2	Backside Illumination.....	196

8.2.3	Photo Devices .....	197
8.2.4	Design Methodology .....	197
8.3	CMOS Color Sensor .....	198
8.3.1	Transimpedance Amplifier Topology.....	198
8.3.2	Current to Frequency Topology.....	198
8.3.3	Current Integration Topology .....	199
8.4	CMOS Image Sensor .....	202
8.4.1	CMOS Image Sensor Architecture.....	202
8.4.1.1	Pixel-Level ADC .....	202
8.4.1.2	Column-Level ADC.....	203
8.4.1.3	Chip-Level ADC.....	204
8.4.2	Analog Pixel Sensor .....	205
8.4.3	Digital Pixel Sensor.....	208
8.4.4	Low Power and Low Noise Technique .....	208
8.4.4.1	Low Power Techniques .....	208
8.4.4.2	Low Noise Techniques.....	209
8.5	SPICE Example .....	209
8.6	Layout .....	212
8.7	Summary .....	213
	References .....	213
<b>Chapter 9</b>	<b>Peripheral Circuits.....</b>	<b>217</b>
9.1	Introduction .....	217
9.2	Oscillator .....	217
9.2.1	Ring Oscillator .....	217
9.2.2	RC Oscillator .....	217
9.2.2.1	Ramp Oscillator.....	218
9.3	Non-overlapping Generator .....	220
9.4	Interface Circuitry .....	222
9.4.1	Basic Interface Circuit.....	222
9.4.2	I2C .....	224
9.5	I/O Pad.....	225
9.6	Schmitt Trigger Circuit.....	226
9.7	Voltage Level Shifters .....	227
9.8	Power on Reset .....	229
9.9	ESD Circuit .....	232
9.10	SPICE Example .....	237
9.11	Layout Example.....	244
9.12	Summary .....	246
	References .....	246

<b>Chapter 10</b>	Layout and Packaging .....	247
10.1	Introduction .....	247
10.2	Process.....	247
10.2.1	Antenna Rule.....	247
10.2.2	Electromigration and Metal Density .....	247
10.2.3	Shear Stress .....	249
10.3	Floor Planning.....	250
10.4	ESD and I/O Pad Layout .....	251
10.4.1	Low Parasitic Capacitance Pad .....	251
10.4.2	Seal Ring .....	251
10.5	Analog Circuit Layout Technique .....	253
10.5.1	Matching.....	253
10.5.2	Guard Ring.....	254
10.5.3	Shielding .....	255
10.5.4	Voltage (IR) Drop.....	255
10.5.5	Metal over Implant .....	257
10.5.6	Substrate Tap.....	257
10.6	Digital Circuit Layout Technique .....	257
10.6.1	Power Distribution for Mixed-Signal Design.....	257
10.6.2	Clock Distribution .....	258
10.6.3	Latch-up.....	259
10.7	Packaging .....	260
10.7.1	Die Attach.....	260
10.7.2	Package Type.....	261
10.7.3	Package Parasitic .....	263
10.8	Summary .....	264
	References .....	264
<b>Index</b> .....		265