

SEVENTH EDITION

Microelectronic Circuits

Adel S. Sedra
University of Waterloo

Kenneth C. Smith
University of Toronto

New York Oxford
OXFORD UNIVERSITY PRESS

Oxford University Press is a department of the University of Oxford. It furthers the University's objective of excellence in research, scholarship, and education by publishing worldwide.

Oxford New York
Auckland Cape Town Dar es Salaam Hong Kong Karachi
Kuala Lumpur Madrid Melbourne Mexico City Nairobi
New Delhi Shanghai Taipei Toronto

With offices in
Argentina Austria Brazil Chile Czech Republic France Greece
Guatemala Hungary Italy Japan Poland Portugal Singapore
South Korea Switzerland Thailand Turkey Ukraine Vietnam

Copyright © 2015, 2010, 2004, 1998 by Oxford University Press;
1991, 1987 Holt, Rinehart, and Winston, Inc.; 1982 CBS College Publishing

For titles covered by Section 112 of the US Higher Education
Opportunity Act, please visit www.oup.com/us/he for the
latest information about pricing and alternate formats.

Published in the United States of America by
Oxford University Press
198 Madison Avenue, New York, NY 10016
<http://www.oup.com>

Oxford is a registered trade mark of Oxford University Press.

All rights reserved. No part of this publication may be reproduced,
stored in a retrieval system, or transmitted, in any form or by any means,
electronic, mechanical, photocopying, recording, or otherwise,
without the prior permission of Oxford University Press.

Library of Congress Cataloging-in-Publication Data

Sedra, Adel S., author.
Microelectronic circuits / Adel S. Sedra, University of Waterloo, Kenneth C. Smith,
University of Toronto. — Seventh edition.
pages cm. — (The Oxford series in electrical and computer engineering)
Includes bibliographical references and index.
ISBN 978-0-19-933913-6
1. Electronic circuits. 2. Integrated circuits. I. Smith,
Kenneth C. (Kenneth Carless), author. II. Title.
TK7867.S39 2014
621.3815—dc23

2014033965

Multisim and National Instruments are trademarks of National Instruments. The Sedra/Smith, *Microelectronic Circuits*, Seventh Edition book is a product of Oxford University Press, not National Instruments Corporation or any of its affiliated companies, and Oxford University Press is solely responsible for the Sedra/Smith book and its content. Neither Oxford University Press, the Sedra/Smith book, nor any of the books and other goods and services offered by Oxford University Press are official publications of National Instruments Corporation or any of its affiliated companies, and they are not affiliated with, endorsed by, or sponsored by National Instruments Corporation or any of its affiliated companies.

OrCad and PSpice are trademarks of Cadence Design Systems, Inc. The Sedra/Smith, *Microelectronic Circuits*, Seventh Edition book is a product of Oxford University Press, not Cadence Design Systems, Inc., or any of its affiliated companies, and Oxford University Press is solely responsible for the Sedra/Smith book and its content. Neither Oxford University Press, the Sedra/Smith book, nor any of the books and other goods and services offered by Oxford University Press are official publications of Cadence Design Systems, Inc. or any of its affiliated companies, and they are not affiliated with, endorsed by, or sponsored by Cadence Design Systems, Inc. or any of its affiliated companies.

Cover Photo: This 3D IC system demonstrates the concept of wireless power delivery and communication through multiple layers of CMOS chips. The communication circuits were demonstrated in an IBM 45 nm SOI CMOS process. This technology is designed to serve a multi-Gb/s interconnect between cores spread across several IC layers for high-performance processors.

(Photo Credit: The picture is courtesy of Professor David Wentzloff, Director of the Wireless Integrated Circuits Group at the University of Michigan, and was edited by Muhammad Faisal, Founder of Movellus Circuits Incorporated.)

Printing number: 9 8 7 6 5 4 3 2 1

Printed in the United States of America
on acid-free paper

CONTENTS

Tables xvi
“Expand-Your-Perspective”
Notes xvii
Preface xix

PART I DEVICES AND BASIC CIRCUITS 2

1 Signals and Amplifiers 4

- Introduction 5
- 1.1 Signals 6
- 1.2 Frequency Spectrum of Signals 9
- 1.3 Analog and Digital Signals 12
- 1.4 Amplifiers 15
 - 1.4.1 Signal Amplification 15
 - 1.4.2 Amplifier Circuit Symbol 16
 - 1.4.3 Voltage Gain 17
 - 1.4.4 Power Gain and Current Gain 17
 - 1.4.5 Expressing Gain in Decibels 18
 - 1.4.6 The Amplifier Power Supplies 18
 - 1.4.7 Amplifier Saturation 21
 - 1.4.8 Symbol Convention 22
- 1.5 Circuit Models for Amplifiers 23
 - 1.5.1 Voltage Amplifiers 23
 - 1.5.2 Cascaded Amplifiers 25
 - 1.5.3 Other Amplifier Types 28
 - 1.5.4 Relationships between the Four Amplifier Models 28
 - 1.5.5 Determining R_i and R_o 29
 - 1.5.6 Unilateral Models 29
- 1.6 Frequency Response of Amplifiers 33
 - 1.6.1 Measuring the Amplifier Frequency Response 33
 - 1.6.2 Amplifier Bandwidth 34
 - 1.6.3 Evaluating the Frequency Response of Amplifiers 34
 - 1.6.4 Single-Time-Constant Networks 35
 - 1.6.5 Classification of Amplifiers Based on Frequency Response 41
- Summary 44
- Problems 45

2 Operational Amplifiers 58

- Introduction 59
- 2.1 The Ideal Op Amp 60
 - 2.1.1 The Op-Amp Terminals 60
 - 2.1.2 Function and Characteristics of the Ideal Op Amp 61
 - 2.1.3 Differential and Common-Mode Signals 63
- 2.2 The Inverting Configuration 64
 - 2.2.1 The Closed-Loop Gain 65
 - 2.2.2 Effect of the Finite Open-Loop Gain 67
 - 2.2.3 Input and Output Resistances 68
 - 2.2.4 An Important Application—The Weighted Summer 71
- 2.3 The Noninverting Configuration 73
 - 2.3.1 The Closed-Loop Gain 73
 - 2.3.2 Effect of Finite Open-Loop Gain 75
 - 2.3.3 Input and Output Resistance 75
 - 2.3.4 The Voltage Follower 75
- 2.4 Difference Amplifiers 77
 - 2.4.1 A Single-Op-Amp Difference Amplifier 78
 - 2.4.2 A Superior Circuit—The Instrumentation Amplifier 82
- 2.5 Integrators and Differentiators 87
 - 2.5.1 The Inverting Configuration with General Impedances 87
 - 2.5.2 The Inverting Integrator 89
 - 2.5.3 The Op-Amp Differentiator 94
- 2.6 DC Imperfections 96
 - 2.6.1 Offset Voltage 96
 - 2.6.2 Input Bias and Offset Currents 100
 - 2.6.3 Effect of V_{os} and I_{os} on the Operation of the Inverting Integrator 103
- 2.7 Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance 105
 - 2.7.1 Frequency Dependence of the Open-Loop Gain 105
 - 2.7.2 Frequency Response of Closed-Loop Amplifiers 107

2.8 Large-Signal Operation of Op Amps	110
2.8.1 Output Voltage Saturation	110
2.8.2 Output Current Limits	110
2.8.3 Slew Rate	112
2.8.4 Full-Power Bandwidth	114
Summary	115
Problems	116
3 Semiconductors	134
Introduction	135
3.1 Intrinsic Semiconductors	136
3.2 Doped Semiconductors	139
3.3 Current Flow in Semiconductors	142
3.3.1 Drift Current	142
3.3.2 Diffusion Current	145
3.3.3 Relationship between D and μ	148
3.4 The pn Junction	148
3.4.1 Physical Structure	149
3.4.2 Operation with Open-Circuit Terminals	149
3.5 The pn Junction with an Applied Voltage	155
3.5.1 Qualitative Description of Junction Operation	155
3.5.2 The Current–Voltage Relationship of the Junction	158
3.5.3 Reverse Breakdown	162
3.6 Capacitive Effects in the pn Junction	164
3.6.1 Depletion or Junction Capacitance	164
3.6.2 Diffusion Capacitance	166
Summary	168
Problems	171
4 Diodes	174
Introduction	175
4.1 The Ideal Diode	176
4.1.1 Current–Voltage Characteristic	176
4.1.2 A Simple Application: The Rectifier	177
4.1.3 Another Application: Diode Logic Gates	180
4.2 Terminal Characteristics of Junction Diodes	184
4.2.1 The Forward-Bias Region	184
4.2.2 The Reverse-Bias Region	189
4.2.3 The Breakdown Region	190
4.3 Modeling the Diode Forward Characteristic	190
4.3.1 The Exponential Model	190
4.3.2 Graphical Analysis Using the Exponential Model	191
4.3.3 Iterative Analysis Using the Exponential Model	191
4.3.4 The Need for Rapid Analysis	192
4.3.5 The Constant-Voltage-Drop Model	193
4.3.6 The Ideal-Diode Model	194
4.3.7 The Small-Signal Model	195
4.3.8 Use of the Diode Forward Drop in Voltage Regulation	200
4.4 Operation in the Reverse Breakdown Region—Zener Diodes	202
4.4.1 Specifying and Modeling the Zener Diode	203
4.4.2 Use of the Zener as a Shunt Regulator	204
4.4.3 Temperature Effects	206
4.4.4 A Final Remark	207
4.5 Rectifier Circuits	207
4.5.1 The Half-Wave Rectifier	208
4.5.2 The Full-Wave Rectifier	210
4.5.3 The Bridge Rectifier	212
4.5.4 The Rectifier with a Filter Capacitor—The Peak Rectifier	213
4.5.5 Precision Half-Wave Rectifier—The Superdiode	219
4.6 Limiting and Clamping Circuits	221
4.6.1 Limiter Circuits	221
4.6.2 The Clamped Capacitor or DC Restorer	224
4.6.3 The Voltage Doubler	226
4.7 Special Diode Types	227
4.7.1 The Schottky-Barrier Diode (SBD)	227
4.7.2 Varactors	228
4.7.3 Photodiodes	228
4.7.4 Light-Emitting Diodes (LEDs)	228
Summary	229
Problems	230
5 MOS Field-Effect Transistors (MOSFETs)	246
Introduction	247
5.1 Device Structure and Physical Operation	248
5.1.1 Device Structure	248
5.1.2 Operation with Zero Gate Voltage	250

5.1.3	Creating a Channel for Current Flow	250
5.1.4	Applying a Small v_{DS}	252
5.1.5	Operation as v_{DS} Is Increased	256
5.1.6	Operation for $v_{DS} \geq V_{OV}$: Channel Pinch-Off and Current Saturation	258
5.1.7	The p -Channel MOSFET	261
5.1.8	Complementary MOS or CMOS	263
5.1.9	Operating the MOS Transistor in the Subthreshold Region	264
5.2	Current–Voltage Characteristics	264
5.2.1	Circuit Symbol	264
5.2.2	The i_D – v_{DS} Characteristics	265
5.2.3	The i_D – v_{GS} Characteristic	267
5.2.4	Finite Output Resistance in Saturation	271
5.2.5	Characteristics of the p -Channel MOSFET	274
5.3	MOSFET Circuits at DC	276
5.4	The Body Effect and Other Topics	288
5.4.1	The Role of the Substrate—The Body Effect	288
5.4.2	Temperature Effects	289
5.4.3	Breakdown and Input Protection	289
5.4.4	Velocity Saturation	290
5.4.5	The Depletion-Type MOSFET	290
	Summary	291
	Problems	292

6 Bipolar Junction Transistors (BJTs) 304

	Introduction	305
6.1	Device Structure and Physical Operation	306
6.1.1	Simplified Structure and Modes of Operation	306
6.1.2	Operation of the npn Transistor in the Active Mode	307
6.1.3	Structure of Actual Transistors	315
6.1.4	Operation in the Saturation Mode	316
6.1.5	The pnp Transistor	318
6.2	Current–Voltage Characteristics	320
6.2.1	Circuit Symbols and Conventions	320
6.2.2	Graphical Representation of Transistor Characteristics	325

6.2.3	Dependence of i_C on the Collector Voltage—The Early Effect	326
6.2.4	An Alternative Form of the Common-Emitter Characteristics	329
6.3	BJT Circuits at DC	333
6.4	Transistor Breakdown and Temperature Effects	351
6.4.1	Transistor Breakdown	351
6.4.2	Dependence of β on I_C and Temperature	353
	Summary	354
	Problems	355

7 Transistor Amplifiers 366

	Introduction	367
7.1	Basic Principles	368
7.1.1	The Basis for Amplifier Operation	368
7.1.2	Obtaining a Voltage Amplifier	369
7.1.3	The Voltage-Transfer Characteristic (VTC)	370
7.1.4	Obtaining Linear Amplification by Biasing the Transistor	371
7.1.5	The Small-Signal Voltage Gain	374
7.1.6	Determining the VTC by Graphical Analysis	380
7.1.7	Deciding on a Location for the Bias Point Q	381
7.2	Small-Signal Operation and Models	383
7.2.1	The MOSFET Case	383
7.2.2	The BJT Case	399
7.2.3	Summary Tables	420
7.3	Basic Configurations	423
7.3.1	The Three Basic Configurations	423
7.3.2	Characterizing Amplifiers	424
7.3.3	The Common-Source (CS) and Common-Emitter (CE) Amplifiers	426
7.3.4	The Common-Source (Common-Emitter) Amplifier with a Source (Emitter) Resistance	431
7.3.5	The Common-Gate (CG) and the Common-Base (CB) Amplifiers	439
7.3.6	The Source and Emitter Followers	442
7.3.7	Summary Tables and Comparisons	452

7.3.8 When and How to Include the Transistor Output Resistance r_o	453
7.4 Biasing	454
7.4.1 The MOSFET Case	455
7.4.2 The BJT Case	461
7.5 Discrete-Circuit Amplifiers	467
7.5.1 A Common-Source (CS) Amplifier	467
7.5.2 A Common-Emitter (CE) Amplifier	470
7.5.3 A Common-Emitter Amplifier with an Emitter Resistance R_e	471
7.5.4 A Common-Base (CB) Amplifier	473
7.5.5 An Emitter Follower	475
7.5.6 The Amplifier Frequency Response	477
Summary	479
Problems	480

PART II INTEGRATED-CIRCUIT AMPLIFIERS 506

8 Building Blocks of Integrated-Circuit Amplifiers 508

Introduction	509
8.1 IC Design Philosophy	510
8.2 IC Biasing—Current Sources, Current Mirrors, and Current-Steering Circuits	511
8.2.1 The Basic MOSFET Current Source	512
8.2.2 MOS Current-Steering Circuits	515
8.2.3 BJT Circuits	518
8.2.4 Small-Signal Operation of Current Mirrors	523
8.3 The Basic Gain Cell	525
8.3.1 The CS and CE Amplifiers with Current-Source Loads	525
8.3.2 The Intrinsic Gain	527
8.3.3 Effect of the Output Resistance of the Current-Source Load	530
8.3.4 Increasing the Gain of the Basic Cell	536
8.4 The Common-Gate and Common-Base Amplifiers	537
8.4.1 The CG Circuit	537
8.4.2 Output Resistance of a CS Amplifier with a Source Resistance	541

8.4.3 The Body Effect	542
8.4.4 The CB Circuit	543
8.4.5 Output Resistance of an Emitter-Degenerated CE Amplifier	546
8.5 The Cascode Amplifier	546
8.5.1 Cascoding	546
8.5.2 The MOS Cascode Amplifier	547
8.5.3 Distribution of Voltage Gain in a Cascode Amplifier	552
8.5.4 Double Cascoding	555
8.5.5 The Folded Cascode	555
8.5.6 The BJT Cascode	557
8.6 Current-Mirror Circuits with Improved Performance	559
8.6.1 Cascode MOS Mirrors	559
8.6.2 The Wilson Current Mirror	560
8.6.3 The Wilson MOS Mirror	563
8.6.4 The Widlar Current Source	565
8.7 Some Useful Transistor Pairings	567
8.7.1 The CC–CE, CD–CS, and CD–CE Configurations	567
8.7.2 The Darlington Configuration	571
8.7.3 The CC–CB and CD–CG Configurations	572
Summary	575
Problems	576

9 Differential and Multistage Amplifiers 594

Introduction	595
9.1 The MOS Differential Pair	596
9.1.1 Operation with a Common-Mode Input Voltage	597
9.1.2 Operation with a Differential Input Voltage	601
9.1.3 Large-Signal Operation	602
9.1.4 Small-Signal Operation	607
9.1.5 The Differential Amplifier with Current-Source Loads	611
9.1.6 Cascode Differential Amplifier	612
9.2 The BJT Differential Pair	614
9.2.1 Basic Operation	614
9.2.2 Input Common-Mode Range	616
9.2.3 Large-Signal Operation	617
9.2.4 Small-Signal Operation	620
9.3 Common-Mode Rejection	627
9.3.1 The MOS Case	628
9.3.2 The BJT Case	634
9.4 DC Offset	637

9.4.1 Input Offset Voltage of the MOS Differential Amplifier	637
9.4.2 Input Offset Voltage of the Bipolar Differential Amplifier	640
9.4.3 Input Bias and Offset Currents of the Bipolar Differential Amplifier	643
9.4.4 A Concluding Remark	644
9.5 The Differential Amplifier with a Current-Mirror Load	644
9.5.1 Differential to Single-Ended Conversion	644
9.5.2 The Current-Mirror-Loaded MOS Differential Pair	645
9.5.3 Differential Gain of the Current-Mirror-Loaded MOS Pair	647
9.5.4 The Bipolar Differential Pair with a Current-Mirror Load	651
9.5.5 Common-Mode Gain and CMRR	655
9.6 Multistage Amplifiers	659
9.6.1 A Two-Stage CMOS Op Amp	659
9.6.2 A Bipolar Op Amp	664
Summary	672
Problems	674
10 Frequency Response	696
Introduction	697
10.1 Low-Frequency Response of Discrete-Circuit Common-Source and Common-Emitter Amplifiers	699
10.1.1 The CS Amplifier	699
10.1.2 The Method of Short-Circuit Time-Constants	707
10.1.3 The CE Amplifier	707
10.2 Internal Capacitive Effects and the High-Frequency Model of the MOSFET and the BJT	711
10.2.1 The MOSFET	711
10.2.2 The BJT	717
10.3 High-Frequency Response of the CS and CE Amplifiers	722
10.3.1 The Common-Source Amplifier	722
10.3.2 The Common-Emitter Amplifier	728
10.3.3 Miller's Theorem	732
10.3.4 Frequency Response of the CS Amplifier When R_{sig} Is Low	735
10.4 Useful Tools for the Analysis of the High-Frequency Response of Amplifiers	739
10.4.1 The High-Frequency Gain Function	739
10.4.2 Determining the 3-dB Frequency f_H	740
10.4.3 The Method of Open-Circuit Time Constants	743
10.4.4 Application of the Method of Open-Circuit Time Constants to the CS Amplifier	744
10.4.5 Application of the Method of Open-Circuit Time Constants to the CE Amplifier	748
10.5 High-Frequency Response of the Common-Gate and Cascode Amplifiers	748
10.5.1 High-Frequency Response of the CG Amplifier	748
10.5.2 High-Frequency Response of the MOS Cascode Amplifier	754
10.5.3 High-Frequency Response of the Bipolar Cascode Amplifier	759
10.6 High-Frequency Response of the Source and Emitter Followers	760
10.6.1 The Source-Follower Case	761
10.6.2 The Emitter-Follower Case	767
10.7 High-Frequency Response of Differential Amplifiers	768
10.7.1 Analysis of the Resistively Loaded MOS Amplifier	768
10.7.2 Analysis of the Current-Mirror-Loaded MOS Amplifier	772
10.8 Other Wideband Amplifier Configurations	778
10.8.1 Obtaining Wideband Amplification by Source and Emitter Degeneration	778
10.8.2 The CD-CS, CC-CE, and CD-CE Configurations	781
10.8.3 The CC-CB and CD-CG Configurations	786
Summary	788
Problems	789
11 Feedback	806
Introduction	807
11.1 The General Feedback Structure	808
11.1.1 Signal-Flow Diagram	808
11.1.2 The Closed-Loop Gain	809

- 11.1.3 The Loop Gain **810**
 - 11.1.4 Summary **814**
 - 11.2 Some Properties of Negative Feedback **815**
 - 11.2.1 Gain Desensitivity **815**
 - 11.2.2 Bandwidth Extension **816**
 - 11.2.3 Interference Reduction **817**
 - 11.2.4 Reduction in Nonlinear Distortion **819**
 - 11.3 The Feedback Voltage Amplifier **820**
 - 11.3.1 The Series–Shunt Feedback Topology **820**
 - 11.3.2 Examples of Series–Shunt Feedback Amplifiers **821**
 - 11.3.3 Analysis of the Feedback Voltage Amplifier Utilizing the Loop Gain **823**
 - 11.3.4 A Final Remark **828**
 - 11.4 Systematic Analysis of Feedback Voltage Amplifiers **828**
 - 11.4.1 The Ideal Case **829**
 - 11.4.2 The Practical Case **831**
 - 11.5 Other Feedback Amplifier Types **840**
 - 11.5.1 Basic Principles **840**
 - 11.5.2 The Feedback Transconductance Amplifier (Series–Series) **844**
 - 11.5.3 The Feedback Transresistance Amplifier (Shunt–Shunt) **855**
 - 11.5.4 The Feedback Current Amplifier (Shunt–Series) **865**
 - 11.6 Summary of the Feedback Analysis Method **871**
 - 11.7 The Stability Problem **871**
 - 11.7.1 Transfer Function of the Feedback Amplifier **871**
 - 11.7.2 The Nyquist Plot **873**
 - 11.8 Effect of Feedback on the Amplifier Poles **875**
 - 11.8.1 Stability and Pole Location **875**
 - 11.8.2 Poles of the Feedback Amplifier **876**
 - 11.8.3 Amplifier with a Single-Pole Response **877**
 - 11.8.4 Amplifier with a Two-Pole Response **878**
 - 11.8.5 Amplifiers with Three or More Poles **883**
 - 11.9 Stability Study Using Bode Plots **885**
 - 11.9.1 Gain and Phase Margins **885**
 - 11.9.2 Effect of Phase Margin on Closed-Loop Response **886**
 - 11.9.3 An Alternative Approach for Investigating Stability **887**
 - 11.10 Frequency Compensation **889**
 - 11.10.1 Theory **889**
 - 11.10.2 Implementation **891**
 - 11.10.3 Miller Compensation and Pole Splitting **892**
 - Summary **895**
 - Problems **896**
- ## 12 Output Stages and Power Amplifiers **920**
- Introduction **921**
 - 12.1 Classification of Output Stages **922**
 - 12.2 Class A Output Stage **923**
 - 12.2.1 Transfer Characteristic **924**
 - 12.2.2 Signal Waveforms **925**
 - 12.2.3 Power Dissipation **926**
 - 12.2.4 Power-Conversion Efficiency **928**
 - 12.3 Class B Output Stage **929**
 - 12.3.1 Circuit Operation **929**
 - 12.3.2 Transfer Characteristic **929**
 - 12.3.3 Power-Conversion Efficiency **930**
 - 12.3.4 Power Dissipation **931**
 - 12.3.5 Reducing Crossover Distortion **933**
 - 12.3.6 Single-Supply Operation **934**
 - 12.4 Class AB Output Stage **935**
 - 12.4.1 Circuit Operation **935**
 - 12.4.2 Output Resistance **937**
 - 12.5 Biasing the Class AB Circuit **940**
 - 12.5.1 Biasing Using Diodes **940**
 - 12.5.2 Biasing Using the V_{BE} Multiplier **942**
 - 12.6 Variations on the Class AB Configuration **945**
 - 12.6.1 Use of Input Emitter Followers **945**
 - 12.6.2 Use of Compound Devices **946**
 - 12.6.3 Short-Circuit Protection **949**
 - 12.6.4 Thermal Shutdown **950**
 - 12.7 CMOS Class AB Output Stages **950**
 - 12.7.1 The Classical Configuration **950**
 - 12.7.2 An Alternative Circuit Utilizing Common-Source Transistors **953**
 - 12.8 IC Power Amplifiers **961**
 - 12.8.1 A Fixed-Gain IC Power Amplifier **962**

- 12.8.2 The Bridge Amplifier **966**
- 12.9 Class D Power Amplifiers **967**
- 12.10 Power Transistors **971**
 - 12.10.1 Packages and Heat Sinks **971**
 - 12.10.2 Power BJTs **972**
 - 12.10.3 Power MOSFETs **974**
 - 12.10.4 Thermal Considerations **976**
- Summary **982**
- Problems **983**

13 Operational-Amplifier Circuits **994**

- Introduction **995**
- 13.1 The Two-Stage CMOS Op Amp **996**
 - 13.1.1 The Circuit **997**
 - 13.1.2 Input Common-Mode Range and Output Swing **998**
 - 13.1.3 DC Voltage Gain **999**
 - 13.1.4 Common-Mode Rejection Ratio (CMRR) **1001**
 - 13.1.5 Frequency Response **1002**
 - 13.1.6 Slew Rate **1007**
 - 13.1.7 Power-Supply Rejection Ratio (PSRR) **1008**
 - 13.1.8 Design Trade-Offs **1009**
 - 13.1.9 A Bias Circuit for the Two-Stage CMOS Op Amp **1010**
- 13.2 The Folded-Cascode CMOS Op Amp **1016**
 - 13.2.1 The Circuit **1016**
 - 13.2.2 Input Common-Mode Range and Output Swing **1018**
 - 13.2.3 Voltage Gain **1020**
 - 13.2.4 Frequency Response **1021**
 - 13.2.5 Slew Rate **1022**
 - 13.2.6 Increasing the Input Common-Mode Range: Rail-to-Rail Input Operation **1024**
 - 13.2.7 Increasing the Output Voltage Range: The Wide-Swing Current Mirror **1026**
- 13.3 The 741 BJT Op Amp **1028**
 - 13.3.1 The 741 Circuit **1028**
 - 13.3.2 DC Analysis **1032**
 - 13.3.3 Small-Signal Analysis **1038**
 - 13.3.4 Frequency Response **1051**
 - 13.3.5 Slew Rate **1053**
- 13.4 Modern Techniques for the Design of BJT Op Amps **1054**

- 13.4.1 Special Performance Requirements **1054**
- 13.4.2 Bias Design **1056**
- 13.4.3 Design of the Input Stage to Obtain Rail-to-Rail V_{ICM} **1058**
- 13.4.4 Common-Mode Feedback to Control the DC Voltage at the Output of the Input Stage **1064**
- 13.4.5 Output-Stage Design for Near Rail-to-Rail Output Swing **1069**
- 13.4.6 Concluding Remark **1073**
- Summary **1073**
- Problems **1074**

PART III DIGITAL INTEGRATED CIRCUITS **1086**

14 CMOS Digital Logic Circuits **1088**

- Introduction **1089**
- 14.1 CMOS Logic-Gate Circuits **1090**
 - 14.1.1 Switch-Level Transistor Model **1090**
 - 14.1.2 The CMOS Inverter **1091**
 - 14.1.3 General Structure of CMOS Logic **1091**
 - 14.1.4 The Two-Input NOR Gate **1094**
 - 14.1.5 The Two-Input NAND Gate **1095**
 - 14.1.6 A Complex Gate **1096**
 - 14.1.7 Obtaining the PUN from the PDN and Vice Versa **1096**
 - 14.1.8 The Exclusive-OR Function **1097**
 - 14.1.9 Summary of the Synthesis Method **1098**
- 14.2 Digital Logic Inverters **1100**
 - 14.2.1 The Voltage-Transfer Characteristic (VTC) **1100**
 - 14.2.2 Noise Margins **1101**
 - 14.2.3 The Ideal VTC **1103**
 - 14.2.4 Inverter Implementation **1103**
- 14.3 The CMOS Inverter **1114**
 - 14.3.1 Circuit Operation **1114**
 - 14.3.2 The Voltage-Transfer Characteristic (VTC) **1117**
 - 14.3.3 The Situation When Q_N and Q_P Are Not Matched **1120**
- 14.4 Dynamic Operation of the CMOS Inverter **1125**

14.4.1 Propagation Delay	1125
14.4.2 Determining the Propagation Delay of the CMOS Inverter	1129
14.4.3 Determining the Equivalent Load Capacitance C	1136
14.5 Transistor Sizing	1139
14.5.1 Inverter Sizing	1139
14.5.2 Transistor Sizing in CMOS Logic Gates	1141
14.5.3 Effects of Fan-In and Fan-Out on Propagation Delay	1145
14.5.4 Driving a Large Capacitance	1146
14.6 Power Dissipation	1149
14.6.1 Sources of Power Dissipation	1149
14.6.2 Power–Delay and Energy–Delay Products	1152
Summary	1154
Problems	1156

15 Advanced Topics in Digital Integrated-Circuit Design 1166

Introduction	1167
15.1 Implications of Technology Scaling: Issues in Deep-Submicron Design	1168
15.1.1 Silicon Area	1169
15.1.2 Scaling Implications	1169
15.1.3 Velocity Saturation	1171
15.1.4 Subthreshold Conduction	1177
15.1.5 Temperature, Voltage, and Process Variations	1178
15.1.6 Wiring: The Interconnect	1178
15.2 Digital IC Technologies, Logic-Circuit Families, and Design Methodologies	1179
15.2.1 Digital IC Technologies and Logic-Circuit Families	1180
15.2.2 Styles for Digital System Design	1182
15.2.3 Design Abstraction and Computer Aids	1182
15.3 Pseudo-NMOS Logic Circuits	1183
15.3.1 The Pseudo-NMOS Inverter	1183
15.3.2 Static Characteristics	1184
15.3.3 Derivation of the VTC	1186
15.3.4 Dynamic Operation	1188
15.3.5 Design	1189
15.3.6 Gate Circuits	1189

15.3.7 Concluding Remarks	1190
15.4 Pass-Transistor Logic Circuits	1192
15.4.1 An Essential Design Requirement	1193
15.4.2 Operation with NMOS Transistors as Switches	1194
15.4.3 Restoring the Value of V_{OH} to V_{DD}	1198
15.4.4 The Use of CMOS Transmission Gates as Switches	1199
15.4.5 Examples of Pass-Transistor Logic Circuits	1206
15.4.6 A Final Remark	1208
15.5 Dynamic MOS Logic Circuits	1208
15.5.1 The Basic Principle	1209
15.5.2 Nonideal Effects	1212
15.5.3 Domino CMOS Logic	1216
15.5.4 Concluding Remarks	1217
15.6 Bipolar and BiCMOS Logic Circuits	1217
15.6.1 Emitter-Coupled Logic (ECL)	1218
15.6.2 BiCMOS Digital Circuits	1223
Summary	1226
Problems	1227

16 Memory Circuits 1236

Introduction	1237
16.1 Latches and Flip-Flops	1238
16.1.1 The Latch	1238
16.1.2 The SR Flip-Flop	1240
16.1.3 CMOS Implementation of SR Flip-Flops	1241
16.1.4 A Simpler CMOS Implementation of the Clocked SR Flip-Flop	1247
16.1.5 D Flip-Flop Circuits	1247
16.2 Semiconductor Memories: Types and Architectures	1249
16.2.1 Memory-Chip Organization	1250
16.2.2 Memory-Chip Timing	1252
16.3 Random-Access Memory (RAM) Cells	1253
16.3.1 Static Memory (SRAM) Cell	1253
16.3.2 Dynamic Memory (DRAM) Cell	1260
16.4 Sense Amplifiers and Address Decoders	1262
16.4.1 The Sense Amplifier	1263

16.4.2	The Row-Address Decoder	1271
16.4.3	The Column-Address Decoder	1273
16.4.4	Pulse-Generation Circuits	1274
16.5	Read-Only Memory (ROM)	1276
16.5.1	A MOS ROM	1276
16.5.2	Mask Programmable ROMs	1278
16.5.3	Programmable ROMs (PROMs, EPROMs, and Flash)	1279
16.6	CMOS Image Sensors	1281
	Summary	1282
	Problems	1283

PART IV FILTERS AND OSCILLATORS 1288

17 Filters and Tuned Amplifiers 1290

	Introduction	1291
17.1	Filter Transmission, Types, and Specification	1292
17.1.1	Filter Transmission	1292
17.1.2	Filter Types	1293
17.1.3	Filter Specification	1293
17.2	The Filter Transfer Function	1296
17.3	Butterworth and Chebyshev Filters	1300
17.3.1	The Butterworth Filter	1300
17.3.2	The Chebyshev Filter	1304
17.4	First-Order and Second-Order Filter Functions	1307
17.4.1	First-Order Filters	1308
17.4.2	Second-Order Filter Functions	1311
17.5	The Second-Order LCR Resonator	1316
17.5.1	The Resonator Natural Modes	1316
17.5.2	Realization of Transmission Zeros	1317
17.5.3	Realization of the Low-Pass Function	1317
17.5.4	Realization of the High-Pass Function	1319
17.5.5	Realization of the Bandpass Function	1319
17.5.6	Realization of the Notch Functions	1319
17.5.7	Realization of the All-Pass Function	1321
17.6	Second-Order Active Filters Based on Inductor Replacement	1322

17.6.1	The Antoniou Inductance-Simulation Circuit	1322
17.6.2	The Op Amp–RC Resonator	1323
17.6.3	Realization of the Various Filter Types	1325
17.6.4	The All-Pass Circuit	1325
17.7	Second-Order Active Filters Based on the Two-Integrator-Loop Topology	1330
17.7.1	Derivation of the Two-Integrator-Loop Biquad	1330
17.7.2	Circuit Implementation	1332
17.7.3	An Alternative Two-Integrator-Loop Biquad Circuit	1334
17.7.4	Final Remarks	1335
17.8	Single-Amplifier Biquadratic Active Filters	1336
17.8.1	Synthesis of the Feedback Loop	1336
17.8.2	Injecting the Input Signal	1339
17.8.3	Generation of Equivalent Feedback Loops	1341
17.9	Sensitivity	1344
17.10	Transconductance-C Filters	1347
17.10.1	Methods for IC Filter Implementation	1347
17.10.2	Transconductors	1348
17.10.3	Basic Building Blocks	1349
17.10.4	Second-Order G_m –C Filter	1351
17.11	Switched-Capacitor Filters	1354
17.11.1	The Basic Principle	1354
17.11.2	Practical Circuits	1356
17.11.3	Final Remarks	1359
17.12	Tuned Amplifiers	1359
17.12.1	The Basic Principle	1360
17.12.2	Inductor Losses	1362
17.12.3	Use of Transformers	1363
17.12.4	Amplifiers with Multiple Tuned Circuits	1365
17.12.5	The Cascode and the CC–CB Cascade	1366
17.12.6	Synchronous Tuning and Stagger Tuning	1367
	Summary	1368
	Problems	1369

18 Signal Generators and Waveform-Shaping Circuits 1378

	Introduction	1379
18.1	Basic Principles of Sinusoidal Oscillators	1380

18.1.1 The Oscillator Feedback Loop	1380	18.6 Generation of a Standardized Pulse: The Monostable Multivibrator	1417
18.1.2 The Oscillation Criterion	1381	18.7 Integrated-Circuit Timers	1419
18.1.3 Analysis of Oscillator Circuits	1382	18.7.1 The 555 Circuit	1419
18.1.4 Nonlinear Amplitude Control	1385	18.7.2 Implementing a Monostable Multivibrator Using the 555 IC	1420
18.1.5 A Popular Limiter Circuit for Amplitude Control	1386	18.7.3 An Astable Multivibrator Using the 555 IC	1420
18.2 Op Amp–RC Oscillator Circuits	1388	18.8 Nonlinear Waveform-Shaping Circuits	1424
18.2.1 The Wien-Bridge Oscillator	1388	18.8.1 The Breakpoint Method	1424
18.2.2 The Phase-Shift Oscillator	1391	18.8.2 The Nonlinear-Amplification Method	1426
18.2.3 The Quadrature Oscillator	1392	Summary	1428
18.2.4 The Active-Filter-Tuned Oscillator	1394	Problems	1428
18.2.5 A Final Remark	1396		
18.3 LC and Crystal Oscillators	1396		
18.3.1 The Colpitts and Hartley Oscillators	1396		
18.3.2 The Cross-Coupled LC Oscillator	1400		
18.3.3 Crystal Oscillators	1402		
18.4 Bistable Multivibrators	1404		
18.4.1 The Feedback Loop	1405		
18.4.2 Transfer Characteristic of the Bistable Circuit	1406		
18.4.3 Triggering the Bistable Circuit	1407		
18.4.4 The Bistable Circuit as a Memory Element	1407		
18.4.5 A Bistable Circuit with Noninverting Transfer Characteristic	1408		
18.4.6 Application of the Bistable Circuit as a Comparator	1409		
18.4.7 Making the Output Levels More Precise	1411		
18.5 Generation of Square and Triangular Waveforms Using Astable Multivibrators	1412		
18.5.1 Operation of the Astable Multivibrator	1413		
18.5.2 Generation of Triangular Waveforms	1415		

Appendices

- A. VLSI Fabrication Technology (on website) A-1
- B. SPICE Device Models and Design and Simulation Examples Using PSpice® and Multisim™ (on website) B-1
- C. Two-Port Network Parameters (on website) C-1
- D. Some Useful Network Theorems (on website) D-1
- E. Single-Time-Constant Circuits (on website) E-1
- F. s-Domain Analysis: Poles, Zeros, and Bode Plots (on website) F-1
- G. Comparison of the MOSFET and the BJT (on website, also Table G.3 in text) G-1
- H. Design of Stagger-Tuned Amplifiers (on website) H-1
- I. Bibliography (on website) I-1
- J. Standard Resistance Values and Unit Prefixes J-1
- K. Typical Parameter Values for IC Devices Fabricated in CMOS and Bipolar Processes K-1
- L. Answers to Selected Problems (on website) L-1

Index IN-1

TABLES

FOR REFERENCE AND STUDY

Table 1.1	The Four Amplifier Types 28
Table 1.2	Frequency Response of STC Networks 36
Table 2.1	Characteristics of the Ideal Op Amp 62
Table 3.1	Summary of Important Semiconductor Equations 169
Table 5.1	Regions of Operation of the NMOS Transistor 266
Table 5.2	Regions of Operation of the PMOS Transistor 275
Table 6.1	BJT Modes of Operation 307
Table 6.2	Summary of the BJT Current–Voltage Relationships in the Active Mode 322
Table 6.3	Simplified Models for the Operation of the BJT in DC Circuits 334
Table 7.1	Systematic Procedure for the Analysis of Transistor Amplifier Circuits 421
Table 7.2	Small-Signal Models of the MOSFET 421
Table 7.3	Small-Signal Models of the BJT 422
Table 7.4	Characteristics of MOSFET Amplifiers 452
Table 7.5	Characteristics of BJT Amplifiers 453
Table 8.1	Gain Distribution in the MOS Cascode Amplifier for Various Values of R_L 554
Table 10.1	The MOSFET High-Frequency Model 716
Table 10.2	The BJT High-Frequency Model 722
Table 11.1	Summary of the Parameters and Formulas for the Ideal Feedback-Amplifier Structure of Fig. 11.1 815
Table 11.2	Summary of Relationships for the Four Feedback-Amplifier Topologies 872
Table 13.1	DC Collector Currents of the 741 Circuit (μA) 1038
Table 14.1	Important Parameters of the VTC of the Logic Inverter 1102
Table 14.2	Summary of Important Characteristics of the CMOS Logic Inverter 1155
Table 15.1	Implications of Device and Voltage Scaling 1170
Table 15.2	Regions of Operation of the Pseudo-NMOS Inverter 1187
Table 17.1	Design Data for the Circuits Based on Inductance Simulation (Fig 17.22) 1328
Table 17.2	Design Data for the Tow-Thomas Biquad Circuit in Fig 17.26 1335
Table G.3	Comparison of the MOSFET and the BJT G-1
Table J.1	Standard Resistance Values J-1
Table J.2	SI Unit Prefixes J-2
Table J.3	Meter Conversion Factors J-2
Table K.1	Typical Values of CMOS Device Parameters K-1
Table K.2	Typical Parameter Values for BJTs K-1