SEVENTH EDITION

Microelectronic Circuits

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University of Toronto

New York Oxford
OXFORD UNIVERSITY PRESS

Oxford University Press is a department of the University of Oxford. It furthers the University's objective of excellence in research, scholarship, and education by publishing worldwide.

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Published in the United States of America by
Oxford University Press
198 Madison Avenue, New York, NY 10016
http://www.oup.com

Library of Congress Cataloging-in-Publication Data

Sedra, Adel S., author.
Microelectronic circuits / Adel S. Sedra, University of Waterloo, Kenneth C. Smith, University of Toronto. — Seventh edition.
pages cm. — (The Oxford series in electrical and computer engineering)
Includes bibliographical references and index.
ISBN 978–0–19–933913–6
1. Electronic circuits. 2. Integrated circuits. I. Smith, Kenneth C. (Kenneth Carless), author. II. Title.
TK7867.S39 2014
621.3815—dc23 2014033965

Cover Photo: This 3D IC system demonstrates the concept of wireless power delivery and communication through multiple layers of CMOS chips. The communication circuits were demonstrated in an IBM 45 nm SOI CMOS process. This technology is designed to serve a multi-Gb/s interconnect between cores spread across several IC layers for high-performance processors.
(Photo Credit: The picture is courtesy of Professor David Wentzloff, Director of the Wireless Integrated Circuits Group at the University of Michigan, and was edited by Muhammad Faisal, Founder of Movellus Circuits Incorporated.)

Printing number: 9 8 7 6 5 4 3 2 1

Printed in the United States of America
on acid-free paper

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FOR REFERENCE AND STUDY