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FOR ENGINEERS AND ENGINEERING MANAGERS-WORLDWIDE

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USABLE GATES	7K - 31K	15K - 63K	22K - 69K	29K - 93K	36K - 116K	46K - 118K	62K - 158K	82K - 211K
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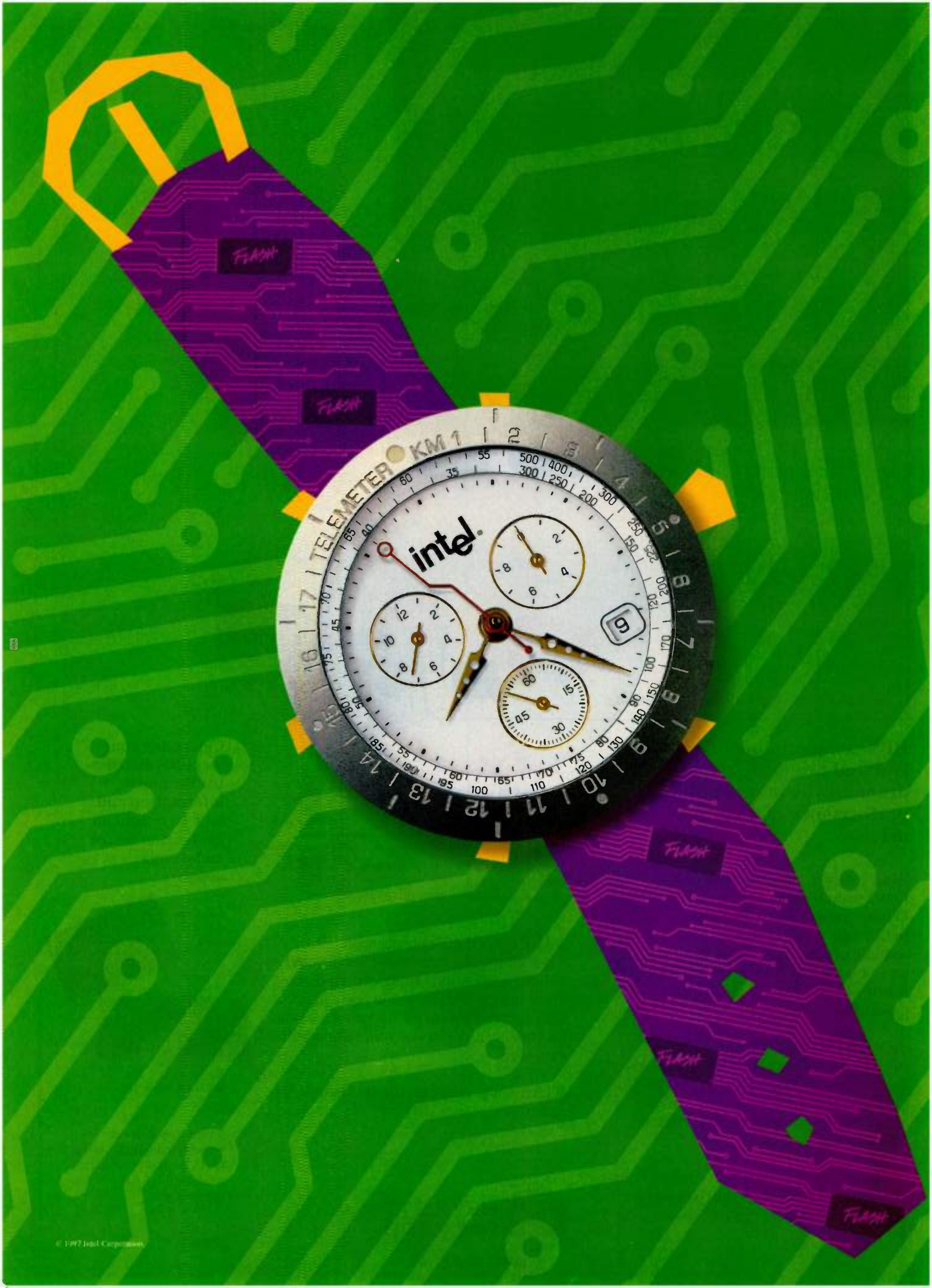
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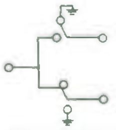

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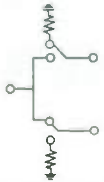

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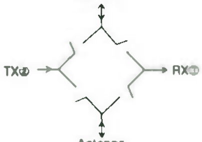

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ELECTRONIC DESIGN

August 4, 1997 Volume 45, Number 16

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PIPS

SENSOR TECHNOLOGY

QUICKLOOK

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1968 First Place Award
1972 Certificate of Merit
1975 Two Certificates of Merit
1976 Certificate of Merit
1978 Certificate of Merit
1980 Certificate of Merit
1986 First Place Award
1989 Certificate of Merit
1992 Certificate of Merit

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ELECTRONIC DESIGN

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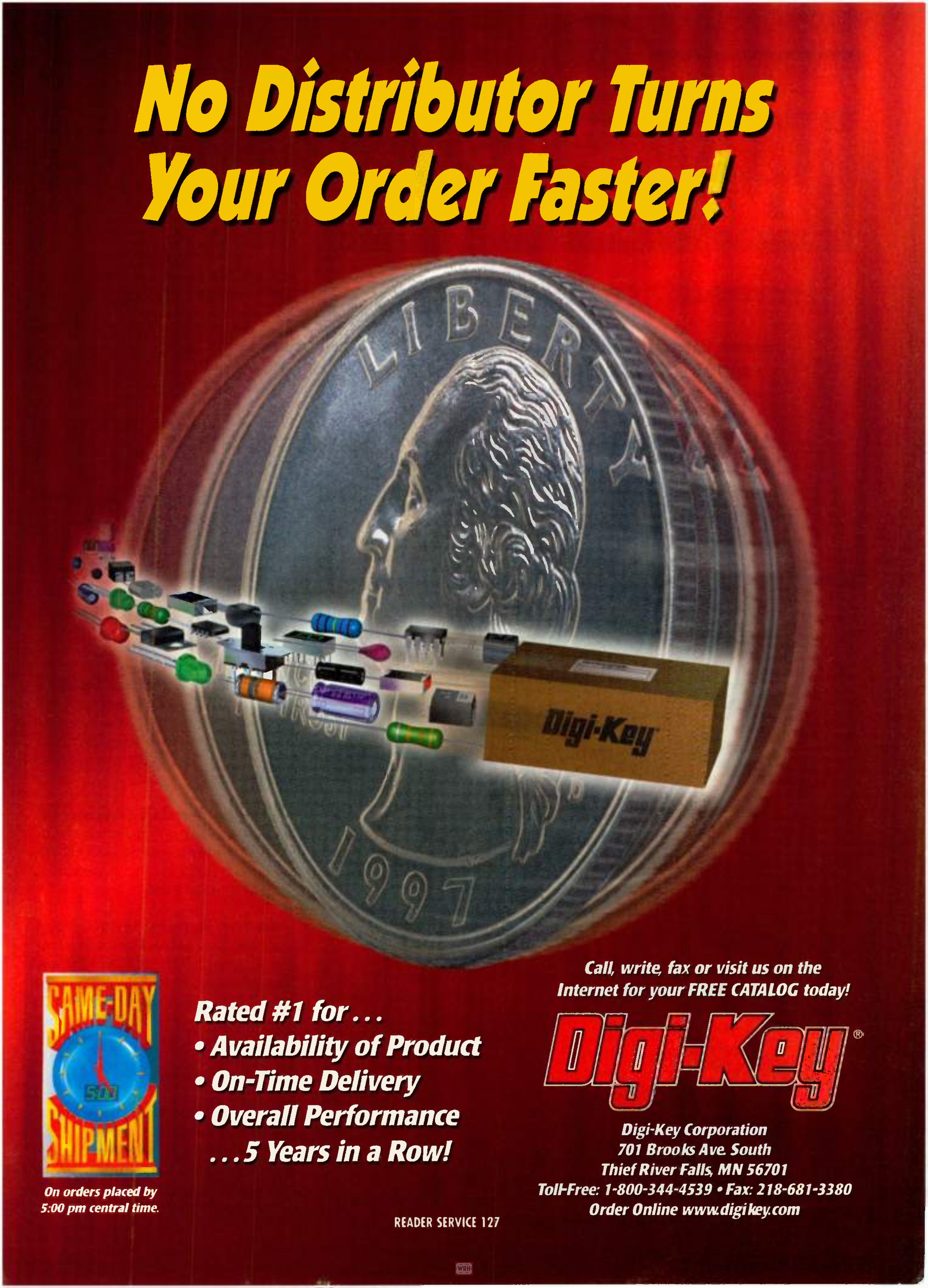
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AUGUST 1997

IEEE International Symposium on Electromagnetic Compatibility (EMC '97), August 18-22. Contact John Osburn, EMC Test Systems LP., 2205 Kramer Lane, Austin, Texas 78758; (512) 835-4684, ext. 669; fax (512) 835-4729.

SEPTEMBER

Seventh Surface Mount International (SMD) Conference & Exhibition, September 7-11. San Jose Convention Center, San Jose, California. Contact Miller Freeman information desk (617) 821-6720; Internet: http://www.surfacemount.com.

Telecom Interactive '97, Sept. 8-14. Geneva, Switzerland. Contact (703) 907-7736.

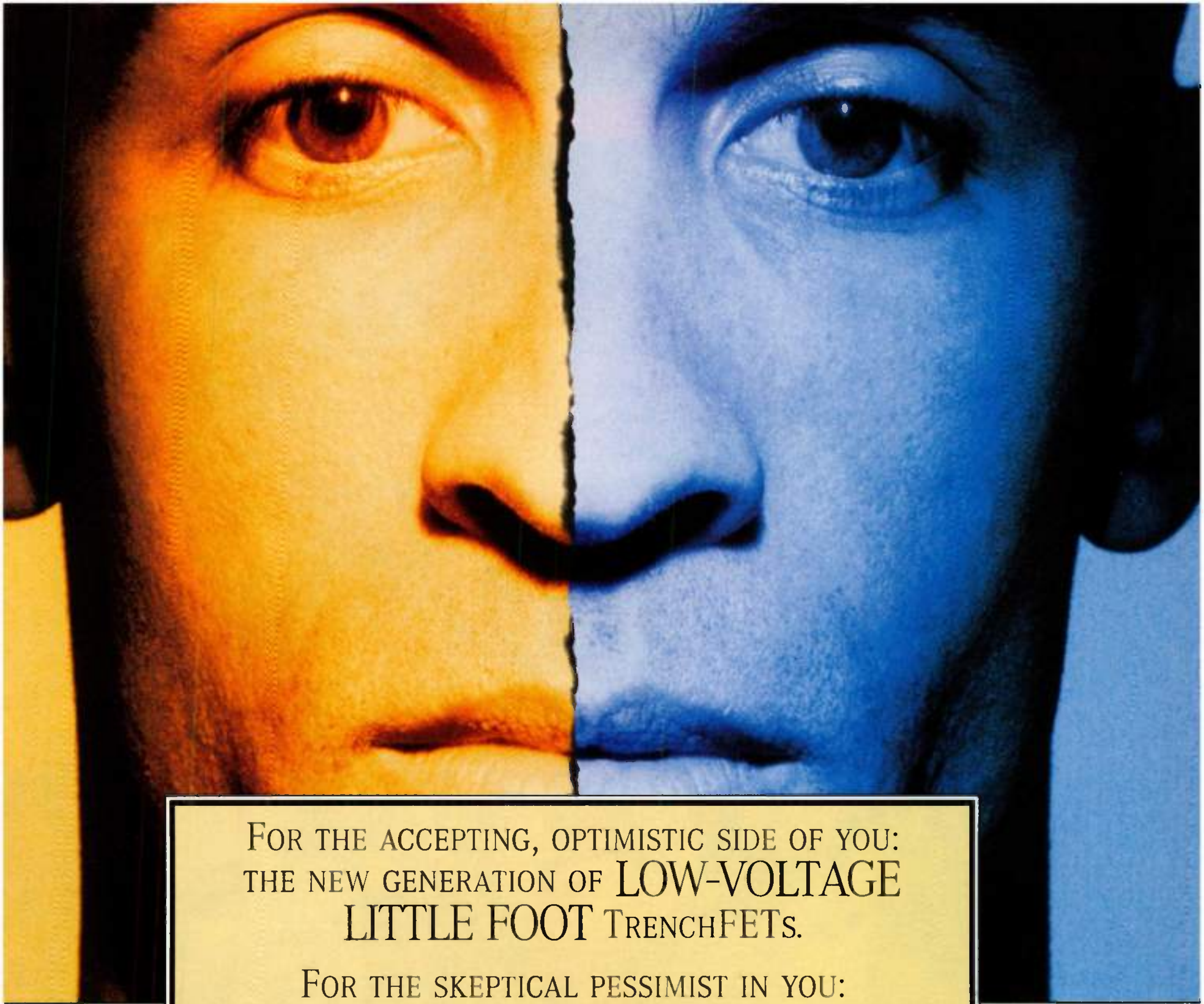
Fifth European Congress on Intelligent Techniques and Soft Computing (EUFIT '97), September 8-11. Aachen, Germany. Contact Promenade 9, 52076 Aachen, Germany; (49) 2408 6969; fax (49) 2408 94582; e-mail: eufit@mitgmbh.de; Internet: http://www.mitgmbh.de/elite/elite/-eufit.html.

ICSPAT & DSP World Expo, September 14-17. San Diego Convention Center, San Diego, California. Contact Jennifer Call, Miller Freeman Inc., (415) 278-5239; e-mail: jcall@mfi.com.

MCM Test Workshop, September 14-17. Napa Valley, California. Contact Y. Zorian, (408) 453-0146, ext. 227; e-mail: zorian@lvision.com.

Northcon, September 16-18. Oregon Convention Center, Portland, Oregon. Contact Electronic Conventions Management, 8110 Airport Boulevard, Los Angeles, California 90045; (800) 877-2668 or (310) 215-3976; fax (310) 641-5117; e-mail: northcon@ieee.org; Internet: www.northcon.org.

The Vision Show, Sept. 16-18. Santa Clara Convention Center, Santa Clara, California. Contact Automated Imaging Association, Ann Arbor, Michigan, (313) 994-6088; fax (313) 994-3338.



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FOR THE SKEPTICAL PESSIMIST IN YOU: THE REST OF THE FACTS.

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You know, the part that wants cold, hard facts. Irrefutable evidence. For that large, commanding section of your psyche, may we present our new low-voltage LITTLE FOOT TrenchFETs.

First, they are half the size of our previous generation of TrenchFETs, or half the on-resistance. That is verifiable, mathematical, and 100% accurate. And then throw in something no other MOSFET manufacturer can do: speak your language. We're talking about TrenchFETs with 2.5- and 4.5-volt ratings, the voltages you have available in your designs. We're talking about TrenchFETs with p-channel options you use in your designs today, with lower resistance than the n-channel MOSFETs. We're talking about the things you care about when you design products today—NOT the 10-volt and n-channel technology you used yesterday (we'll let others talk about that).

But if you're still in need of convincing, Mr. Incredulous, there is simply one thing to do. Call us at **1-800-554-5565 ext.546** to try our new low-voltage LITTLE FOOT TrenchFETs when you're designing your next battery operated product.

We guarantee, that every bit of you will approve.

LOW VOLTAGE	Part No.	Type	R_{DS}@ V_{GS}= 4.5V	R_{DS}@ V_{GS}= 2.5V
20-V n-channel TrenchFETs optimized for operations at low V_{GS} are used for switches in Li-Ion batteries	Si4466DY	single/N-Ch.	0.009	0.013
	Si4966DY	dual/N-Ch.	0.020	0.030
	Si3446DV	single/N-Ch.	0.035	0.060
	Si6466DQ	single/N-Ch.	0.014	0.021
	Si6966DQ	dual/N-Ch.	0.035	0.050
20-V p-channel TrenchFETs optimized for operations at low V_{GS} are used for load switches in cell phones and notebook PCs	Si4463DY	single/P-Ch.	0.014	0.020
	Si4963DY	dual/P-Ch.	0.033	0.050
	Si3443DV	single/P-Ch.	0.065	0.100
	Si6463DQ	single/P-Ch.	0.020	0.030
	Si6963DQ	dual/P-Ch.	0.045	0.090
20-V n&p-channel MOSFETs pairs	Si4562DY	N-Ch. / P-Ch. } pair	0.020 / 0.030	0.030
	[illegible]	N-Ch. / P-Ch. } pair	0.035 / 0.085	0.050

DY=SO-8, DV=TSOP-6, DQ=TSSOP-8

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SEPTEMBER

International Conference on Solid State Devices and Materials (SSDM), Sept. 16-19. Act City Hamamatsu, Hamamatsu, Japan. Contact Secretariat of SSDM '97, Business Center for Academic Societies Japan, 5-16-9 Honkomagome, Bunkyo,Tokyo 113, Japan; (81) 3 5814 5800; fax (81) 3 5814 5823; e-mail: confg3@bcasj.or.jp.

Photomask Technology & Management Conference & Exhibition, Sept. 17-19. Redwood City, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Thermionic Workshop, Sept. 21-23. Cannes, France. Contact Bernard Courtois, (33) 35 76 7 46 15; e-mail: bernard.courtois@imag.fr.

ISS'97: World Telecommunications Congress, Sept. 21-26. Toronto, Canada. Contact The Pinnacle Group: Victoria Lord, (416) 588-2420; Jane Tucker, (416) 588-3522; Internet: http://www.ISS97.org.

Photonics East & Electronic Imaging International Exhibition, Sept. 22-24. Boston, MA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

AUTOTESTCON '97, Sept. 22-25. Disneyland Hotel, Anaheim, CA. Contact Robert C. Rassa, Hughes Aircraft, P.O. Box 92426, MS R07/P553, Los Angeles, CA 90009-2426; (310) 334-4922; fax (310) 334-2578; e-mail: rcrassa@ccgate.hac.com.

Electrical Overstress/Electrostatic Discharge Symposium, Sept. 23-25. Santa Clara Convention Center, Santa Clara, CA. Contact ESD Association, 7902 Turin Rd., Suite 4, Rome, NY 13440-2069; (315) 339-6937; fax (315) 339-6793.

Fifth China International Electronics Exhibition (CIEE '97), Sept. 24-28. China International Exhibition Centre, Beijing. Contact Gu Jinjing, CEIEC, P.O. Box 140, Beijing, 100036 China; (011) 8610 6822 3909; fax (011) 8610 6821 3348.

Eastern Regional Conference on Crystal Growth & Epitaxy, ACCGE/East-97, Sept. 28-Oct. 1. Bally's Park Place Hotel & Casino, Atlantic City, NJ. Contact Louis G. Casagrande, (516) 346-6379; fax (516) 346-3670; e-mail: Lou_Casagrande@atdc.grumman.com, or Ed Porbansky, Conference Secretariat, 163 Carson Dr., Colonia, NJ 07067; (908) 382-1806.

Embedded Systems Conference, Sept. 29-Oct. 2. San Jose Convention Center, San Jose, CA. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563; (415) 538-3848; e-mail: esc@mfi.com.

OCTOBER

OEMed Northeast, Oct. 1-2. Bayside Expo Center, Boston, MA. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

EDITORIAL

May You (And I) Live In Exciting Times

Two items caught my eye recently as I was sifting through a pile of paper at day's end. One was a press release announcing the coming of the "second silicon revolution." The other was a paper from Lucent Technologies celebrating the "dawn of the information age"— the invention of the transistor 50 years ago.

What an interesting stroke of luck, I thought. In my hands I was reading about the past, present, and future of the electronics industry.

Although I enjoy reading historical perspectives as much as the next guy, I 'm of the mind-set that the future is more important in my line of work. Moreover, whenever I see or hear the word "revolution" tossed around on TV or in a headline, that in itself is generally enough to snap me to attention No one wants to be the last to know that a revolution is brewing in the streets.

The Future: According to the release, Sandia National Laboratories has licensed its intelligent micromachine technology to Analog Devices Inc., which will commercialize the technology. An integrated micromachine is a tiny "smart" machine that combines microcircuits, sensors, and actuators on a single computer chip. The agreement is expected to help stimulate production of a new generation of very small consumer and military devices.

"Devices we envision represent a second silicon revolution," said Paul McWhorter, manager of Sandia's micromachine effort. "We're not simply adding more, smaller transistors to a chip. We are adding functions that can sense and act."

McWhorter explained that packing more transistors onto a chip to make a more powerful computer, for example, is history. He says the licensing agreement "will beak this trend" by focusing on the development of chips with not only electronics but also small machines, which gives this new revolutionary chip the ability to sense where they are and what is going on around them. He predicts the micromechanical industry will reach $8 to $12 billion by the year 2000.

The Past: Considering what the future may hold for us, it's quite amazing to recall that the transistor was invented only 50 years ago. The report, 'The Transistor: 50 Glorious Years and Where We're Going," written by William F. Brickman, vice president, Physical Sciences Research, Lucent Technologies *(http://www.lucent.com/ideas2heritage/transistor)*, is a fascinating account of the Bell Labs team that discovered the transistor effect only two years after the formation of the team, and the subsequent growth of the industry.

The Chinese proverb that headlines this editorial certainly holds true for those of us involved in the electronics industry.

Tom Halligan
Editor-in-Chief
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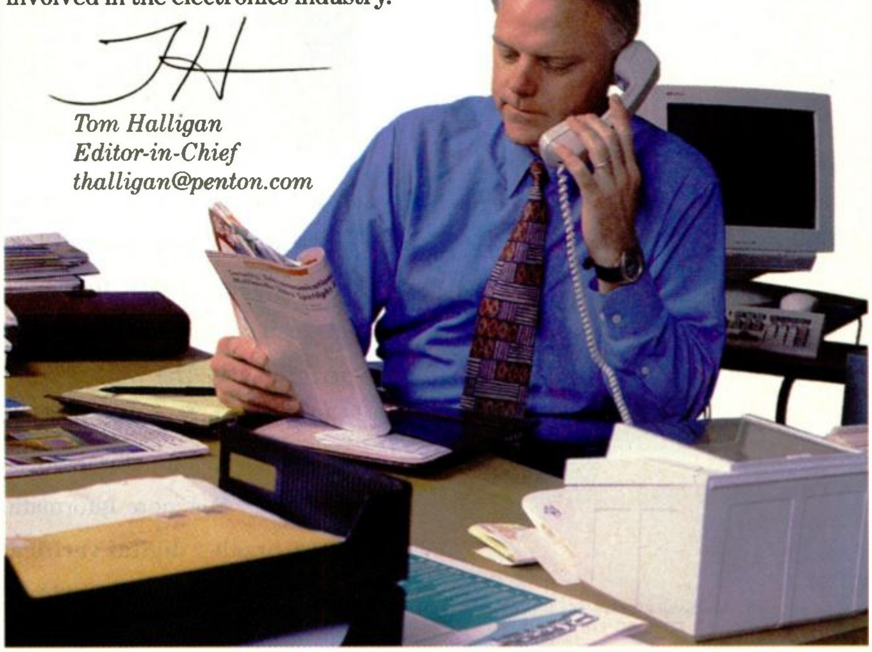

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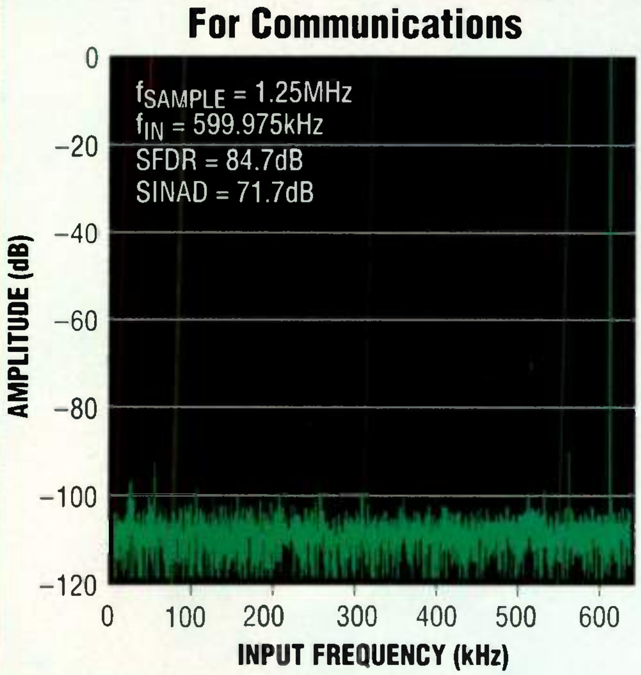

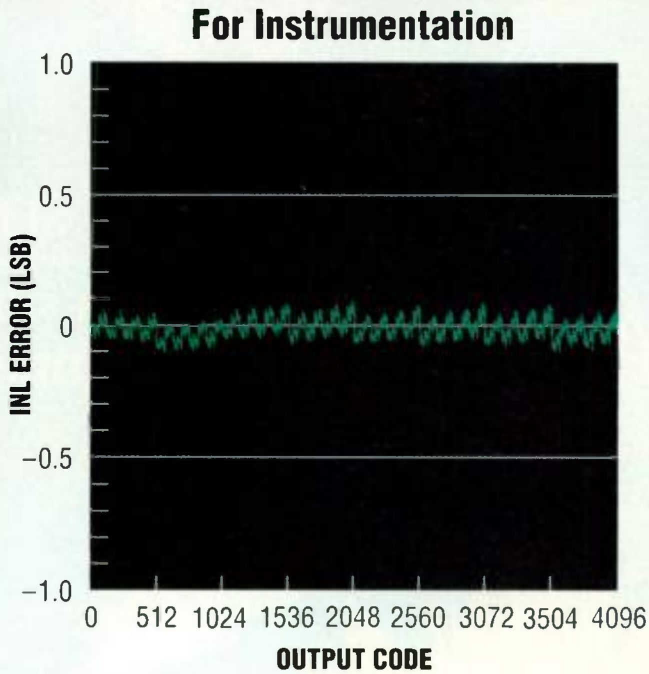

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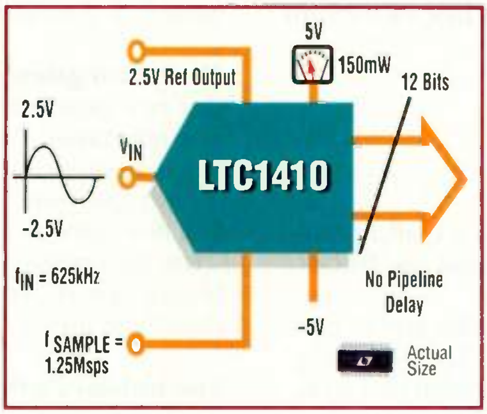

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On the Internet at http://www.ic.nec.co.jp/index_e.html

Getting Back To Basics, Together

This column is about working together, putting oneself in a secondary position, and trying to understand the whole. I have written several times here about the dangers of land mines left on and in the fields of wars in various parts of the world. Politicians, talk-show hosts, our competition, and even royalty have taken up the cause in one form or another in the last year. Good for them! The need to get these destructive devices that kill and maim the innocent out of the world's arsenals is a no-brainer. But with all their good intent at banning, which the U.S. Government is still adamant about not doing, the well-intentioned forget the basics.

The mines that kill children, tear off legs, and destroy livestock are not the products of most developed nations. In battle, in accordance with conventions, a country like the U.S. plants mines and maps them; at the end of the conflict, they remove them. The mines in Angola, Afghanistan, and all the other countries where they lay waiting are mostly homemade. You can build a limb-ripper in the casing of a pen for less than a dollar.

The world must rid itself of this menace with detection systems that will recover those that are already planted, and make the planting of new ones a useless exercise. The only people who are going to be able to design and build systems that will work 100% of the time are you, our readers. If you have a message about a (potential) solution let me know; I will get it circulated!


PAUL McGOLDRICK
ANALOG

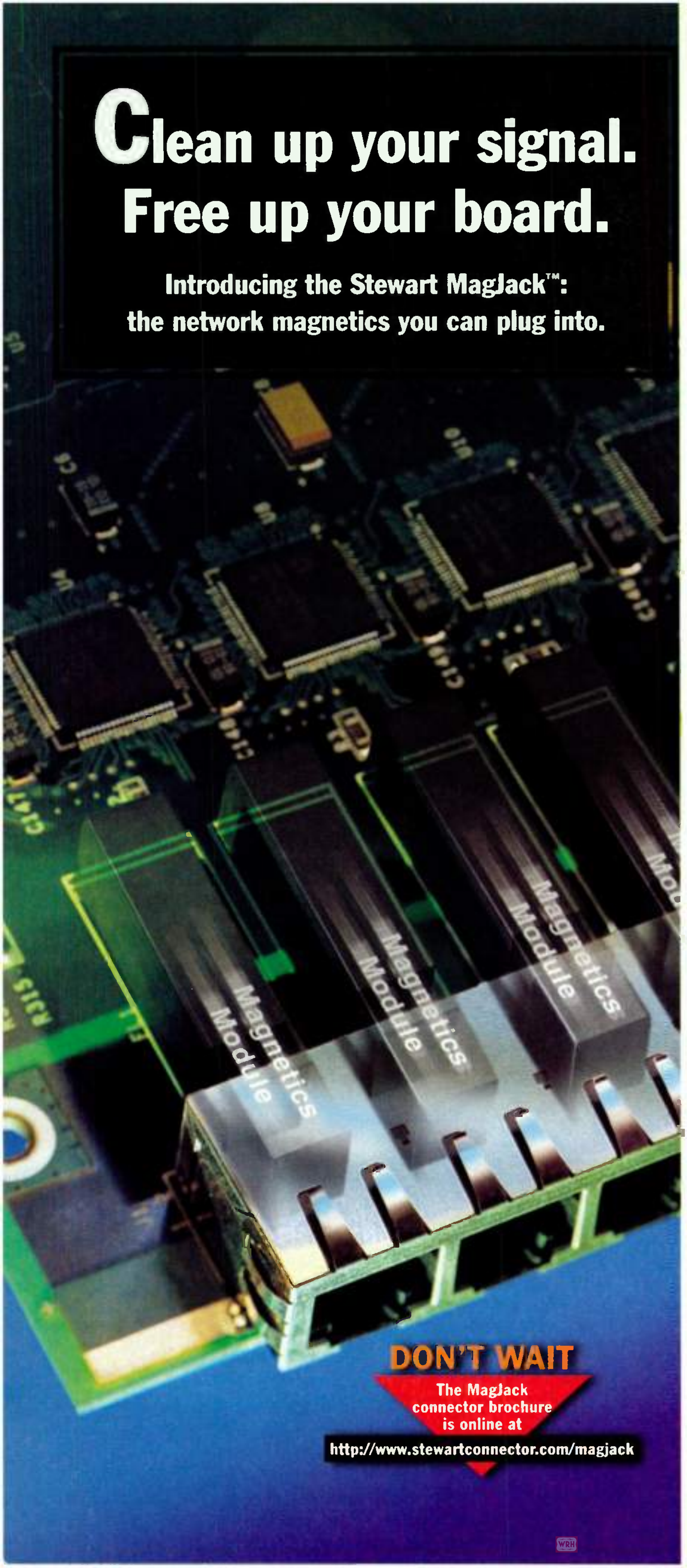
Editors, like me, have egos. Some are larger than others, but there is no standard measuring system available. That might be a blessing in disguise because it does at least stop individuals from developing their ego to match the highest available. We are paid to have opinions, which we should be able to justify if we are called on them. But on a daily basis, we make decisions about what stories we are going to write and what we will accept as contributed articles. We do that on the basis of our experience as to the importance to you and the commercial impact the technology or part is going to make.

This too is often an individual decision and it is hoped that individual editors have unbiased views of the companies, the way the story is presented, and the outcome. Some of us go to great lengths to do that, even to the extent of not owning any technology stocks at all. Some of us will talk with our colleagues about their feelings about the importance of the story. We may disagree and the other guy might write it because he/she thinks it is important. It happens between Frank Goodenough and myself on a weekly basis.

I was at a housewarming recently. The house was located fairly deep in the country with just the occasional Harley biking past at a rate of knots designed to keep the deer off the road. The homeowner is a PR person who is incredibly smart and who, at the moment, has no clients on my analog side of the fence. Another editor, from another magazine, also was there and the conversation somehow drifted to talk about a third editor, known to all three of us, who consistently falls asleep during briefings. The realization that from different sides of the fence and from different magazines we have been protecting this person is a little unbelievable. The basics of grade-school "don't-be-a-tattletale" obviously dies hard! That is the kind of working together that is unhealthy, and downright unprofessional.

Visiting about ten companies a month, it becomes quite clear which of them have got the real synergy of marketing, sales and engineering working together. It is horribly few. The pressure to create the needed teamwork for it to happen can only come from one place—the top. I once wrote about a management situation in a major company that left a remarkable design team afloat without oars. A few company staffers recognized the group involved and were suitably embarrassed. It didn't help. The design group is gone. The company had to purchase another company to replace the lost products in what is a core area of their business. Corporate America, please wake up!

As always, I wait to be abused at *PMcGoldrick@compuserve.com.*



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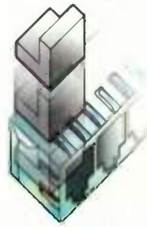

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READER SERVICE 174

Advanced Silicon-On-Insulator Process Boosts Performance

An enhanced silicon-on-insulator process employing sapphire substrates overcomes many of the yield-limiting factors that held back the use of SOS technology from mass-market applications. Developed by Peregrine Semiconductor Inc., San Diego, Calif., the improved processing allows MOS transistors with 0.5-µm features to deliver f_{max} values of 50 GHz. The process is based on both a single solid-phase epitaxy regrowth technique to form ultra-thin silicon films on sapphire substrates, and research done by Hewlett-Packard involving material annealing to produce high-quality, volume-producible SOS wafers. The process yields a low-defect-density film with a final thickness of 100 nm and electron and hold mobilities similar to those found in bulk silicon.

The resulting wafers then are processed with standard CMOS processing equipment—as done by Peregrine's production partner, Asahi Kasei Microsystems Co. Ltd., Tokyo, Japan, which manufactures circuits based on a 0.7-µm single-poly, triple-level-metal process. Local oxidation of silicon is used for device isolation, gate oxides are 13 nm, and oxide spacers are used to form lightly doped drain structures. One issue does arise with SOS: Its transparency often causes optical sensors on the processing equipment to not always detect the presence of a wafer. Thus, to minimize such problems, the back side of the wafer is coated with a polysilicon/nitride sandwich to reduce the transparency.

Transistors manufactured with the SOS technology have extremely linear performance. Such a characteristic make them ideal for CDMA communication applications and high-compression-point signals, such as found in high-frequency communications. As proof of concept, last month the company released a dual fractional divide-by-N phase-locked loop that has an upper frequency of 1.1 GHz or 510 MHz. The circuit achieves a very low phase noise—less than –82 dBc/Hz at a 2-kHz offset or a 30-kHz step at a carrier frequency of 900 MHz.. Contact Jon Siann at (619) 646-8888; or on the web at http://www.peregrine-semi.com. *DB*

Changes In The World Of Images Spurs Interdisciplinary Programs

The sweeping way in which the world is represented by images has changed: Gone are the analog, monochrome, standalone, passive images; in are the digital, color, communicative, interactive images. These changes were recognized by Stanford University by the formation of Image Systems Engineering, a multidisciplinary program established from psychology, electrical engineering, and computer science with the aim of training students for the growing number of positions in the new field of imaging science.

The prime mover behind the program is professor of psychology Brian Wandell, who sees the single curriculum as making sense. Another psychologist, David Heeger, who also is involved in other departments, feels that imaging science is a peripheral subject in all three disciplines. In psychology, it is the study of human vision; in electrical engineering, it is image processing; in computer science, it is research into computer vision. Tangible evidence of industry interest comes by way of a $1 million equipment grant from Hewlett-Packard to equip a new image processing laboratory. Xerox has also given financial support.

HP circulated an RFP on programs in image-systems engineering. Out of 23 applications, the company funded five. In addition to Stanford the University of California at San Diego, the Georgia Institute of Technology, the University of Iowa, and Purdue were selected.

The curriculum now includes 14 courses that fall into three paths: medical imaging, image processing, and Fourier and statistical optics. Ninety students used the lab in the first year. For more information, contact Brian Wandell, Psychology, at: brian@psych.stanford.edu; Joseph Goodman, Engineering, at: goodman@EE.stanford.edu. *PMcG*

Integrated Smart Micromachine Technology Focus Of Agreement

Sandia National Laboratories, Albuquerque, N.M., and Analog Devices, Woburn, Mass., have reached an agreement in which Sandia has licensed Analog Devices to commercialize the technology used to make Sandia's integrated micromachines. An integrated micromachine is a tiny "smart" machine that combines microcircuits, sensors, and actuators on a single computer chip.

Expectations are that the agreement will help stimulate production of a new generation of very small consumer and military devices. In cars, these should include anti-tamper, anti-skid, and active-vibration control systems. Says Paul McWhorter, manager of Sandia's micromachine effort, "Devices we envision represent a second silicon revolution. We're not simply adding more, smaller transistors to a chip. We are adding functions that sense and act."

The long-term license involves transfer of Sandia's intelligent micromachine technology to Analog Devices. Analog has been in the forefront of micromachining; its airbag sensors use micromachines to signal when a vehicle is undergoing sufficiently rapid, sustained deceleration for the airbag to deploy.

Because batches of silicon micromachines can be fabricated through manufacturing techniques already widely used to make ICs, micromachines are much less expensive than the complicated multi-metal constructions originally necessary to signal an airbag to inflate. Rather than being made individually, micromachines can be fabricated quickly and inexpensively by the thousands. Furthermore, due to the machines being so lightweight, they're less likely to be damaged by sudden deceleration, because force is proportional to mass (which in this case is almost nonexistent). Contact Sandia at (505) 844-8066; fax (505) 844-6367. *RE*

Gallium-Nitride-Based Blue Lasers Last Over One Hour

Based on gallium nitride (GaN) on a silicon-carbide (SiC) substrate, a pulsed blue laser developed by Cree Research Inc., Durham, N.C., was measured with a lifespan of over one hour. Emitting at a wavelength of 402 nm, the laser uses a 0.1 % duty cycle at a 1-kHz repetition rate and has threshold current density of 1.2 A at 42 V. Key to the device's operation is the use of SiC as the substrate.

While other manufacturers have based their efforts on sapphire, the high current density of Cree's device—48 kA/cm^2—necessitates using SiC due to its higher thermal conductivity. This prolongs the device's active life before burnout. Proclaimed the Holy Grail of optical storage systems, a blue laser source could increase storage capacity by a factor of four or five times due to its shorter wavelength, relative to the red or infrared laser being used today.

While an operating lifespan of one hour is a far cry from the 10,000-hour minimum required for commercial applications, researchers at Cree are continuing to focus their efforts to improve the device along epitaxial and fabrication avenues. Cree is the first to demonstrate a pulsed blue laser based on this technology here in the U.S., but the competitive nature of the research being done in this area unfortunately means that details on device structure often are vague. Competition comes mainly from Japan, where Nichia Chemical, Neijo University, and Toshiba have made substantial gains. Although Nichia's sapphire-based devices are more advanced— achieving lifespans in the tens of hours—Cree feels that, due to the high levels of power dissipation, SiC is the way to go. Call Alan Robertson at (919) 361-5709 or fax (919) 361-4630. *PM*

Record Solar Efficiency Achieved By Thin Film Photovoltaic Array

Tests conducted on a series of thin film photovoltaic arrays at the National Renewable Energy Laboratory (NREL) yielded a new world's record for efficiency. The 1-kW array under test consisted of 28 modules, each producing an average power level of 39 W, with an overall efficiency of 9%. Manufactured by Siemens Solar Group, Munich Germany, the modules contain solar cells fabricated using advanced copper-indium di-selenide (CIS) thin-film technology. The entire cell structure consists of four layers: a molybdenum base that serves as a contact and a mechanical substrate; a modified CIS semiconductor absorber; a very thin layer of cadmium sulfide that acts as a junction; and a transparent zinc oxide top conductor/electrode. The best module in the array was confirmed by NREL to produce 40.6 W, setting a new world-record for efficiency for thin-film modules of this size at 11.1% from aperture area of 3665 square centimeters.

The cells have several advantages over conventional wafer-based crystalline silicon units. For instance, the panels are constructed monolithically on large substrates with built-in interconnect circuitry. This eliminates the wiring and labor needed to assemble a panel from a large group of small cells. Also, the vapor-deposition fabrication process has the potential to be much less expensive than conventional semiconductor manufacturing methods. The new Champion module is based on the standard frame and junction hardware from their SM55 series of modules. For more information, contact the Siemens Solar Group's offices in Camarillo, Calif. at (905) 388-6525, or in Germany at +49-89-636-59307; http:// wwwsolarpv.com. *LG*

ANSI Group Merges CAP, QAM Line Codes In RADSL Standard

The emerging rate-adaptive ADSL (RADSL) standard will support interoperation between both carrierless amplitude/phase (CAP) and quadrature/amplitude modulation (QAM) formats, according to a recent announcement from the Ad Hoc committee appointed by ANSI to study the matter. In an agreement between QAM advocate Broadcom Corp., Irvine, Calif., and CAP supporter GlobeSpan Technologies, Red Bank, N.J., the specification requires that receivers can handle both QAM and CAP signals to assure rapid and widespread adoption of this technology.

Interoperability is possible because they produce similar signal constellations. The only difference is that CAP has no carrier frequency, while QAM employs a carrier tone. According to the agreement, the first unit to transmit a signal determines whether CAP or QAM will be used for that connection. During the startup training sequence, the receiver will detect the presence or absence of a carrier signal and adjust itself to demodulate the appropriate signal.

RADSL can independently adjust its upstream and downstream data rates, according to prevailing line conditions. This permits telcos to install RADSL service without time-consuming and expensive line-conditioning procedures. The new specification defines data rates of up to 7 Mbits/s in the downstream, and upstream rates of up to 1 Mbit/s. Contact GlobeSpan at (908) 345-7500; http://www.globespan.net, or Broadcom at (714) 450-8700; http://www.broadcom.com. *LG*

Edited by Roger Engelke

summer UNITRODE HIGHLIGHTS

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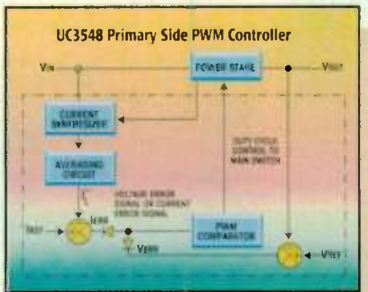
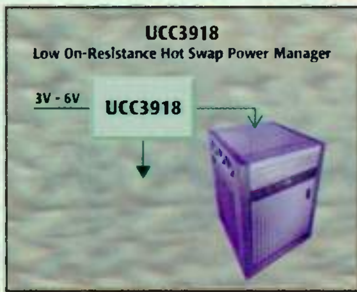


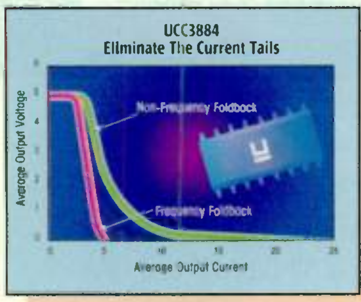
UC3548

The UC3548 is a unique primary side PWM controller. It is the first IC to combine the simplicity of voltage mode control during normal operation and average current mode control during overload or short circuit conditions.



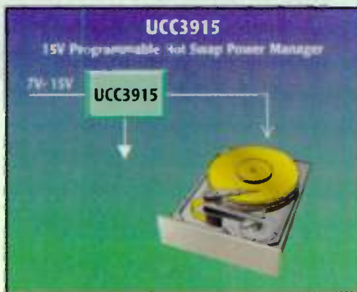
UCC3918

Operating at 3V to 6V, this programmable Hot Swap Power Manager™ Control IC is ideal for communication port, router, server, and disk drive hot swapping. Incorporating a programmable active current limit (0 to 4A) and on-chip power FET (60 mΩ), the device provides a complete hot swap solution.



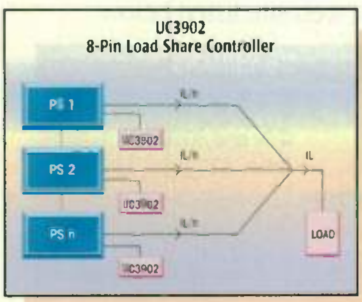
UCC3884

The UCC3884 is a high performance controller designed for high-frequency, single-ended converters. The device's frequency foldback feature decreases PWM frequency under overload conditions to reduce the average output current and to eliminate current tails.



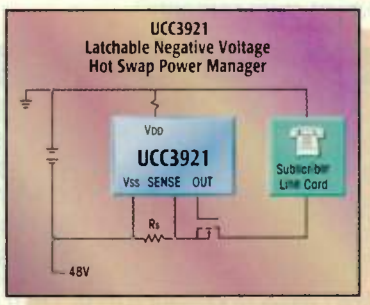
UCC3915

A member of the programmable Hot Swap Power Manager™ family, the UCC3915 operates at 7V to 15V and is ideal for communication port hot swapping and high voltage disk drive hot swapping.



UC3902

This simple-to-use, low-cost controller balances the output current of two or more independent, paralleled power supplies sharing a common load. System reliability is improved due to redundancy and lower thermal stresses.



UCC3921

Part of Unitrode's family of negative voltage Hot Swap Power Manager™ ICs, the UCC3921 provides complete power management, hot swap, and fault handling capability, while operating over the full -20V to -200V telecom range.

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MPEG-4 Standard To Allow Access To Individual Objects Within A Picture

Many design engineers rely heavily on the implementation of MPEG-1 and MPEG-2 solutions. Both video standards have enough features to make them very useful; however, they suffer from one big restriction—they both process rectangular pictures. The processing is performed blockwise, and the geometry of the blocks is fixed because the entire picture is divided by a grid into individual subpictures. As a result, the picture's content and the block geometry do not match, meaning that access to individual objects within the picture (such as a house, tree, or person) is not possible. MPEG-4, the latest standard, however, overcomes this limitation. Committee drafts of the standard will most likely be finalized by the end of this year.

"This content-based interactivity allows the interaction with objects within an audio-visual stage; currently, it is only possible with synthetic objects in the computer graphics area," says Dr. Ralf Schaefer, head of the image-signal-processing department, the Heinrich-HertzInstitut in Berlin, Germany. "Such an interactivity is planned to be extended to natural and hybrid synthetic objects to enable new forms of interactive audio-visual services."

A better encoding efficiency is said to allow "very low data rates," enabling the transmission of images over narrow-banded channels. Furthermore, MPEG-4 will allow the universal access to audio-visual data from different storage media over a variety of different networks, with a special focus on mobile networks. This feature requires special immunity to transmission errors and small bandwidths.

MPEG-4 will offer tools for content-related multimedia data access as well as the possibility to manipulate and edit data in a content-based manner at the bitstream level. It also will allow the coding of hybrid natural/synthetical stages, and offer an improved random-time access. Additionally, MPEG-4 also will allow scalability in different dimensions such as quality (local, timely resolution) and contents (priority of different objects in the picture) *(Table 1)*.

To allow users access to individual objects within a video-picture sequence, MPEG-4 video object planes (VOPs) support fundamental content-related functionalities at the decoder. Every VOP describes specific picture content, and is encoded in a separate VOP layer. A VOP may contain just one object. The decoding of all VOP layers enables the reconstruction of an original picture sequence in total. Single VOP picture content can be decoded and reconstructed separately by using the content-related scalablility.

This basic feature of the VOP structure allows the content-related manipulation of picture data at the decoder without a new transcoding. Practically, this means that there must be an algorithm which is able to determine individual objects within a picture. the algorithm also must follow these objects through a video sequence.

Imagine a picture of a house with a tree in front of it, a person running through the picture, and some blue sky with little clouds. You also might describe this picture by its different objects. Let's call the house and backround Object 1, the tree Object 2, and the running person Object 3. If you're only interested in the running person and his or her movements, you only have to decode Object 3. By bitstream manipulation, this object can be placed in front of a totally new background like the Great Salt Lake in Utah or the lush rain forests of Hawaii. This kind of bitstream manipulation at first resembles the well-known blue-screen technique.

At the Heinrich-Hertz-Institut, Dr. Schaefer showed some first examples of manipulations of pictures described by VOPs. He videotaped a TV moderator in front of a wall comprising operating TV monitors, and defined a binary "alpha-plane" mask describing the outline of the person. Even though the person was constantly moving, the outline followed the person. The next step was the exchange of the backgrounds. When the number of VOPs is limited to one, and the outline shape is determined to be rectangular, the preconditions for MPEG-1 and MPEG-2 are set. These older standards are included within MPEG-4.

Dr. Schaefer thinks that "a major number of MPEG-4 applications will be running on general-purpose signal processors with algorithms implemented in software," which would eliminate the need for dedicated hardware. Consequently, he says MPEG-4

CORE EXPERIMENTS OF MPEG-4

Kind of experiment	Techniques being investigated
Movement prediction	Global movement compensation, block partitioning, short-term/long-term picture memory, movement compensation with variable block size, 2D triangular mesh prediction, and sub-pel prediction
Texture coding in pictures	Wavelet transformation, matching pursuits, 3D DCT, overlapping transformations, improved intrapicture coding, and DCT coding with variable block size
Contour coding and alpha-plane coding	Gray-level contour coding, geometrical transformations, contour-adapative macroblock grid, and segmenting with blocks of variable size
Texture coding in arbitrarily formed picture segments (video-object planes)	8 by 8 DCT with pixel extrapolation, contour-adaptive DCT (SADCT), 8 by 8 DCT with pixel enlargement/interpolation, and wavelet/subband coding
Fault tolerance/ruggedness	Resynchronization techniques, hierarchical coding/structures, back-channel signaling, and error concealment
Scalability of bandwidth and complexity	Generalized time/spatial coding, and contents-related time scalability
Others	Bit-rate control, noise suppression, automatic segmentation, SPRITE generation, and stereo/multiview coding

TIME SCHEDULE FOR MPEG-4'S STANDARDIZATION

Title	Call for proposal	Working drafts	Committee draft	International standard draft	International standard
MPEG-4 systems description language (MSDL)		11/95-11/96	11/97	7/98	11/98
Synthetic natural hybrid coding (SNHC)	Submission: 3/96 Notification: 11/96	11/96-7/97	11/97	7/98	11/98
Video	Submission: 3/96 Notification: 11/96	1/96-11/96	11/97	7/98	11/98
Audio	Submission: 3/96 Notification: 3/97	11/96	11/97	7/98	11/98
MPEG-4 integration		11/96-7/97	11/97-3/98	7/98	11/98

will not be standardized the usual way where entire algorithms for audio and video decoding and system multiplexing were standardized in MPEG-1 and MPEG-2. "The target of MPEG-4 is mainly to standardize a set of tools for video encoding", he adds. "In order to stick to the MPEG-1 and MPEG-2 terminology such a video tool might, for example, be a DCT module or a module for movement compensation."

This means that the MSDL (MPEG-4 Systems Description Language) also will transmit the decoder's structure in addition to the traditional MPEG system requirements (multiplexing for audio and video) in the bitstream. So information about how to use the tools and how to interpret the bitstreams is transmitted to the decoder as well.

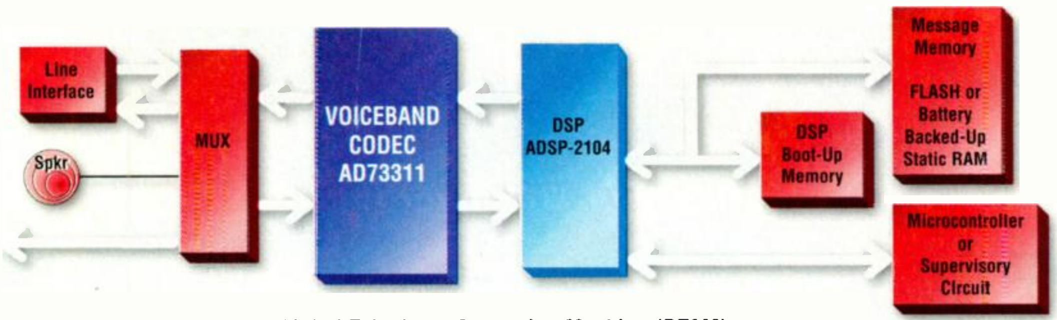
Currently, the MPEG-4 verification model is applied to pixel displays with YUV signal components in the 4:2:0 format where each pixel is quantized with 8 bits. The size as well as the form of the input pictures may vary according to the application.

With all of MPEG-4's working drafts completed, the next step is the formulation of the committee drafts which will be done later this year. The international standard draft, as well as the standard itself will likely be finalized by next year *(Table 2)*.

Contact Dr. Ralf Schaefer, Einsteinufer 37, 10587 Berlin, Germany; telephone: 49 3031 002560; fax: 49 3039 27200; e-mail: schaefer@hhi.de.

ALFRED VOLLMER

New Voice Codec Speaks Volumes In Consumer Applications.



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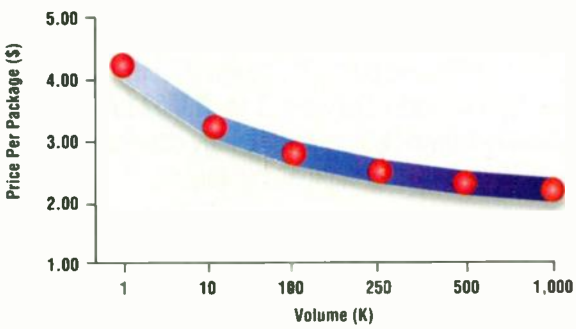

While integrated circuit conditioning helps overall system costs stay low on a 2.7 to 5.5 V single supply.

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Speedy 8-Bit Microcontroller Crafts Virtual Peripherals

With A 50-MIPS Throughput, This MCU Uses Software To Create Application-Specific Virtualized Peripheral Support Functions.

Dave Bursky

COVER FEATURE

Single-chip 8-bit microcontrollers solve many embedded control applications by inexpensively integrating many system control functions along with the processor onto a single chip. However, as system needs grow more complex, the silicon area of the microcontroller unit (MCU) also grows—often to the point of making the chip too expensive for the application. Furthermore, many of the application sub-tasks (counting, timing, serial and parallel communications, pulse-width modulation, etc.) do not demand the ultimate in CPU performance, but can usually be accomplished with a CPU that runs at a few megahertz, since on-chip logic supports those functions.

To lower the cost of the silicon, Scenix Semiconductor has a better idea. Instead of putting application support functions in hard logic, they use software to create virtual peripherals. Each support function is actually a software module that can be incorporated into the MCU's program storage memory. Modules are executed from memory when the functions they represent are needed. Thus, each function requires only a portion of the CPU's overall throughput, limiting the number of support functions a CPU can handle simultaneously. However, by using software, custom silicon development is eliminated in many cases. As a result, silicon costs and hardware turnaround time drop.

After analyzing support-function requirements, Scenix decided to develop the fastest CMOS 8-bit microcontroller—the SX. The chip can run at a clock rate of up to 50 MHz. With its one-instruction/clock execution rate, it can deliver a throughput of about 50 MIPS. The chip is designed to operate from supply voltages as low as 3.7 V, consuming just 12 mA at 50 MHz. The circuit, however, can operate over a supply range spanning the range of 3.7 to 6.25 V.

With such a high instruction throughput, multiple support functions that might require from several thousand instructions/s to several millions of instructions/s to implement, can execute on a time-sliced basis. The time multiplexing provides the appearance that they all simultaneously exist (*see the table*). However, sometimes additional hardware must be used due to resolution or speed requirements. High-resolution ADCs (beyond 10 bits), for example, are best implemented as separate chips because their integration with the MCU usually brings conflicting process requirements.

Overhead And Code

Just how much overhead and/or code do the virtual peripherals require? Not too much for some specific functions, and most of the CPU's capability for others. For example, code needed for an IR transceiver interface is about 170 words of EEPROM. This code requires about 5% of the 50-MIPS throughput, leaving about 45 MIPS for other tasks. An SPI/Microwire serial port takes about 50 words of storage and about 10% of the CPU throughput. A stepper-motor controller also requires about 50 words of storage, yet demands only about 2% of the CPU throughput.

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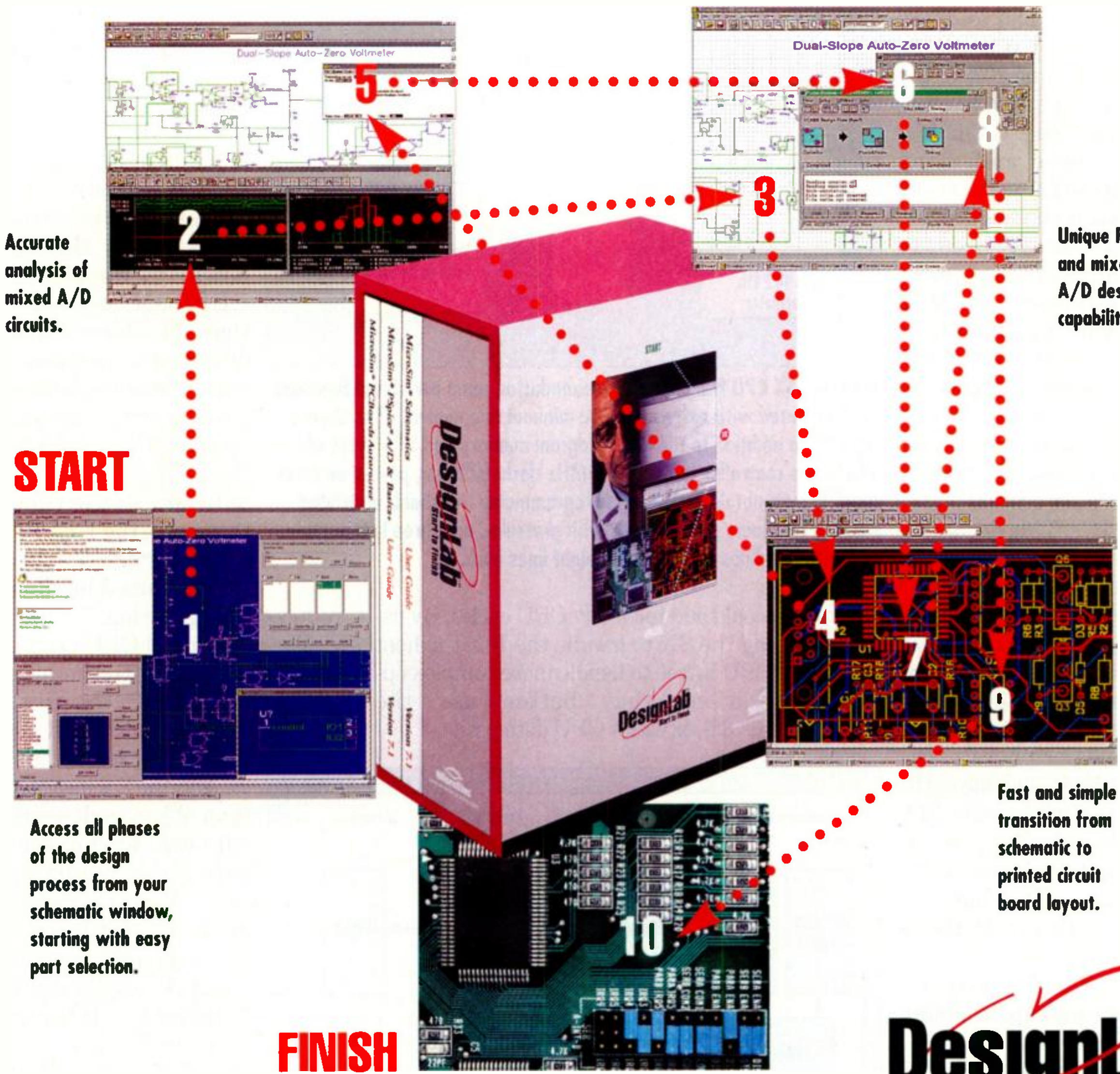

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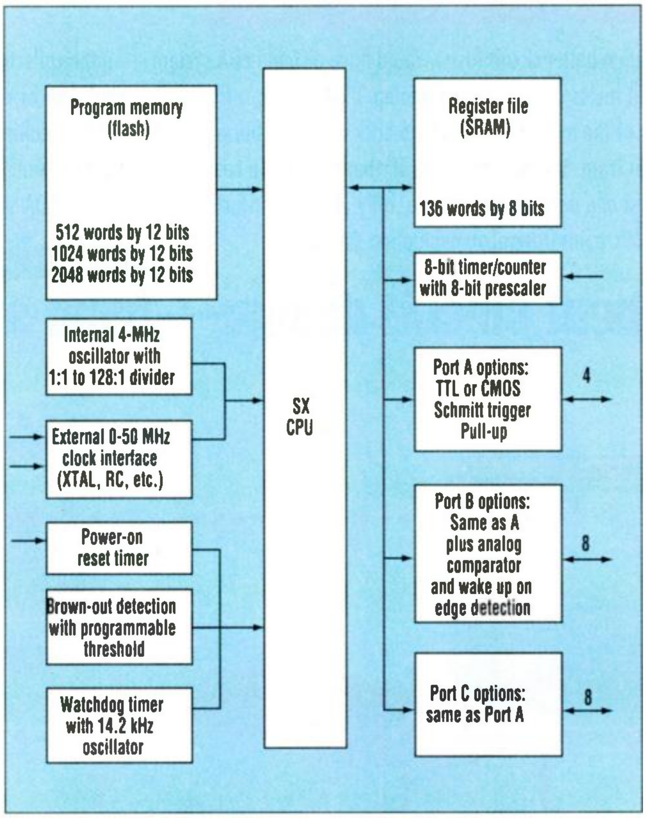
Popular functions such as a keypad scanner or LCD controller require only 70 or 120 words of code, respectively, but both consume just 1% of the CPU throughput. A full PC keyboard and mouse controller also would require about 80 words of code storage, yet the larger keyboard demands no more processing—just 1% of the CPU's throughput. More complex functions such as a 1200-baud modem or a music synthesizer require 280 and 180 words of code, respectively, but each consume 20% of the CPU's horsepower, leaving 40 MIPS for other tasks.

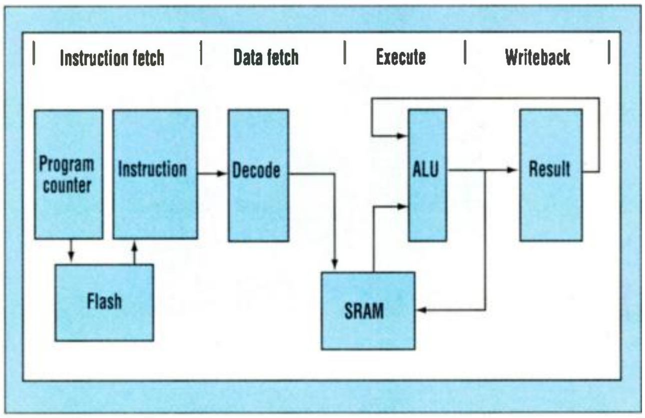
Since these and many other support functions can be implemented via software, the processor only needs to pack a minimal complement of on-chip support logic (*Fig. 1*). The wide operating voltage range, coupled with the on-chip brown-out detector, reset circuit, and watchdog timer eliminate the need for external circuitry such as voltage regulators and power monitor ICs. This design allows the MCU to run directly from batteries.



1. On the SX CPU from Scenix Semiconductor, most peripheral functions can be created with software and a minimal complement of hardware support. In addition to the flash program memory and 136 bytes of SRAM, the controller contains a 4-MHz clock oscillator, power-on reset timer, brown-out detection with programmable threshold, watchdog timer, 8-bit timer/counter with 8-bit prescaler, and three I/O ports—one with four lines and two with eight lines each.

Key to the processor's flexibility is the high-speed 8-bit CPU core. It runs at 50 MHz, and has three programmable I/O ports (one 4-bit and two 8-bit ports) that can be used to implement the virtual peripherals. The 4-bit port (RA) and one of the 8-bit ports (RC) provide TTL or CMOS interface levels with Schmitt-trigger inputs and pull-ups on the outputs. The other 8-bit port (RB) has the same features, but also includes an analog comparator and a wake-up capability on edge detection.

The minimal feature set will keep the chip cost low. They also will allow it to serve as a low-cost addition to an embedded PC or RISC system. In this way, the chip would provide the I/O functions that don't make economic sense to integrate into the host CPU, or would add too many CPU cycles. By using the SX to handle the I/O, the host CPU is free to handle more complex operations that better use the 16-, 32-, or 64-bit CPU data path.



2. A four-stage pipeline is used for the 8-bit CPU core in the SX microcontroller. The simple pipeline includes an instruction-fetch stage, data-fetch stage, execute stage, and write-back stage. This arrangement allows the CPU to achieve a throughput approaching 50 MIPS when clocked at 50 MHz.

On-chip memory consists of a 136-byte static-RAM-based register file, and a choice of either 512, 1024, or 2048 12-bit words of nonvolatile, flash-based program memory. The decision to use flash memory was critical in light of the performance objective—memory access times of just 12 ns, 3.7-V operation, and a 10,000-write-cycle endurance. The EEPROM also is in-system programmable. Consequently, a separate external programmer is not required for updates.

To implement the high-speed flash, designers at Scenix developed a new, asynchronous flash-EEPROM structure. Address transition detection also helps lower the memory power by deselecting the EEPROM between cycles. Once the address stabilizes, a differential sense amplifier with a bias in the linear region is turned on and fully saturated. Consequently, the flash EEPROM is enabled only 60% of the time. Furthermore, the EEPROM has a high signal-to-noise ratio with reduced loading and a reduced voltage swing.

The high-speed CPU structure on the chip is similar to the Microchip PIC architecture, the first 8-bit processor to employ a RISC-like pipelined architecture (*Fig. 2*). And the SX instruction set is an object-code-compatible superset of the Microchip PIC 16C5x family instructions. However, at the assembly mnemonic level, the SX also supports an opcode format previously defined by Parallax Inc. Designers can select whichever they prefer since it's a simple matter to perform the 1-for-1 translation between the mnemonics.

In The Pipeline

To keep the pipeline simple and fast, there's no fancy interlock hardware, nor software delay slots that waste

code space. In the pipeline are the instruction-fetch-and-decode stage, the operand-fetch stage, the instruction-execute stage, and the write-back stage. Once the pipeline is full, a complete instruction can be executed every clock cycle.

By relying on a streamlined four-stage pipeline with a Harvard-style memory structure, and employing extremely fast (12 ns t_{ACC}) on-chip instruction and data memories, the SX can run at 50 MHz and execute almost any instruction in a single clock cycle. One exception, though, are Branch operations. They require three clock cycles and simply annul (replace with a no-op) the two instructions that follow the Branch command. With a 20-ns instruction cycle, the chip packs enough punch to deliver about 10 times the performance of popular 8-bit MCUs from other suppliers. And, even when running with the low-speed 4-MHz internal oscillator, the SX delivers a higher throughput than a 40-MHz 8051-type MCU.

Although the MCU can run at 50 MHz, it doesn't have to, thanks to the use of static logic in the MCU's circuits. The chip can run at any frequency below 50 MHz (even stopped) without data or state loss. With the lower frequency comes the associated reduction in power consumption due to the CMOS logic. Designers can take advantage of the on-chip 4-MHz oscillator, for instance, since it offers eight programmable division ratios, from 1:1 to 128:1. The on-chip oscillator, reduces system cost, board space, and electromagnetic interference.

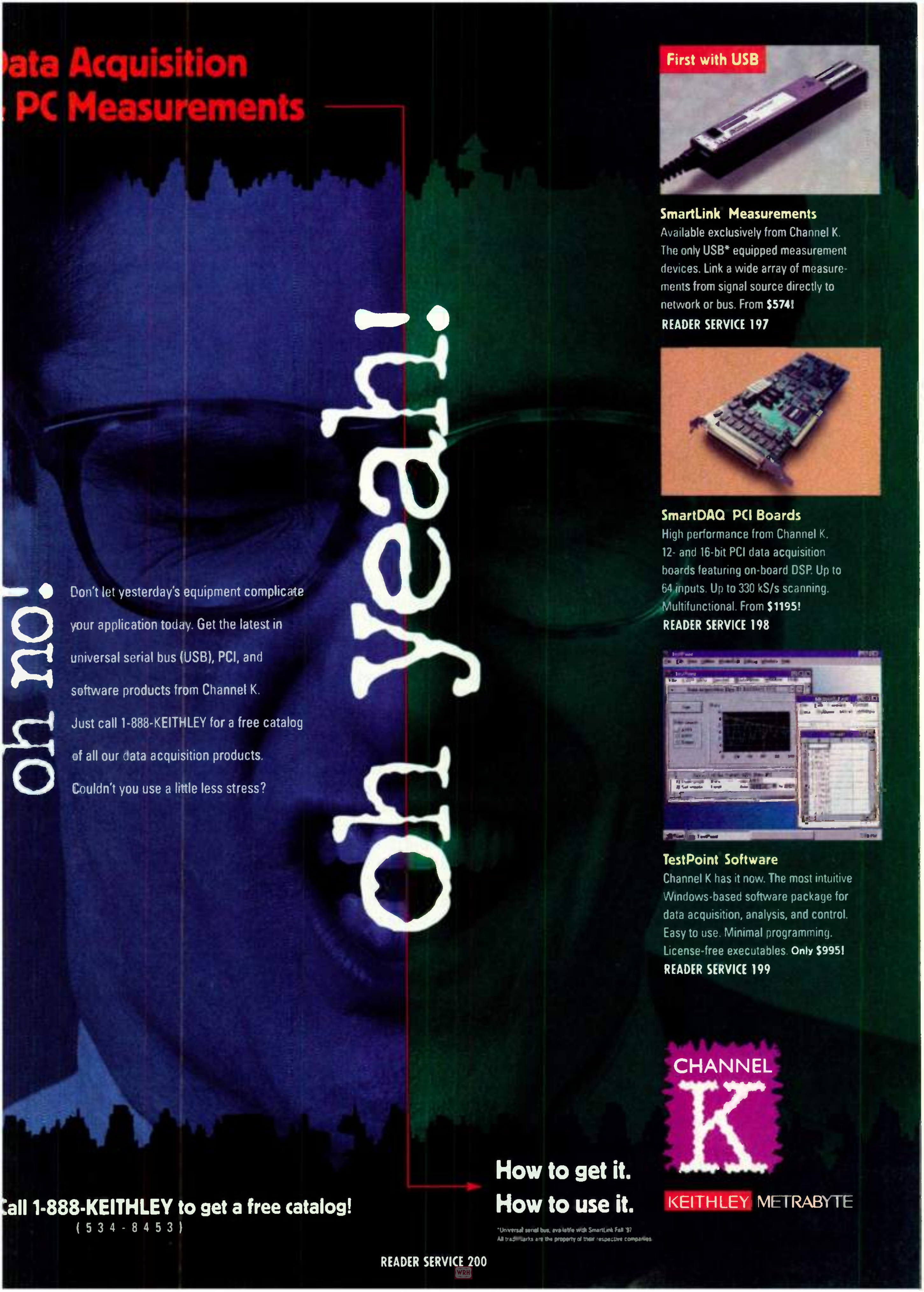
The 12-bit-instruction word width also is very efficient—it allows both the opcode and the operand in the same instruction. Additionally, the partitioning of the word between the opcode and operand is flexible, permitting maximum code density. And, to further optimize access to all the I/O features, 11 special-purpose instructions were added to speed common operations and reduce code size. For example, an additional carry-flag mode that works in conjunction with a carry-bit in the CPU significantly accelerates multibyte numeric calculations. It also yields performance approaching that of MCUs that have costly hardware multipliers. Additional enhancements include a Bank instruction that switches execution to a new register bank and a Page instruction that switches the CPU to a new instruction page. Other new instructions deal with I/O mode bits and returns from interrupts.

Speedy Interrupts

The processor's high performance also gives it a very short response time to interrupts. The interrupts can be generated by a built-in timer or external-pin edge detection. By exploiting deepened and dedicated hardware stacks, the SX guarantees response times of just three cycles (60 ns) for internal timer interrupts and five cycles (two extra for synchronization) for external inputs (100 ns total). One-level special hardware stacks automatically store critical registers during an interrupt and restore them upon return. That dedicated support lets the MCU quickly switch tasks to

VIRTUAL PERIPHERAL CODE AND PERFORMANCE NEEDS

Peripheral function	EEPROM words	Percentage of 50 MIPS	Remaining MIPS
Dc-100-kHz frequency generator	30	4%	48
Dc-100-kHz frequency measurement	40	5%	47.5
100-kHz background timer	30	2%	49
I^{2}C master	50	6%	47
I^{2}C slave	80	3%	48.5
Keypad scanner	70	1%	49.5
PC keyboard and mouse controller	80	1%	49.5
IR transmitter	60	2%	49
IR receiver	110	3%	48.5
LCD module	120	1%	49.5
Dc-100-kHz resonance loop	130	10%	45
19.2-kbit/s serial UART	60	3%	48.5
Centronics parallel port	30	1%	49.5
500-kHz SPI/Microwire	50	10%	45
Dallas microwire serial port	130	3%	48.5
DMX-512	100	8%	46
X-10	60	1%	49.5
Video controller	130	20%	40
DRAM server	40	3%	48.5
Switch-mode power-supply controller	30	4%	48
Networking	130	5%	47.5
Music synthesis	180	20%	40
20-kHz 8-bit PWM output	30	10%	45
D-Σ ADC (1 kHz/8 bit; 4 Hz/16 bit)	50	10%	45
Dc-100-kHz spectrum analyzer	150	7%	46.5
DTMF I/O	120	10%	45
Caller ID	180	10%	45
300/1200-baud modem	280	15%	42.5
Speech synthesis	300	20%	40
Stepper-motor sequencer	50	2%	49
250-kHz quadrature encoder	40	10%	45
Servo loop	170	10%	45
PID loop	160	10%	45



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implement virtual peripherals or execute application code specific to service that interrupt, all while executing code for other tasks.

Most older MCUs only interrupt tasks at instruction boundaries. In RISC processors, this limitation can be somewhat unpredictable because instruction lengths and the number of clock cycles required for the instruction change depending on the instruction. As a result, interrupt responses are slower than those with the SX RISC processor. The slow response also may introduce jitter into system timing, which ends up forming a fundamental limit on system performance and accuracy. In contrast, the SX's response to interrupts is much more predictable and repeatable.

Versatile Interfacing

The chip's I/O lines also incorporate the latest interface technologies, giving designers a flexible set of lines. All I/O pins are individually programmable as inputs or outputs, with or without 20-kΩ pull-up resistors. Inputs offer selectable TTL or CMOS levels with optional Schmitt triggers. Every output can sink or source up to 30 mA. The four pins on the 4-bit port (RA0-3) include symmetrical drive characteristics that permit the SX to easily drive inductive loads, which require equal push and pull (speakers, ultrasonic transducers, etc.). Additionally, three lines on the 8-bit RB port (RB0-2) can optionally connect an internal analog comparator to external signals. Furthermore, eight of the pins can be configured as external interrupt inputs. Besides redirecting program flow in response to external events, these inputs can wake up the chip from a power-down mode.

On-Board Emulation

To ensure the SX controller is properly configured, built-in, in-circuit emulation circuits allow designers to use the standard SX chip to debug software and hardware operations, as well as program the on-chip flash memory. No special bond-out chip or complex tools are required, thereby lowering development cost. The approach combines the best of traditional ROM monitor and newer remote-debug schemes, and is tailored to the SX's specific characteristics.

Since the SX is flash-based, it overcomes the single-chip-only dilemma—the application program can be repeatedly modified and downloaded into the chip along with a tiny debug kernel. To minimize memory consumption, the kernel handles only the bare minimum of functions needed to control the MCU (read and write instruction memory, go, and stop). All higher-level debug and human interfaces are performed on a host PC. The CPU's static nature also allows for true hardware single stepping or slowing of execution speed.

The low-pin-count packages planned for the SX (18, 20, or 28 leads) also limit the number of pins that can be dedicated to the background debug or a JTAG-like test port. To overcome the pin limitation, programming and debug operations take place over two clock pins (OSC1 and OSC2). This design works because these pins usually serve no application function other than clocking the CPU. That avoids any conflicts between the active I/O lines and the debug signals.

To ease software development, Scenix created the SX development system. It includes an assembler, an in-circuit development tool that also doubles as a programmer and debugger, a demo board, and two sample parts. The kit is available from Parallax Inc., Rocklin, Calif., (916) 624-8333, and sells for $249. Parallax also is developing a Basic compiler for the SX that will include an assortment of predesigned virtual peripherals. The compiler and peripheral library will be available as an upgrade in the fourth quarter for $99. Byte Craft Ltd. also is developing a C compiler and assembler for the SX. The company can be reached at (519) 888-6911.

PRICE AND AVAILABILITY

The SX microcontroller with 2 kbytes of EEPROM sells for $2.98 apiece in lots of 10,000 units. Samples will be available in September and production quantities will be available in the late fourth quarter.

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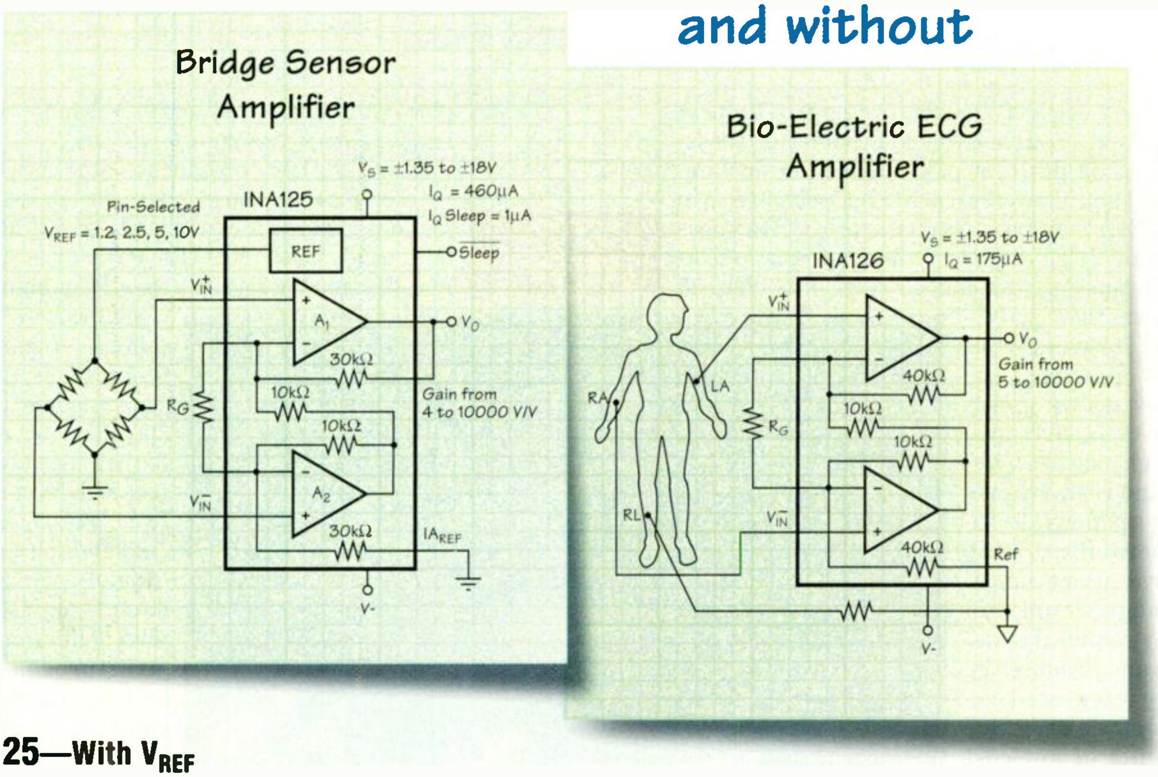

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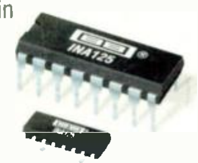

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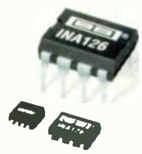

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802.11 Wireless LANs: A Blueprint For The Future?

After Overcoming Many Obstacles, The IEEE's Newest Specification Awaits Final Approval. This Could Slash The Cost Of Wireless Data And Pave The Way For Future RF- and IR-Based Networks.

Lee Goldberg

SPECIAL REPORT

After a long and often frustrating development period, the IEEE's 802.11 committee has issued the final draft of its specification for wireless local-area networks (LANs), and submitted it to the IEEE's main body for final approval. If all goes well at the IEEE Standards Activity Board Meeting, we can expect to see the release of a published document this September. If its window of market opportunity has not passed, the spec's completion could signal the beginning of a wireless land rush. By providing a pathway for interoperability, chip makers can now commit the huge chunks of money required to develop and produce the highly integrated circuits that will be the core elements of low-cost wireless data systems.

Even though the ink is still not completely dry on the 500+ page document, the changes that might occur at this point are small enough that many manufacturers are already rushing to build products to meet its specifications. The resulting chips, boards, and modules will allow designers to pick and choose the portions of a wireless system, if any, they wish to engineer themselves. This will not only accelerate their product's time-to-market, but also allows them to concentrate more closely on the details of their intended application.

Art Courtesy: Raytheon Semiconductor

Electronic Design has extensively covered the development of the 802.11 standard, but we thought it might be a good idea to give you a quick refresher course and bring you up to date on recent developments. Later, we'll finish up this report with a look at what the future holds for 802.11 and other wireless LANs. And, if you still want more information, refer to the June 26, 1995 issue of *Electronic Design* to explore additional details of 802.11's inner workings (*see the references section for details*).

One of the best things about 802.11 is its flexibility. For example, the standard encompasses wireless data transmission using both RF in the 2.4-GHz band, and diffuse IR energy over 850 to 950 nm. To comply with the Federal Communications Commission's (FCC's) requirements, the RF interface uses spread-spectrum modulation, with specifications provided for both frequency-hopping and direct-sequence techniques. Some of this flexibility is the product of intense wrangling between "control freaks" who believe in rigidly structured networks, and members of the committee more inclined to letting users define as much of how they use a system as possible. As a result, there are provisions within the spec that allow two or more devices to establish a simple peer-to-peer network on an "ad hoc" basis, or to attach themselves to a centrally controlled wired or wireless LAN infrastructure.

This allow you to roam across a building or campus and access all your e-mail, Internet connections, and critical files from your laptop (*Fig. 1*). Equally important, the ad hoc feature lets you and your friends set up impromptu electronic workgroups in an airport lounge, a sunny meadow, or wherever else you happen to be.

Physical Facts

At the physical level, the standard specifies parameters that allow unlicensed operation within North America per the FCC's regulations, specified in Document 15.247, part 15. It allocates 83

MHz of spectrum in the U.S., beginning at 2.4 GHz, with a maximum output power of 1 W. It also contains frequency and power specs that allow operation in compliance with regulations in Europe, Japan, Spain, and France.

Spread-spectrum modulation using both direct sequence (DS) and frequency hopping (FH) transmission techniques are employed to provide some level of noise immunity, and to minimize interference with other unlicensed applications. For infrared systems, a 16-value pulse-position modulation scheme is employed to transmit data at 1 Mbit/s while an enhanced version supports 2 Mbits/s. Using office ceilings as reflectors, the IR systems achieve a range of about 10 meters.

The direct sequence system uses differential binary phase-shift keying (DBPSK) modulation for data transmission at 1 Mbit/s, shifting to differential quadrature shift keying (DQPSK) to support a 2-Mbit/s rate. An 11-bit Barker sequence is used as the DS spreading code against which the data is modulated (*Fig. 2*). Besides spreading the transmission across a wide spectrum to resist interference, the Barker code's unique property of having a low correlation coefficient unless it is precisely aligned (in time) lets the receiver lock on to a very weak and noisy signal. The receiver thus enjoys an additional 10 dB of "processing gain." Unfortunately, the current spectrum allocation scheme does not permit use of a longer spreading code that could further enhance noise immunity.

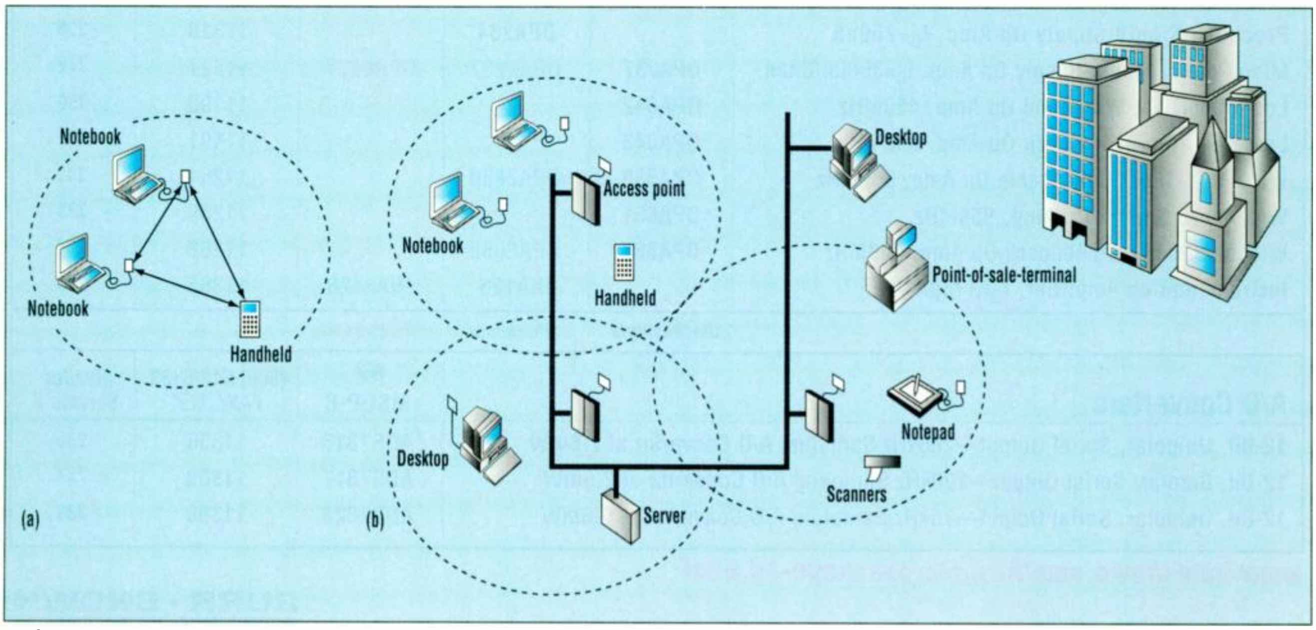
The 802.11 spec's frequency hopping provision employs 2-level Gaussian frequency shift keying (GFSK) for 1-Mbit/s operations, and 4-level GFSK when transmitting at 2 Mbits/s. The 83-MHz band is broken up into 79 1-MHz channels, which the radios hop between at a minimum rate of 2.5 hops/s. There are 22 orthogonal hop patterns that are defined as sequences that minimize the chance of 2 or more networks "bumping into each other," even if they are operating in the same office. This allows wireless to LANs increase their capacity by distributing traffic across several of these hopping "channels."

There's still a heated debate going on between FH and DS advocates as to which system is better. Conflicting claims are being exchanged about performance, noise immunity, and spectral efficiency, with each party waving reams of "conclusive evidence" to back them up. The only definitive thing that can be said at the moment is that most of the research for implementing faster data rates beyond the current 2-Mbit/s limit are centered around DS technology. For an informative look at both sides of the DS/FH debate, you might want to get a copy of the Jan. 1997 issue of *Wireless System Design (see the references section for details).*

802.11 data is carried within a highly modified Ethernet packet structure that has some additional control and error-recovery features to help it cope with the rigors of the wireless environment (*Fig. 3*). Part of the packet's header is devoted to a synchronization sequence, giving the receiver a known string of bits to lock on to.

The header also includes a short string of bits that specifies the speed at which the payload will be transmitted. Space has been reserved within this string for the higher data rates (10 Mbits/s or more) that should be available within the next few years. To ensure backward compatibility with all 802.11-compliant units, the header is always transmitted at the slower 1-Mbit/s rate. While this incurs a slight performance penalty, it allows slower and faster radios to interoperate, as well as negotiate the highest data rate they can mutually support.

Besides handling PHY-layer chores, the frame's header also plays a crucial part in coordinating network media access control (MAC) functions. The wireless MAC shares most of the concepts used in the original Ethernet shared-media protocols, where two or more devices hang off the same twisted-pair or coaxial cable, but it has been significantly modified to cope with problems not found in a wired environ-



1. The IEEE 802.11 standard for wireless LANs supports peer-to-peer "ad hoc" nets, and more traditional centrally controlled wireless nets. In an ad hoc environment, each terminal communicates directly with any other net member. The same terminals can associate with an access point (AP), which gives them access to the LAN's wired infrastructure in the building, campus, or area. With AP control, all LAN communications are directed through the AP.

ment. For this reason, 80.11's MAC is the most complex protocol in the 802.x family of standards.

The MAC Three-Step

To keep everybody from talking at once, most 802x wired flavors use carrier-sense, multiple-access, collision detect (CSMACD). In CSMACD, a transmitter listens before talking. After waiting for a clear channel, it then transmits its data while checking the line for an abnormal voltage that indicates another unit started to talk at the same time. If a collision is sensed, both parties "back off" the channel, and set a timer with a random delay that must pass before they try to transmit again.

Since a collision is much harder to detect in a wireless environment, 802.11 employs a set of rules known as carrier-sense, multiple access, collision avoidance (CSMACA). As with wired networks, a transmitter does its best to listen for a time when nobody else is on the air before talking. Instead of transmitting its entire message, however, the sending station first issues a short request to send (RTS) message that gives the transmitting station's address, the destination address, and the type of data to be sent. Also included is the network allocation vector (NAV), which indicates the length and number of packets waiting to be sent.

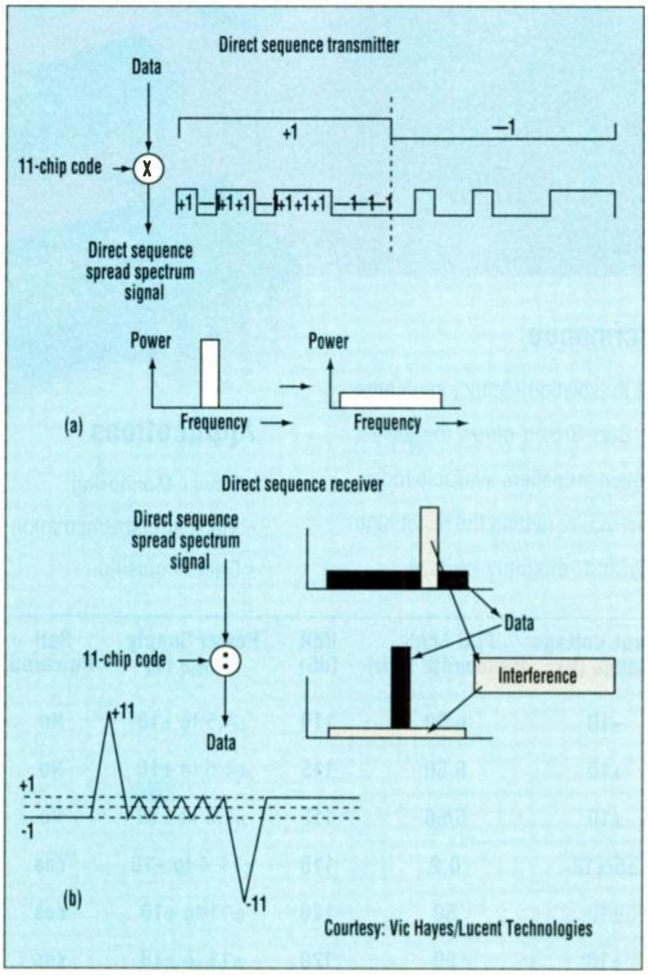
If the receiving station gets the RTS, it issues a clear to send (CTS) message, which echoes the addresses and the NAV. The message's main body is then transmitted, followed by an acknowledge (ACK) from the receiver after each packet, if it was received properly. If the receiving station fails to issue a CTS or ACK, the transmitter is obliged to go back to square one and begin all over again.

While seemingly time-consuming and wasteful of bandwidth, the little dance of RTS/CTS/ACK is essential to ensure that data transfers happen with as little interference or dropped bits as possible. Having both transmit and receive stations positively acknowledge each other and state the amount of time they intend to use the channel helps ensure that other stations within earshot will not interfere.

This two-way handshake also cures what is known as the "hidden node" problem, where a station on the LAN's far side might not hear a distant neighbor as it tried to talk to an access point located part way between them. For short exchanges (under 100 bytes), the protocol does allow the data to be sent in a modified RTS frame without a CTS, eliminating some of the overhead.

The MAC and its CSMACA protocol was developed some years ago, but has undergone some recent tweaking by the committee, prior to release of the final draft. Whereas the standard originally called for a fairly sophisticated (read "expensive to implement") method for clear channel assessment, the latest version allows a transceiver to check for radio traffic using detection of RF energy levels, carrier sensing, or both. The time-out provisions called for by earlier versions has been eliminated.

Once the connection is set up, a frame is transmitted much like in a wired network. While it can be shorter, a frame's maximum size is 2312 octets (802.11 folks hesitate to use the word "byte" because the frame can contain binary data in any form). The frame's header contains the traditional 48-bit MAC addresses for source and destination, plus two more address fields to accommodate connections to APs. Also included is a tag that indicates the type of data being carried, the speed it will be transmitted at (currently 1 or 2 Mbits/s), and several other pieces of information required for controlling traffic in a wireless environment. A 32-bit frame check sequence (FCS) code follows the data frame to insure its integrity.



2. In direct sequence (DS) spread-spectrum modulation, an 11-bit "chipping code" is combined with a single data bit in a baseband mixer (a). The resulting product "spreads" signal energy across a large piece of spectrum, making it more immune to narrowband transients. A DS receiver has a despreading function that uses the same chipping code to correlate the incoming signal and extract the modulated data from background noise (b).

Pretty Good Security

The idea of a wireless data network inevitably raises concerns about privacy and security. Thankfully, the 802.11 committee has devoted much time and effort to providing technologies that offer at least as much protection against uninvited eavesdropping as a traditional wired Ethernet network. Known as wired equivalent privacy (WEP), it employs a 40-bit seed key and the RC4 encryption algorithm.

When enabled, WEP only protects the data-packet contents, leaving the physical-layer header unencrypted. This is necessary to allow all the nodes on the network to share NAVs, control signals, and other information required to interoperate with each other.

While WEP should be adequate for most applications, additional layers of encryption can be easily added to the upper layers of the protocol.

Sufficient provisions have been made to allow 802.11 to support a wide variety of encryption/privacy schemes.

A separate arrangement permits secure registration and authentication. When a node wishes to associate with the network, it waits for an opening in the traffic and issues a request for authentication. The network responds by sending out a block of random text to the potential user's node. The node takes this text string and encrypts it, using the network password as a cipher key, and sends it back to the network for authentication. This prevents the password from being exposed to the less-than-tender mercies of potential intruders.

Octets	2	2	6	6	6	2	6	0-2312	4
	Frame control	Duration/ ID	Address 1 - destination or AP address	Address 2 - source or AP address	Address 3	Sequence control	Address 4	Frame body (data)	Frame check sequence

3. An 802.11 data frame begins with a 2-byte frame control block which lets the system know the kind of data in the frame and at what speed it will be transmitted, followed by a duration/ID word and source and destination addresses. Two additional address blocks are reserved for communication between terminals.

Two Ways To Network

As mentioned earlier, a network can be established as an ad hoc affair, with nodes simply hopping in whenever they have something to say. This is quite useful in many situations, where a few people need to exchange files, coordinate schedules, or collaborate on a project in an area far away from a centrally wired backbone. In higher traffic situations with many users, a more centrally coordinated approach is needed. 802.11 provides a protocol for routing traffic through an access point (AP). When an AP is in use, all traffic in the area is routed through it, whether it is messages between mobile terminals or the wired portion of the LAN.

Because of bandwidth and complexity restrictions, the 802.11 specification is not really intended to support high-density, real-time multimedia applications. It does, however, contain limited provisions for carrying some time-bounded data, such as voice, while using synchronized time slots. The time slots are available when an AP activates an optional centralized control mechanism known as the Point Control Function (PCF). The PCF is a mechanism that ensures that all players on the network get their fair share of the channel's limited bandwidth in an efficient manner.

The PCF allows the stations under its control to communicate in two different ways. It creates a time window known as a "contention-free period," during which each radio is allowed to use the channel for a specific slice of time. The PCF steps through each registered node, ensuring that everybody gets a turn. Units that have nothing to say are passed by, allowing them to be powered down to conserve battery life. If the PCF does not hear from a node within a certain number of cycles, that node is dropped from the "active list" and is no longer polled.

The contention-free interval is followed by a "contention period." During this period, individual transceivers can jump in and vie for extra bandwidth. The contention period also is the time during which new transceivers can announce their presence and register themselves with the network. In addition, network nodes that have been inactive for long periods also can use this time to reclaim their time slot in the contention-free period.

Current estimates are that a single wireless LAN using PCF can support up to four full-duplex, line-quality voice channels. The use of advanced compression techniques may increase this number in the future.

Faster, Better, Cheaper

The release of this long-awaited specification should give rise to a larger market for wireless data products. This also should fuel the engineering required to cut production costs to consumer-friendly levels.

Brian Mathews, marketing manager at Harris Semiconductor's Wireless Products Group, predicts that we will see wireless LAN cards introduced with a retail price ranging from $300 to $350 before the end of this year, with products in the $200 range appearing after the second quarter of 1998. Several companies also are planning to introduce lower-cost consumer-grade wireless data products that use a subset of 802.11's features.

802.11's architects wisely chose to get their standard out into the world as quickly as the committee's contentious politics would allow. For this reason, several key issues, including roaming protocols and higher data rates, have been left for resolution at a later date. The current standard has space reserved within its header to specify faster data rates, but they have not been defined as of yet.

There is currently an initiative underway to develop a faster PHY, with two technical proposals jockeying for an inside track in the approval process. The leading contender is an 11-Mbit/s DS scheme submitted by Harris, which uses M-ary orthogonal keying. In plain language, this means that it uses several orthogonal, or non-overlapping, spreading codes simultaneously to multiply channel capacity.

Running second is Bell Labs' proprietary scheme that uses pulse position modulation (PPM), and is rumored to support 8 to 10 Mbits/s. It is a variant of the original 1-Mbit/s DS modulation method, but instead of having a fixed symbol period, the PPM scheme overlaps some symbol periods. This code shifting varies the time between autocorrelation peaks, allowing the detection of eight distinct pulse positions within the 11-chip symbol. By implementing PPM on both the I and Q channels, 64 distinct states can be achieved, providing eight bits worth of encoding during every symbol period (8 Mbits/s total). Lucent's technologists are attempting to bring it up to a full 10 Mbits/s by adding some sort of quadrature amplitude modulation (QAM) to the signal.

Of course, speed comes with a price. In this case, it will be a significantly reduced range (200 feet or less, versus the 500 to 1000 feet typically found in 1- to 2-Mbit systems). Both modulation techniques also will have somewhat reduced noise immunity. Since their coding schemes are at least partially amplitude-based, they become much more susceptible to spurious RF energy that

occurs within their operating range.

The issue of how mobile units roam between access points was also left open in the original 802.11 standard, but an initiative is under way to address this. An alliance sponsored by Lucent Technologies, Aeronet Wireless Communications, and Digital Ocean has developed a protocol known as the inter-access point protocol (IAPP), which will allow network access points to communicate with each other via the network's wired backbone. Control signals and information about a mobile terminal could be exchanged between access points, allowing smooth hand-offs as it roamed across a building or campus. It has been designed to work in concert with both the 802.11 wireless protocol and all other 802.x wired protocols.

A preliminary version of the IAPP standard has been issued, with the sponsoring companies currently developing products around it. Submissions to the IEEE for incorporation into the 802.11 standard is still under discussion. However, since it sits much further up on the protocol stack, it is beyond the scope of the committee's original charter. For more information on the technical aspects of the IAPP, call Lucent's technical hotline at (800) ATT-WAVE.

5 MHz And Beyond

Last year's allocation of spectrum in the 5.2-GHz band for what is now known as the National Information Infrastructure (NII) has caused increased interest in horizontal wireless data applications. Theoretically, the unlicensed NII (U-NII) band could be used to link students' laptop computers to a school's central network, or let a traveler access maps, directories, and Internet connections at airports, hotels, and even street corners.

At the present time, however, no firm decision has been made as to which technology will be used to implement these services. The two primary technology candidates for the job are the European HiperLAN II standard and a slightly modified version of the 802.11 specification.

The IEEE's 802.11 working group is preparing to define a new PHY layer for the U-NII band, using as much of the original 802.11 MAC as possible. A 5.2-GHz version of 802.11 probably would have slightly wider channels (using 10 to 20 MHz of bandwidth to transmit 20 Mbits/s) and not be obligated to use the spread-spectrum modulation required by the FCC for the 2.4-GHz band. Because of the 802.11 committee's mature body of work, and its proactive response to the U-NII development process, it stands a good chance of being chosen to develop the blueprint for this next-generation standard.

It's a good bet that the higher cost of 5-GHz radio components in the first generation U-NII transceivers will make their price 25 to 50% higher than their 2.4-GHz counterparts. This differential could shrink rapidly, however, as demand fuels competition and technological innovation.

Words Of Caution

It's customary to close a forward-looking technology story such as this with some cheerful babble about a rosy wireless future, or something to that effect. In this case, it's also important to explain that there may be a few potholes in the road on the way to a wireless nirvana.

The actual approval and release of 802.11 is still up in the air at the time this article is going to press. While everything looks good for final approval, it's not a sure thing. Despite all the hard work and good intentions on the part of most of its members, the committee's open-door, consensus-based policy has made it vulnerable to last-minute disagreements that have held up the standard's progress for months at a time. We can only wish them well on the home stretch, and keep a close watch on their web site (*http://stdsbbs.ieee.org/group/802/11*) for the latest developments.

During the course of researching this article, several sources cautioned about some manufacturers claiming "802.11 compatibility" ahead of the actual release of the standard. Depending on the product, this can be a big or little issue.

When designing a product to a specification as complex as 802.11, there is always some margin for interpretation and/or error that can make it deaf and dumb to similar units from another manufacturer. Mike Jones, vice president of the Wireless LAN Alliance Forum, estimates that if the 802.11 committee stays on schedule, it should be some time in early 1998 before manufacturers are actually producing interoperable products.

Even if the standard does not change from its current form prior to approval, it will be some time before extensive interoperability testing between products from different manufacturers will be complete. The kinds of testing required for a carefully engineered product should be fairly subtle, such as the duration and timing relationships between various signals or functions. Nevertheless, make sure that the components you select have enough programmability in them to permit the updates, adjustments, and tweaks required to allow you to achieve true interoperability.

The author wishes to acknowledge Vic Hayes of Lucent's WaveLAN Division, and chair of the 802.11 committee, as well as Tom Tombler and Carl Andren from Harris Semiconductor's Wireless Products Division, for their invaluable assistance in preparing this and other 802.11-related stories.

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The IEEE 802.11 Committee's web site: *http://stdsbbs.ieee.org/group/802/11.*

The Wireless LAN Alliance web site: *http://www.wlana.com.*

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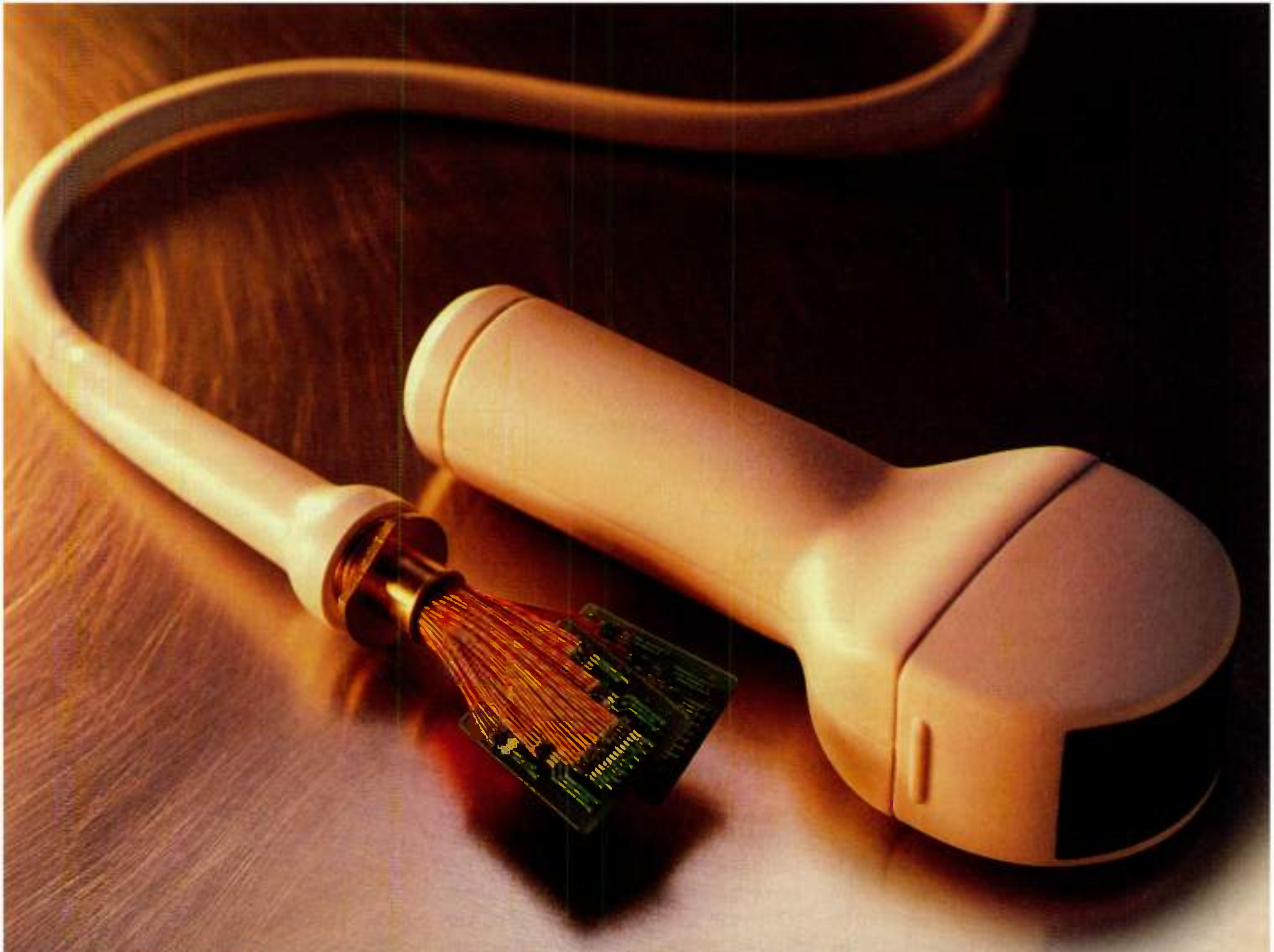


UPDATE ON BUSES

The Universal Serial Bus Is Ready To Take Off As Components And End Products Hit The Street

The Universal Serial Bus (USB) has arrived and is ready for boarding. After about two years of defining the specification and product design, components and end products are hitting the street. The USB offers a simple connection of up to 127 devices, a bus bandwidth of 12 Mbits/s, and a 500-mA maximum current supply. Peripherals can draw power directly from the bus, meaning that peripherals can be built with a single external cable.

Most of the PCs now shipping contain a pair of USB ports. The only missing link is in the operating system. The latest release of Windows 95 contains the USB drivers, but that operating system isn't available in a retail form. It was released by Microsoft in an OEM version, meaning that systems can be sold with the software preloaded if the manufacturer was using the latest operating-system version (called OSR2.1).

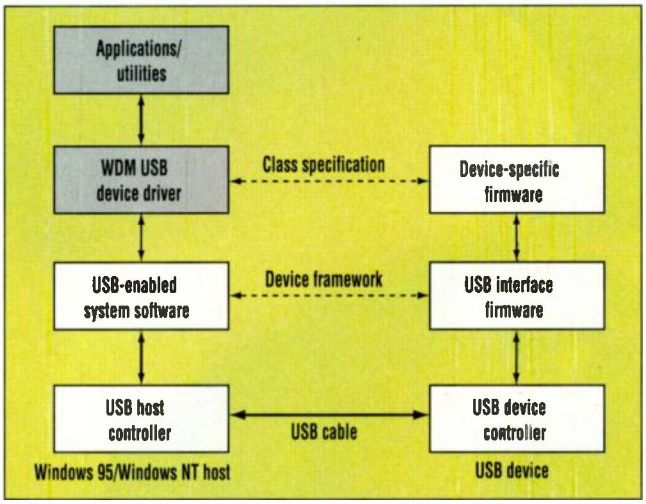
On the component side, Lucent Technologies, Berkeley Heights, N.J., developed its Instant USB USS-720 application-specific standard product (ASSP) which offers is a simple-to-implement interface. It permits peripheral makers to quickly offer USB compatibility in existing products without extensive re-engineering. Functioning as an intelligent device controller, the USS-720 initiates and manages automatic negotiation for the fastest protocol available. The USS-720 can be incorporated into PC peripherals built with a conventional parallel-port interface by providing a bridge between USB and the IEEE 1284 parallel port. Peripherals that make good candidates for the USS-720 include printers, scanners, digital cameras, and back-up storage systems.

A family of 8-bit USB microcontrollers hails from Motorola's Customer Specified Integrated Circuits Div., Austin, Texas. The 68HC705JB2 and 68HC05JB2 are aimed at lower speed applications, such as a mouse or keyboard. Each chip comes with 2 kbytes of ROM (EPROM in the 68HC705JB2) and 128 bytes of user RAM. Other features include ten bidirectional I/O pins, a low-voltage reset circuit, and power-savings modes. The difference between the two components is that the 68HC705JB2 offers a voltage regulator. A complete set of development tools is available for the microcontrollers.

A 4-bit microcontroller from Samsung Semiconductor, San Jose, Calif., supports a 1.5-Mbit/s data rate, suitable for mouse and joystick applications. The KS57C6002 is a low-cost device that has an 8-bit internal data bus, comparator inputs with 4 bits of resolution (for X-Y position of the pointing device), and high-current LED drivers for status recognition. Five internal and two external interrupts offer a fast response to internal and external events. A prototype development board is available to hasten product-to-market time.

To help simplify the USB connection from the end-users' perspective, Phoenix Technologies, San Jose, Calif., has released a Windows 95 application called USBWorks. When bundled with a PC or peripheral, USBWorks addresses specific device configuration requirements. Working with the Windows Device Manager, the software collects and displays information on all operational USB devices, whether they are configured properly or not. As it result, it helps the end user identify and resolve invalid connections and over-current and over-bandwidth problems.

Phoenix also offers a USB developer's kit which lets designers rapidly prototype, evaluate, and test devices based on the company's USB functional core. The kit contains an interface card with a daughtercard connector. The daughtercard, which has direct access to the functional core, would then contain the OEM's specific USB function.

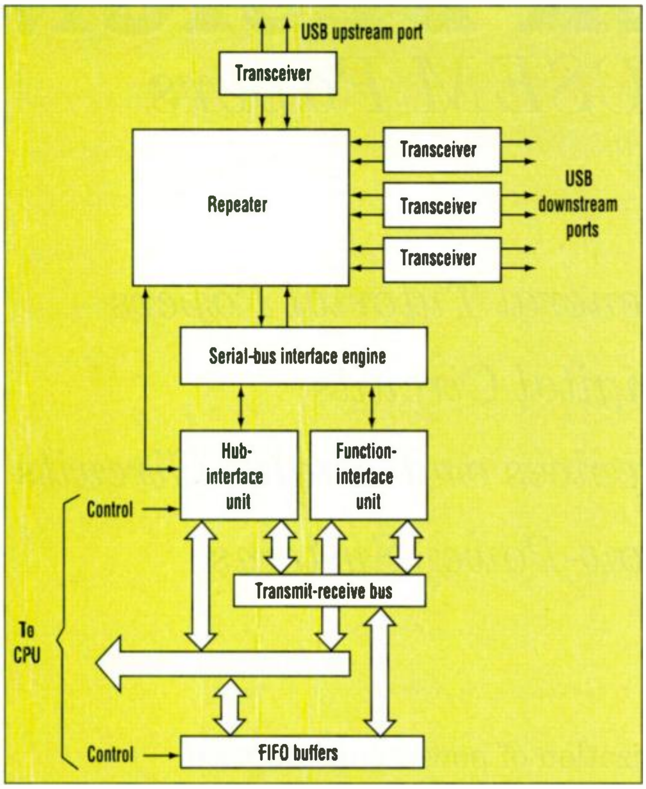


1. The USB Scanner Suite speeds development and eases implementation of USB products by conforming to the USB standard.

One of the applications where USB will make an impact is in input devices. Alps Electric Inc., San Jose, Calif., offers a keyboard and a gamepad. The nature of USB allows users to connect multiple gamepad to a systems for multi-player games. A second keyboard comes from Fujitsu Takamisawa America Inc., Sunnyvale, Calif. The company's FKB8760 is a 104-key keyboard that configures itself upon connection. The keyboard also contains a PS/2 port that can handle a mouse or other pointing device

A scanner that connects to USB was developed by Logitech Inc., Freont, Calif. This design posed some engineering challenges due to the peripheral's power consumption. The company decided early in the design process to manufacture the product with just a single cable, the one that connects to the USB. As a result, the scanner had to draw its power directly from the USB bus, which offers a maximum current source of 500 mA. Typically, scanners consume more power than the allotment offered by USB. As a result, the company had to reengineer the product to stay within the specification. In the scan mode, the typical draw is 440 mA.

To simplify the scanner designer's task, SystemSoft Corp., Natick, Mass., offers a USB Scanner Suite that they claim conforms to emerging standards, speeds development, and eases implementation. The suite consists of four components: USB interface firmware (UIF), scanner-specific firmware, a USB Windows Driver Model (WDM) driver, and a USB monitor Dynamic Linked Library (DLL) *(Fig. 1)*.



2. The 8X930Hx hub controller provides connect and disconnect detection for downstream devices while offering power-management features.

The WDM driver connects the scanner's TWAIN drivers and DLL to the operating-system stack. The UIF supplies a hardware-independent programming interface between the device-specific firmware and the USB controller. The UIF can handle all types of data transfers, including control, bulk, interrupt, and isochronous. Similar suites are available from SystemSoft to support monitors, printers, and uninterruptable power supplies.

A USB-enabled application that carries some promise is video conferencing. Not only does USB make it simple to use, it also makes it affordable. Case in point is the Video Phone from Xirlink Inc., San Jose, Calif., which carries a suggested retail price of $149. The Video Phone consists of a video camera, application software, and necessary cables. The camera draws its power directly from the bus.

The Video Phone supplies real-time audio and video over a standard telephone line. Using video compression, the Video Phone can achieve 30-frame/s video at a SIF resolution (352 by 240 pixels) and 25 frames/s at a CIF resolution (352 by 288 pixels).

One of the logical connection points for USB devices is the monitor. As a result, CTX International Inc., Walnut, Calif., developed the EX700U, a 17-in. monitor that contains a USB hub (place where end users can plug in their USB peripherals). The monitor features a 0.26-mm dot pitch and a maximum resolution of 1600 by 1200 pixels at 72 Hz.

Designed specifically for monitor-based hub solutions, the LM1050 controller, from National Semiconductor Corp., Santa Clara, Calif., performs the hub functions, supplies CRT monitor-control capabilities and integrates clock-generation features for system-level timing. This eliminates the need for a separate microprocessor clock. Also on the chip is a 3.3-V voltage regulator and an oscillator. As a result, one inexpensive crystal can be employed for all system timing functions.

Intel Corp., Chandler, Ariz., also offers a hub controller, the 8X930Hx. The controller provides connect and disconnect detection for downstream devices and power-management features, such as suspend and resume. The device contains one internal and three external downstream ports and integrates USB transceivers, a serial-bus interface engine, a hub-interface unit, and transmit-receive FIFO buffers *(Fig. 2)*. Based on the MCS251 microcontroller, the chip employs the microcontroller's standard instruction set and is binary compatible.

A four-way hub can be built using the PDIUSBH11, from Philips Semiconductors, Eindhoven, The Netherlands. The part provides one upstream port and four downstream ports. It also contains an embedded USB function with associated integrated memory that can be accessed by an external microcontroller using the I^{2}C bus. Between the upstream and downstream ports is a repeater block that's responsible for routing the USB packets from the upstream port to the device connected to the relevant downstream port. It also routes messages from the downstream ports to the host PC through the upstream port.

When building a hub, designers could turn to a low-power switch from Texas Instruments Inc., Dallas, Texas. The TPS2014 offers maintenance-free protection against electrical damage and high temperatures. When the device detects an over-current condition, it automatically limits the current to a specified safe level. The TPS2014 is available in an evaluation module for easy design-in and testing.

One of the best ways to develop and test USB designs is by taking advantage of the USB Inspector Advanced Bus and Protocol Analyzer from Computer Access Technology Corp., Santa Clara, Calif. When connected to any point in the USB network, the Inspector continuously monitors all bus activities and alerts the user to any abnormal bus conditions. The device has a 37-pin interface connector, making many of the control, timing, and recovered signal available externally. These signals can be probed and used by other devices. The Inspector's bundled Windows-based software scans the collected data and presents it to the user in several ways. Timing information and statistical analysis of bus usage can also be viewed.

ASIC and FPGA designers can implement USB functions using the UH01 core, from Sand Microelectronics Inc., Santa Clara, Calif. The hub core is a set of synthesizable blocks that can implement a standalone hub or be combined with a device-controller core to create USB peripherals with integrated hubs. The core consists of a repeater and a controller. The UH01's low gate count helps save silicon cost. Only 12,000 gates are needed for downstream ports.

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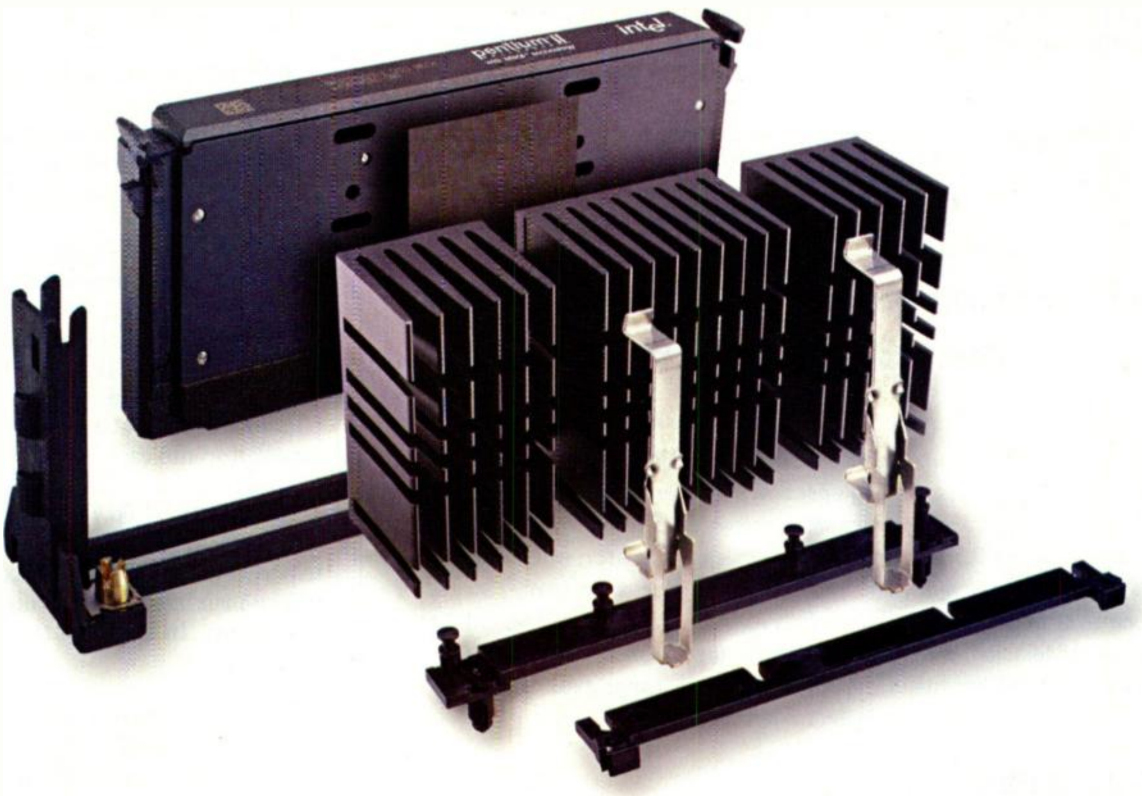

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ICSPAT/DSP World 1997, Oct. 15-17. San Diego Convention Center, San Diego, CA. Contact Denise Chan, Miller Freeman Inc., (415) 278-5231; e-mail: dsp@exporeg.com.

IEEE Holm Conference on Electrical Contacts, October 18-22. Wyndham Franklyn Plaza, Philadelphia, Pennsylvania. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Lane, P.O. Box 1331, Piscataway, New Jersey 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

VHDL International User's Forum (VIUF) Conference, Oct. 19-22. Hyatt Regency Crystal City Hotel, Arlington, VA. Contact VIUF, (415) 329-0510.

IEEE Telecommunications Energy Conference (INTELEC '97), Oct. 19-23. World Congress Centre, Melbourne, Australia. Contact Robert N.K. Thuan, Network Products-Telstra Corp. Level 14, 242 Exhibition St., Melbourne, Victoria 3000, Australia; (61) 3 634 6216; fax (61) 3 632 3607

Sensors Expo, Oct. 21-23. Cobo Convention Center; Detroit, MI. Contact Expocon Management Associates Inc., (203) 256-4700; e-mail: sensors@expocon.com; Internet: http://www.expocon.com.

Fourth IEEE International Conference on Image Processing (ICIP '97), Oct. 26-30. Fess Parker's Red Lion Resort, Santa Barbara, CA. Contact Sanjit K. Mitrea, Electrical & Computer Engineering, University of California, Santa Barbara, CA 93106-9560; (805) 893-3957; fax (805) 893-893-3262; e-mail: mitra@ece.ucsb.edu.

11th Systems Administration Conference (LISA '97), Oct. 26-31. Town & Country Hotel, San Diego, CA. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

SYSTEMS 97, Oct. 27-31. Munich Trade Fair Center, Munich Germany. Contact Messe Munchen GmbH, Messegelande, D-80325 Munchen, (49) (0 89) 51070; fax (49) (089) 51 07506; Internet: http://www.sysems.de; e-mail: info@messe-muenchen.de.

19th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, October 29-November. 2. Sally Chapman, Secretariat, National Res. Council of Canada, Bldg. M-55 Rm. 393, Ottawa, KIA OR8, Canada; (613) 993-4005; fax (613) 954-2216.

19th International Conference of the IEEE Engineering in Medicine & Biology Society, October 30-November 2. Chicago Marriott Downtown, Chicago, Illinois. Contact Meeting Management, 2603 Main Street, Suite 690, Irvine, California 92714; (714) 752-8205; fax (714) 752-7444; e-mail: embs97@ieee.org; Internet: http://www.eecs.uic.edu/-embs97.

NOVEMBER

IEEE International Test Conference (ITC), Nov. 1-5. Sheraton Washington Hotel, Washington, DC. Contact ITC, 655 15th St., N.W., Suite 300, Washington, DC. 20005; (202) 639-4164; fax (202) 347-6109.

Voice, Video, & Data Communications Conference & Exhibition, Nov. 2-6. Dallas, TX. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360)-647-1445; e-mail: exhibits@spie.org.

IEEE Global Telecommunications Conference (GLOBECOM '97), Nov. 3-7. Phoenix, AZ. Contact Nigel Reynolds, 15436 N. First Ave., Phoenix, AZ 85023; (602) 942-5583; fax (602) 942-4542; e-mail: nigelaz@aol.com.

WESCON '97, Nov. 4-6. San Jose Convention Center and Santa Clara Convention Center, San Jose and Santa Clara, CA. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045-3194; (800) 877-2668; fax (310) 641-5117; e-mail: wescon@ieee.org.

IEEE Intelligent Transportation Systems Conference (ITS '97), Nov. 9-12. Boston Park Plaza Hotel, Boston, MA. Contact Richard Sparks, 8 Richard Rd., Bedford, MA 01730; (617) 862-3000; fax (617) 863-0586; e-mail: r.sparks@ieee.org.

Productronica '97, Nov. 11-14. Messegelande, Munchen, Germany. Contact Messe Munchen GmbH, Messegelande, D-80325 Munchen, Germany; (49) (89) 51 07-0; fax (49) (89) 51 07-506; e-mail: info@messe-munchen.de; http://www.Productronica.de.

23rd Annual Conference of IEEE Industrial Electronics (IECON '97), Nov. 9-14. Hyatt Regency Hotel, New Orleans, LA. Contact Michael Greene, 200 Broun Hall, Electrical Engineering, Auburn University, Auburn, AL 36849-5201; (334) 844-1828; e-mail: greene@eng.auburn.edu.

Asian Test Symposium, Nov. 17-19. Akita, Japan. Contact Y. Takamatsu, (81) 89 927-9955; e-mail: takamatsu@cs.ehime-u.ac.jp.

DESIGN NOTES

Dual PowerPath™ Controller Simplifies Power Management

Design Note 160

Jaime Tseng

As the demand for portable electronics with multiple batteries continues to grow, so does the need for simple and efficient solutions for switching between batteries. The LTC®1473 simplifies the design of circuitry for switching between two batteries or a battery and an AC adapter.

The LTC1473 is designed to drive two sets of low loss, back-to-back N-channel MOSFET switches to route power where needed, typically to the input of the main system switching regulator. An internal micropower boost regulator supplies the gate drive for the N-channel MOSFET switches.

The LTC1473 simplifies the designer's task by incorporating a number of protection features. Short-circuit protection shuts off the gate drive when a fault condition exceeds the user-programmable time limit, inrush current limiting limits the current flowing into or out of the system bypass capacitor and a diode default mode allows power to flow from the highest potential until the inputs can be defined.

Automatic Switchover Between Battery and AC Adapter

A protected automatic switchover between a battery and a power source connected at DCIN can be constructed using the circuit in Figure 1. Under normal conditions, this circuit will route the voltage at DCIN to the output. If the voltage at DCIN drops below 9.75V, DCIN is deselected and the battery voltage is routed to the output. If the battery voltage

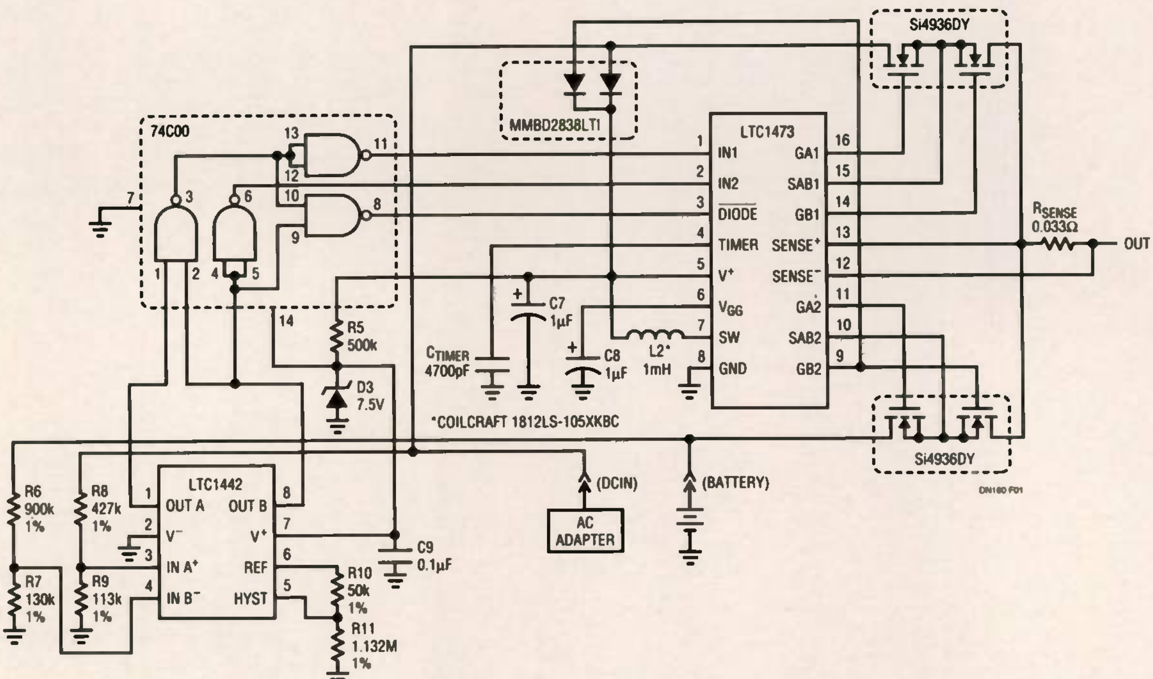

Figure 1. Protected Automatic Switchover Between Battery and AC Adapter

s less than 5.9V, each switch is made to mimic a diode, llowing power to flow from the highest potential source to he output. In this "2-diode" mode, the first half of each PowerPath switch pair is turned on, and the second half is urned off. Thus, two diodes are formed by the body diodes of the MOSFET switches that are turned off.

The inrush current limit of 6A is selected with a 0.033Ω R_{SENSE} resistor. The fault timer is set to 1.1ms with a 4700pF C_{TIMER} capacitor. If a MOSFET switch is in current imit for more than 1.1ms, an internal latch in the LTC1473 s set and the MOSFET switch is turned off.

The LTC1442 shown in Figure 1 is an ultralow power dual comparator with a precision 1.182V reference. This comparator monitors the voltage at DCIN and the battery voltage and selects which MOSFET switch to turn on. Simple ogic, comprising CMOS NAND gates, decodes the comparator outputs to control the inputs of the LTC1473. A 7.5V Zener shunt regulator in series with a 500k resistor supplies power for both the CMOS NAND gates and the LTC1442.

Power Routing Circuit for Microprocessor Controlled Dual Battery Systems

The microprocessor controlled dual battery system shown in Figure 2 uses two LTC1473s to provide input power routing and battery charging multiplexing. The two batteries can be of different chemistries. One LTC1473 is used to connect the output of the charger to the battery; the other connects the battery to the input of the system switching regulator.

The power-management microprocessor provides overall control of the power management system in concert with the two LTC1473s and the auxiliary power-management systems. The microprocessor decides which battery to connect to the input of the system switching regulator and which battery is in need of recharging. To charge a battery, the microprocessor selects the charging algorithm for that particular battery chemistry.

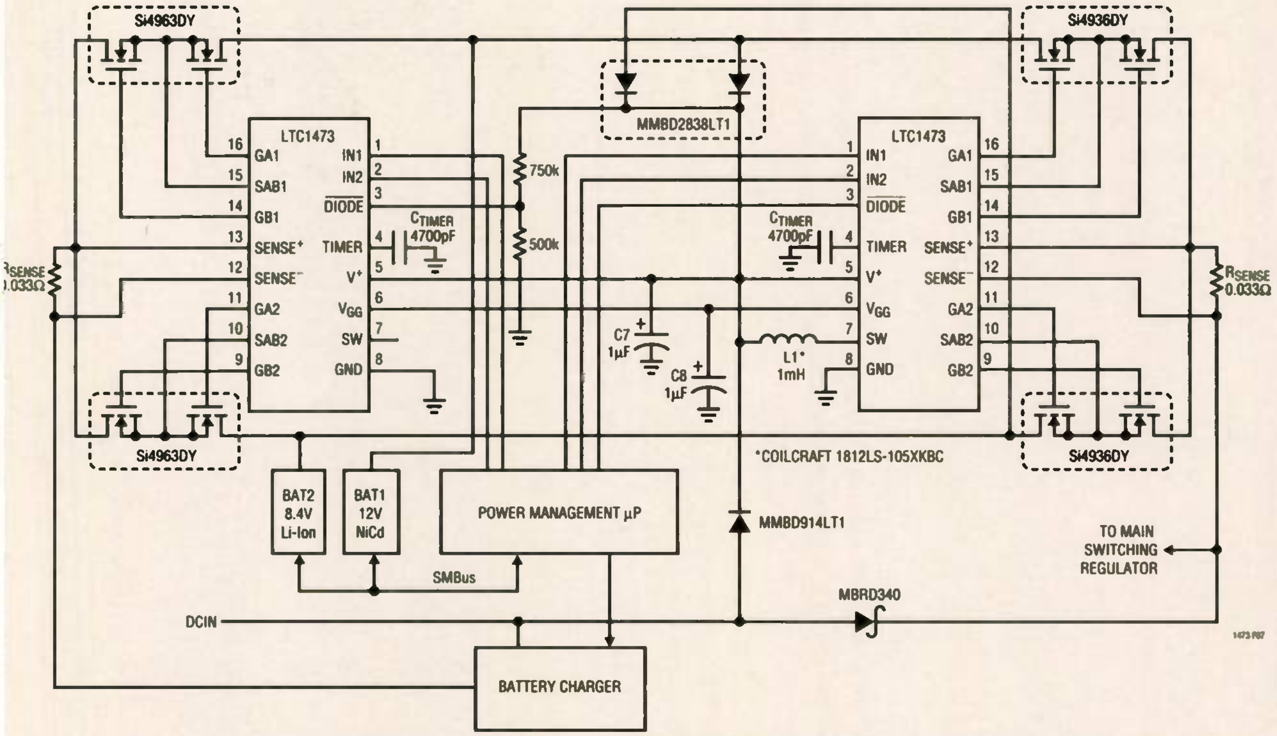

Figure 2. Power Routing Circuit for Microprocessor Controlled Dual Battery System

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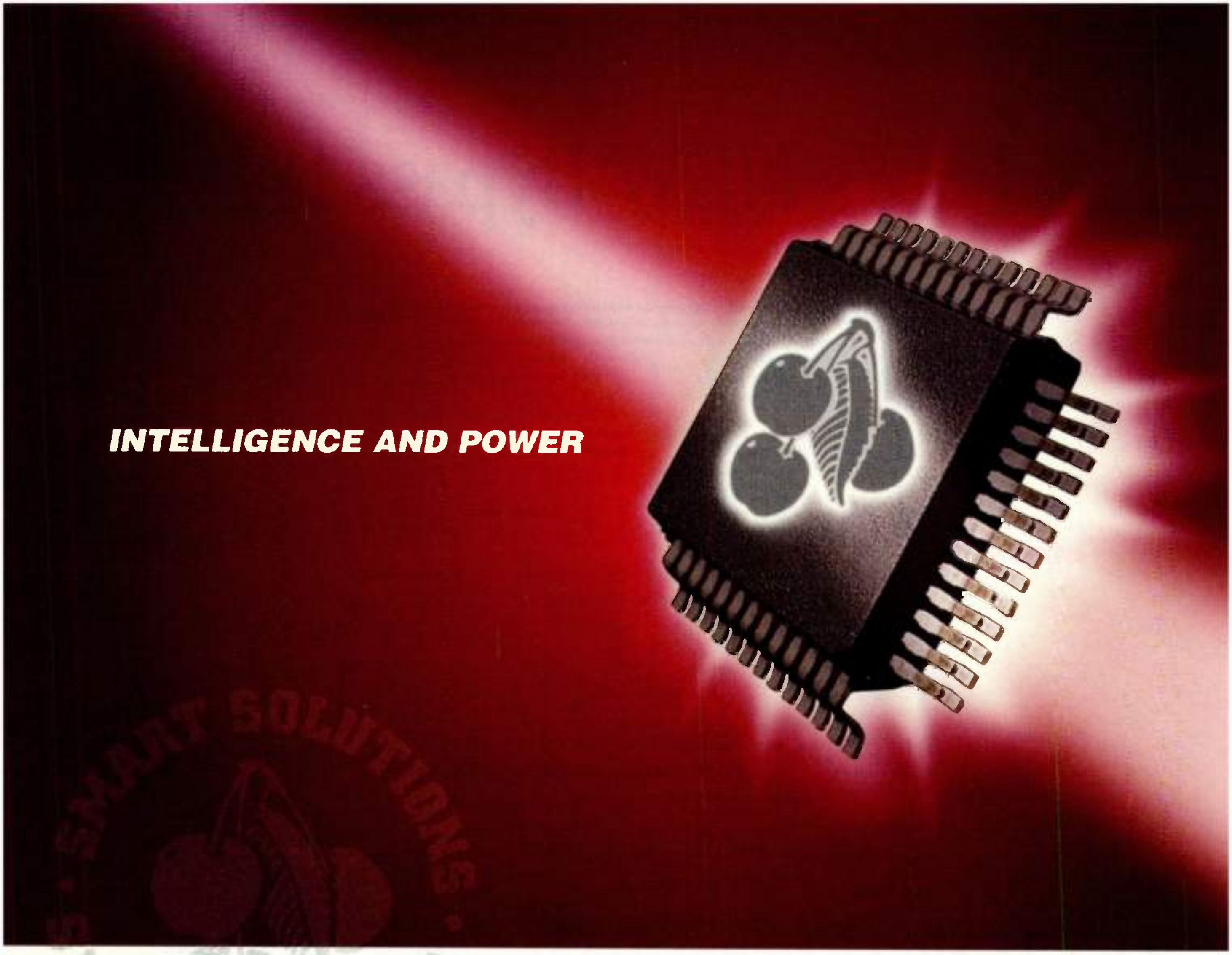

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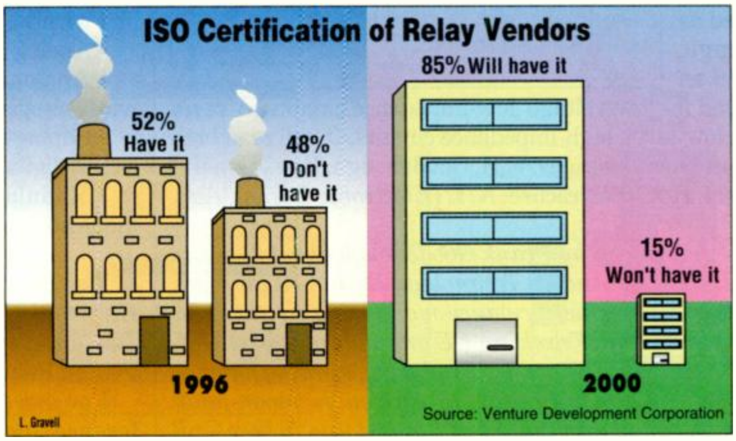
ELECTRONIC DESIGN QUICK LOOK

■ Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

ISO 9000 Really Works—At Least In The Relay Business



Ever since ISO 9000 became a reality, there have been two schools of thought regarding the standardization & certification process: "Quality assurance through ISO 9000 is better in the long run and leads to more reliable products," and "It's not worth the effort, money, or time." A new study from Venture Development Corporation, "North American Electromechanical and Solid State Relay Industry," supports the former. It shows that since their last study regarding ISO 9000 and the relay industry, OEMs have seen an overwhelming improvement in the quality and reliability of the relays they buy. In 1992, 83% of OEMs surveyed talked about all kinds of problems (contamination, failure, problems with coils and contacts, etc.) with the relays that they'd been purchasing. Last year, however, 57% of the OEMs reported relay problems—a 26% decrease in quality problems. Looking at one of the largest issues, reliability, the reported levels dropped from 54% in 1992 to 35% in 1996. Because relay manufacturers are more consistent in producing functional, high-performance products, OEMs are expressing a higher level of confidence in their shipments of relays. Another source of increased quality and reliability appears to be the result of increased automation and standardization of relay specifications. More importantly is the movement on the manufacturing side to obtain quality certification. Last year, 52% of the manufacturers said they were ISO 9000 certified. By the year 2000, the number is projected to jump to 85%.

For more information, contact Venture Development Corporation, One Apple Hill, Natick, MA 01760-9904; (508) 653-9000; fax (508) 653-9836; e-mail: info@vdc-corp.com.—*DS*

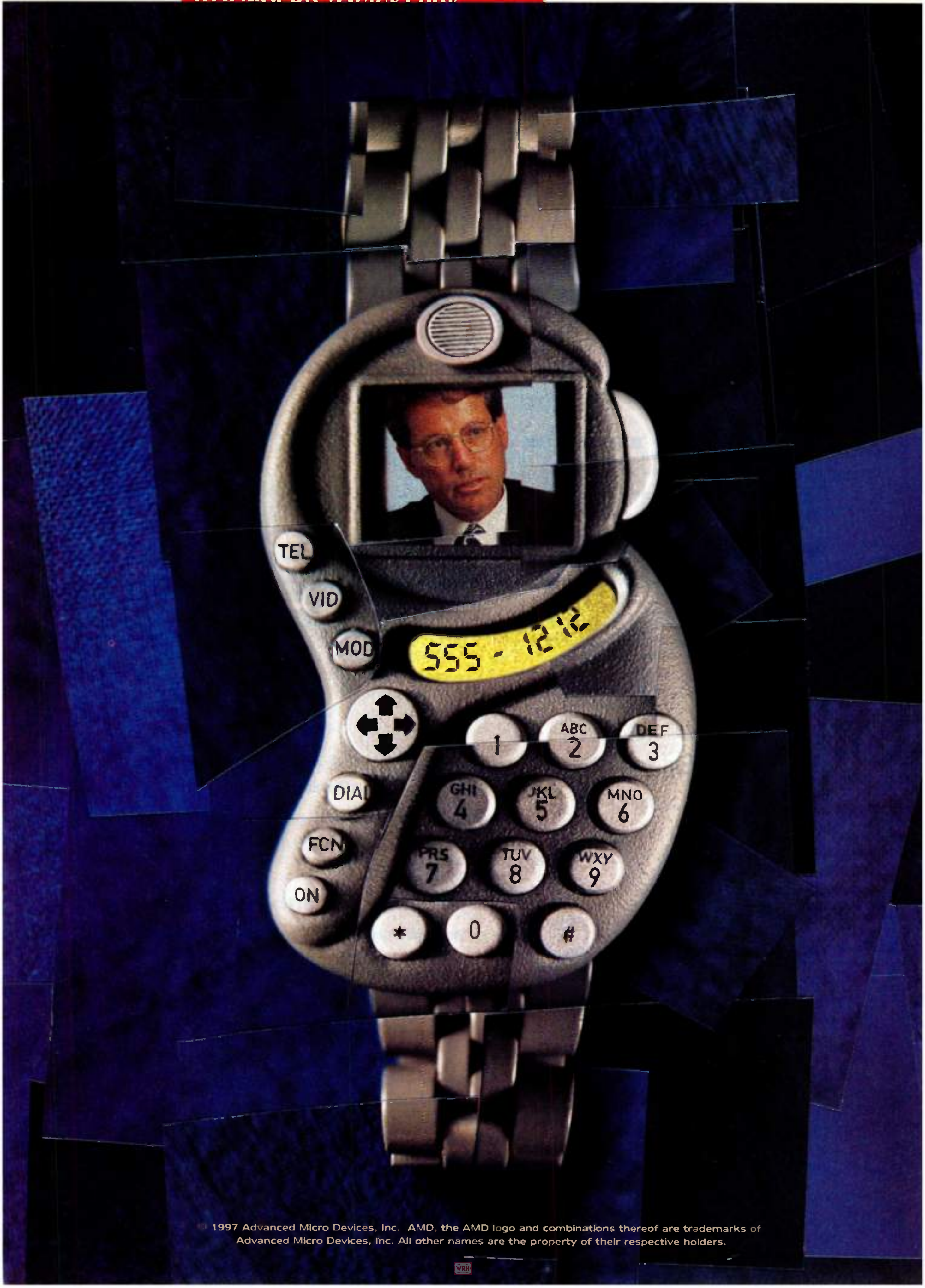
DOINGS IN EUROPE

Not only are industries of all walks going to be in a giant rush to cap off their Y2K compliance work, but now, with the impending Euro expected to come into play starting on January 1, 1999, the complications are starting to pile up.

It looks like this: The European Commission intends that the Euro will become THE currency of Europe, effective the first day of 1999. The new currency will safeguard existing and future contracts, and the transitional phase (from 1992 to 2002) will be orchestrated by the Commission. Additionally, there will be another monetary system for dealings with countries not using the Euro, called EMS Mark Two.

How are European companies dealing with all this? According to a survey from the Rationalization Committee for German Industry, 80% of small- and medium-sized businesses said that they do not have enough information on the Euro. A Meta Group study reports that 42% of the companies they surveyed have yet to act on the Euro changes. Interestingly, 23% of that study's participants hadn't even begun planning for any changes.

For more information, contact Messe München GmbH, Messegelände, D-80325 München; (089) 51 07-0; fax (089) 51 07-506; Internet: http://www.systems.de.—*DS*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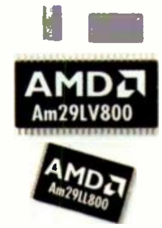

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http://www.dialight.com: Stop in at the Dialight site for a peep at their family of LED circuit-board indicators and panel-mount items. Also at the site, visitors will find links to descriptions of the company and its Electronic Products Group. The products section includes application notes, article reprints, design guidelines, and information request forms. Recent press releases and new product introductions also can be found here. Dialight manufactures light pipes, neon, incandescent lights, and illuminated push-button switches, in addition to the previously mentioned products.••

http://www.thomasregister.com/kooltronic: Linked up to the Thomas Register, Kooltronic's new web site features the latest in air conditioner and heat-exchanger technologies. The company's entire catalog is now available on-line to engineers looking to cool the interiors of enclosures holding heat-sensitive electrical and electronic components. Additionally, the site covers the company's blowers, including single and double centrifugal blowers, and high-pressure and radial blowers. Information on fans also can be found here. One unique feature at the site is the Kooltronic Free Sizing/Model Selection Diskette. The diskette is available in 3-1/2" PC format. The Sizing/Model Selection Diskette shows users practical hints and engineering or calculation aids in choosing the proper product or size.••

http://www.intel.com/english/art: If you don't have a PC equipped with a Pentium processor of the 133-MHz range or better that runs Windows 95 or NT, you might want to just skip over this *Internet Rolodex* entry. These requirements are necessary to achieve the true (OK, as true as it's going to get at the moment) 3D experience and advanced visuals that come with MMX technology. Intel's new State of the Art site, developed in Europe, showcases 3D, digitized art in an interactive setting. Artists such as Isa Genzken, Anton Henning, and Claus Goedicke are featured here. Visitors with the required hardware/software might want to download Superscape's Viscape which is a plug-in for browsers that's optimized for MMX.••

http://www.france98.com: The result of an interesting marketing pairing, the official 1998 World Cup Web site is powered by Hewlett-Packard's HP Domain Internet servers. Visitors to the new World Cup Soccer event information network will benefit from the over 50,000 staff, volunteers, and players involved in the venture. HP computer products will be used to acquire and post game results and statistics, in addition to global communications and ticketing. Additionally, HP's computers will be handling e-mail and media management here.••

TRUDEL TO FORM

JOHN D. TRUDEL
CONTRIBUTING EDITOR

I closed last time with a question: Where does innovation come from? Much as priests in the Middle Ages debated the metaphysical, this will likely be the key 21st Century concern of government and industry leaders. In the new era, wealth will come not from machine age repetitive process or agrarian age natural resources, but from intellectual property.

If we define innovation as the development of technology for commercial gain, we invented it. So said Abe Lincoln, a patent-holder himself: "(It) began in this country with the adoption of our Constitution. Before then, any man might instantly use what another had invented; so the inventor had no special advantage from his own invention. The patent system changed this; secured to the inventor, for a limited time, the exclusive use of his invention and thereby added the fuel of interest to the fire of genius, in the discovery and production of new and useful things."

Innovation, like liberty, has always been an American core value. President Harrison said so at the Centennial of the U.S. patent system. "It distinctly marked, I think, a great step in the progress of civilization when the law took notice of property in the fruit of the mind."

As I write this column, it is unclear if this value will persist. Our Congress came within a hair's-breadth of passing the Japanese designed Patent Sell Out legislation. Still, whatever the future holds, the notion of intellectual property was born in our cradle of liberty.

Note that innovation comes from people, and that the U.S. has been a historic friend of innovation. Our patent laws are unique, since, as a new nation, we felt little need to protect entrenched interests. The biographies of 121 members of the National Inventor's Hall of Fame show that though the inventors came from 24 countries, most of their work (91%) was done in America.

One would think that large companies would produce most all innovation, but one would be very wrong. Indeed, every large high-tech firm in the U.S. is ringed with spin-offs founded to commercialize innovations it rejected or ignored. I could surmise that all the founding executives in Silicon Valley came from larger firms.

The Venture Capital industry is unique to America. Without spin-offs or patents, it wouldn't exist. But innovation always threatens the existing order. "Every great advance in natural knowledge has involved the absolute rejection of authority," said Thomas Henry Huxley. "The most damaging phrase in the language is: It's always been done that way," said Rear Admiral Grace Hopper. Machievelli may have said it best: "There is nothing more difficult to carry out, nor more doubtful of success, nor more dangerous to handle, than to initiate a new order of things."

Machine Age business shares traditions and structures with the military. The mavericks—from General Billy Mitchell to Seymour Cray—are rarely rewarded and often in peril. Indeed, those who succeed in creating enclaves of innovation often become folk heroes.

Of inventors awarded Hall of Fame status, 51% were entrepreneurs who started their own firms, 27% were corporate, 16% academic, and 5% were independents who licensed inventions. It takes exceptional leadership to preserve a firm's innovation capability.

John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops also are available. He is the author of "High Tech with Low Risk." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 640-5599; fax (503) 543-6361; e-mail: jtrudel@gstis.net; Internet: http://www.trudelgroup.com.

OFF THE SHELF

"VHDL for Programmable Logic" is a hands-on tutorial that explains the architectures, features, and technologies of programmable logic and teaches how to write VHDL code for synthesis. The book includes a CD-ROM featuring Warp 2 (R), a VHDL software synthesis tool from Cypress Semiconductor. The book discusses in detail the design description process through synthesis, placement, and routing, to the creation of test benches for design verification. Also included is an interactive waveform that performs functional simulations of CPLD designs. The 593-page book is priced at $45. Contact Addison Wesley Longman, 2725 Sand Hill Rd., Menlo Park, CA 94025; (415) 854-0300; Internet: http://www.aw.com/cseng/.

"Optoelectronic Packaging" is a sourcebook on optoelectronic assembly techniques. It provides an overview of today's state-of-the-art technologies, packages now on the drawing board, and the future direction of packaging types. Topics covered include detector, semiconductor laser, and optical amplifier packaging; waveguide technologies, free-space interconnects, and hybrid technologies; and array device packaging and flip-chip assembly for smart pixel arrays. The book also contains case studies of packaged subassemblies. The 260-page book is priced at $74.95. Contact John Wiley & Sons Inc., Professional, Reference, and Trade Group, 605 Third Ave., New York, NY 10158-0012; (212) 850-6336.

"Linear Electric Actuators and Generators" deals with linear electric actuators (LEAs) that convert electric energy into controlled mechanical motion of limited travel, and linear electric generators (LEGs) that transform mechanical energy into electric energy. The book details the construction, operation, control, and design of LEAs and LEGs. Chapters describe linear induction, permanent-magnet, linear reluctance, switched reluctance, and linear stepper actuators. The text includes design examples. The 237-page book is priced at $59.95. Contact Cambridge University Press, 40 W. 20th St., New York, NY 10011-4211.••

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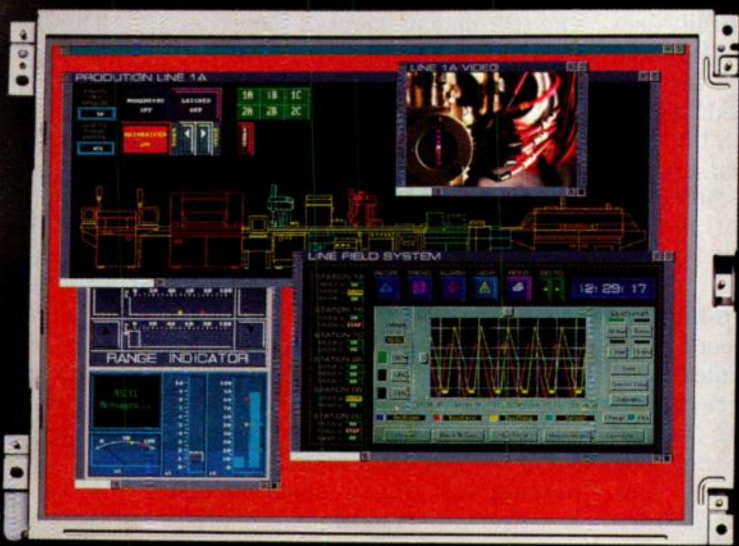

Sharp's CSTN screen sizes include 10.4", 11.3", 12.1", 13.8", 15.0" and 17.7" – with even larger diagonal sizes coming soon!

Video response times and improved contrast ratios will soon allow for animation capabilities able to bring manufacturing process functions to life.

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11.3"	LM64C391	640 x 480	150
12.1"	LM80C31	800 x 600	200
13.8"	LM14X79**	1024 x 768	200
15.0"	LM15X80**	1024 x 768	200
17.7"	LM18X74	1024 x 768	150

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QUICKNEWS

Stop Playing With Your Ethernet—Two new versions of the Allied Telesyn AT-2000 Plug and Play Ethernet adapter card are now available, the AT-2000T PnP and the AT-2000U Pnp. Both cards are fully preconfigured and are adjustable to custom environments. Both versions (as is the case with all Allied Telesyn adapter cards) come with lifetime warranties and free technical support.

The AT-2000T PnP offers 10Base-T support, while the AT-2000U PnP interfaces with 10Base-T, AUI, and BNC.

Both cards feature a 16-bit data path and 15 Kbytes of on-board memory. They also have full-duplex capability for high performance and increased throughput. As far as standards are concerned, the cards stand up to the IEEE 802.3, and are compatible with standard NE2000 drivers found in most network operating system software.

Ensuring easy installation, the cards are bundled with a diagnostics diskette and a full set of software drivers. Users also can find newer and enhanced drivers at Allied Telesyn's BBS, ftp server, and web site.

The AT-2000T PnP cards are priced at $29.00 each, and $530 in packs of 20. The AT-2000U PnP cards are priced at $41.00 each, and $745 in packs of 20.

For more information, contact Allied Telesyn International, 19015 N. Creek Pkwy., Bothell, WA 98011; (206) 481-3784; fax (206) 483-9458; Internet: http://www.alliedtelesyn.com.••

Testing The Waters—Software Research and Aonix have paired to offer an end-to-end automated software testing tools solution. Aonix will be using TestWorks in all Aonix installation and sales, with special emphasis on the 10X package. The agreement between the two companies will integrate their complementary tools to reduce errors in testing, improve productivity, cut the time between releases, and raise the level of quality in software.

The 10X system works through five days of training on requirements modeling and specification-based testing. Aonix's software Through Pictures tool is used in recording requirements. Aonix's "T" is used for generating test cases, then Software Research's TestWorks Regression suite is brought into the picture for automated test execution, validation, and test management of the generated test cases.

When the test cases have shown that the criteria meet the requirements, TestWorks Coverage tool suite looks at the completeness and the quality of the test cases, showing how the source code shakes out in the branch, call-pair, path, or path class levels. All of the information is displayed visually in reports.

The TestWorks suite incorporates capture and playback, code comprehension, coverage analysis, metrics and maintenance, regression testing, software test management and reporting, test-data generation, and test execution and evaluation products for integrated testing and quality assurance.

The tool suite features an open architecture, allowing compatibility with enterprise-wide applications, regardless if they're distributed client/server systems or embedded. It also can be used in in GUI desktop or web applications, operating in JAVA, C, C++, Ada, and Fortran F77.

The Software Through Pictures Object Modeling Technique from Aonix is a robust multi-user analysis and design environment that uses a shared repository. The Use Case Editor and the "T" Test Case Generator perform high-level analysis to identify requirements and automatically build test cases to test those requirements' validity, respectively.

For more information, contact Software Research Inc., 615 Third St., San Francisco, CA 94107-1997; (415) 957-1411; fax (415) 957-0730; Internet: http://www.soft.com.••

Making The Switch—Three switch manufacturers have recently incorporated the ICS 1890 Fast Ethernet transceiver chip into their Gigabit Ethernet switches. Alteon Networks' AceSwitch family, GigaLabs' Gigastar 100/3000 switches, and the FIRST (Fully Integrated Routing Switch Technology) family from Rapid City will all be using the new device. ICS has been a member of the Fast Ethernet Alliance and is currently an active member of the Gigabit Ethernet Alliance.

The ICS 1890 features adaptive equalization, Clock and Data recovery, filtering and autonegotiation modules, MII and symbol interfaces, an MLT-3 encoder/decoder, stream cipher, and a Ten Meg transceiver. Designer configurable register sets and 10/100 channels are implemented via a single off-the-shelf magnetics. The device can function in both half- and full-duplex applications.

ICS 1890 transceivers have been used by Ascend, Compaq, FORE, Hewlett Packard, Hitachi, 3COM, and Xircom. The company also has a technology exchange with IBM.

Alteon Networks' AceSwitch line of switches is a new class of local area network devices known as server switches. They are designed to greatly improve interserver communications. One member of the AceSwitch family, the 110 model, has eight 10/100 Fast Ethernet ports and two Gigabit Ethernet ports.

The Gigastar 100 from GigaLabs offers ATM, Gigabit Ethernet, Gigapipe, HIPPI, and network management in a five-slot modular chassis. The 3000 features 16 slots in a modular chassis. It handles full-duplex Gigabit throughput in each slot.

The FIRST line from Rapid City includes the F1200, F600, and F200. The company offers options of several 10/100 Mbps and Gigabit Ethernet ports. The family of switchers is designed to tighten up the performance line between routing and switching, providing IT managers with a means to add new capabilities to their legacy networks. FIRST devices support Ethernet, Fast Ethernet, and Gigabit Ethernet transmission speeds for optical-fiber and twisted-pair connections to PCs, routers, switches, and workstations.

Alteon Networks can be reached via their web site: *http://www.alteon.com.* Other information can be obtained from GigaLabs, 290 Santa Ana Court, Sunnyvale, CA 94086; (408) 481-3030; fax (408) 481-3045; Internet: http://www.gigalabs.com.••

Guerilla Acoustics And More

As the Audio Engineering Society rings in its 50th year, their 103rd Convention will be held at the Jacob Javits Center in New York City, September 26-29. Technical papers, workshops, and intriguing speakers will be featured at the convention that has a reputation of drawing over 18,000 attendees. This year's event will be more attendee-centric, as strategically placed monitors will carry live coverage of some of each day's events.

Another improvement in the direction of the attendee is the option to take individual workshops. The AES Board of Governors is now offering single admission prices of $35 for members and $50 for nonmembers. Free events such as the NARAS Grammy forum (held on Saturday, Sept. 27) also will attract attendees.

Sixteen workshops and over 140 technical papers will be delivered at the AES convention. Sony's David Kawakami will chair "The Audio Implications of DVD," Pavo's Bob Moses will chair "Firewire: IEEE 1394," and RPG Acoustics' Troy Jensen will hold the "Guerilla Acoustics" workshop, just to name a few. Of special interest will be Tom Owen's "Audio Reconstruction and the Use of Black Boxes in Plane Crash Investigations."

The largest draw of the 103rd AES Convention is expected to be Thomas Dolby Robertson. Commonly known in "alternative music" circles as Thomas Dolby, Robertson will be heading "The Future of Music on the Internet." That session (get there **early**) begins at 2 p.m. on Saturday Sept. 27.

At the convention, the Technical Council will be sponsoring a three-hour tutorial, "Perceptual Coding of Audio Signals," and a five-hour session devoted to "Networks and Interactive Audio" (including the Robertson address). The coding tutorial session on "Auditory Modeling" will be hosted by James D. Johnston of AT&T Labs Research. Thomas Sporer of Universität Erlangen, Germany will host the session on "Objective Audio Signal Evaluation—Applied Psychoacoustics for Modeling the Perceived Quality of Digital Audio." Other papers given on Friday, Sept. 26 include 10 on "Low Bit-Rate Coding Technology." Overall, 73 hours of lectures and presentations are open to convention attendees.

Looking to the future, Sunday, Sept. 28 will feature papers dedicated to emerging hardware, software, and techniques. Takeo Yamamoto of Pioneer Electronic Corporation, for example, will chair the "High-Resolution Recording Systems" sessions. Included at the presentation will be "DVD—Audio Format," by Eiichi Funasaka and Hiroaki Suzuki of JVC Technology Development Division, and "Coding Methods for High-Resolution Recording Systems," by Robert Stuart of Meridian Audio. New hybrid, high-density, optical-disc-carrier technology from Philips and Sony will be discussed in "Disc-Technology for Super High-Quality Audio Applications," presented by Reinier ten Kate of Philips Optical Disc Technology Center.

For more information, contact Howard Sherman, AES, 60 E. 42nd St., New York, NY 10165-2520; (212) 777-4711; fax (212) 979-0128; e-mail: hshermanpr@aol.com; Internet: http://www.aes.org.—*DS*

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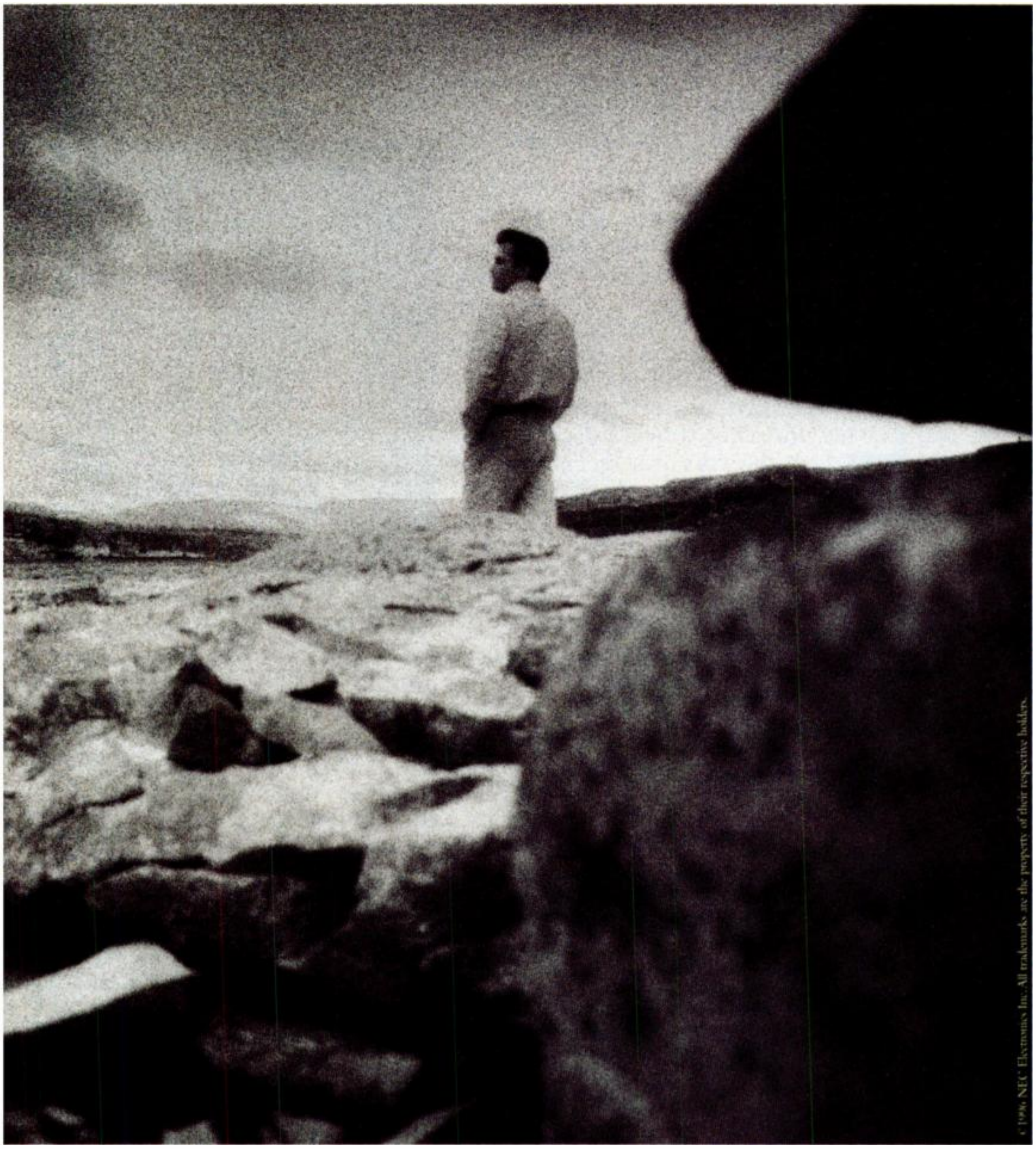

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Pin Count/Package	100 PQFP	160 CQFP	120 PQFP	240 CQFP 256 BGA	272 BGA 223 CPGA	304 CQFP 256 BGA
SPECint92/SPECfp92	45 VAX MIPS	---	80/60	75/85	---	128/120
SPECint95/SPECfp95	---	---	---	---	5.5/5.5	---

NEC

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Y2K UPDATE

Gotta Love The Merchandising

With all the panic going on about the Year 2000 Date Change Dilemma, the last thing anyone's going to want to think about is a T-shirt with Year 2000 anywhere on it. OK, for one company, up in Maine, it's the first thing on their minds. Born out of a need to raise awareness of the Y2K issue, Project 2000 Inc.'s logo is quickly becoming the "official" logo for Y2K project teams worldwide.

David Bettinger, Project 2000's president, started the company with the intent of getting away from the negativity attached to working on such a controversial project. His slogan, "Break on thru to the other side!" is meant to encourage Y2K project teams to strive for excellence, while finishing the project in the most timely manner.

Companies with Y2K project teams have ordered quantities of the Project 2000 t-shirts with their company logos emblazoned on them, in addition to the Project 2000 logo. Bettinger's experience with his own company's Y2K assessment has given him the perspective needed to reach out to fellow Y2K professionals for support.

But, it's not just the kind of support found in purchasing a number of t-shirts for your team. It's more than that. Project 2000 had been, until recently, featured as a link at the Year 2000 Information Center Web site *(http://www.year2000.com/cgi-bin/y2k/year2000.cgi)*. On April 28 of this year, a Canadian novelty company, Year 2000 Inc., threatened to sue deJager & Co., Ltd., the site's owners, unless Project 2000's link was removed.

It gets stickier. Project 2000 is an American company, while both deJager & Co. and Year 2000 are Canadian. Year 2000 owns a Canadian trademark on the term "Year 2000," and plans to market a line of merchandise using the term. Project 2000 had been offering its line of t-shirts, sweatshirts, and baseball-caps on the Year 2000 Information Center's site since March 1996, depending heavily on the link for its sales.

Since the link to Project 2000's site constituted a violation of Canadian trademark law, deJager & Co. removed the link. And, the company is staying out of the dispute, while Project 2000 is moving to trademark "Year 2000" in America.

While it seems ludicrous that companies would need to trademark what would appear to be a public-domain term, this is the state of the market.

The t-shirts are 100% cotton, and come in navy and white. There are short- and long-sleeve versions of the shirt, priced at $15 and $18, respectively. Project 2000 also offers a three-button polo shirt, also in navy and white, priced at $24. If you happen to be bringing a company into Y2K compliance that keeps the temperature around 60°F, you might want to try the sweatshirt, priced at $25. My pick is the unstructured ballcap that comes in blue, green, or gray ($14).

Companies interested in buying quantities for their compliance teams also can choose back or front (or both) for logo placement. Call Project 2000 for specifics.

If you want more ordering information, contact Project 2000 Inc., P. O. Box 1305-114, Brunswick, ME 04011; (207) 729-5438; Internet: http://www.clinic.net/project.••

Now this is the ultimate gift for the Y2K compliance jockey in your life (alright, the ultimate gift would be that elusive silver bullet, but this is the best I could do right now). The CountDown Watch, from Branco International, doesn't just tell the current time, but counts down to the year 2000, as well.

Digitally, via a nine-digit Epson LCD timer, the watch ticks off the hours, minutes, and seconds until

January 1, 2000. The watch does come preprogrammed to count down until "doomsday," but it also can be programmed to count down to any other date the wearer would like to remember, such as tax day, primary day, or even a loved one's birthday. And, the programming is easy, according to Matt Spataro, owner of Branco International, "If you can program your VCR, you can program this watch."

The watch comes in black or white, with the white watch wearing Roman numerals for the 12, 3, 6, and 9 numbers. The case is PDP-plated brass, and for those of us who tend to crash into cubicle walls on a regular basis: Shockproof. It's also waterproof to 90 ft. The analog portion of the watch is ISA 369 Swiss made. It comes with a one-year warranty.

In addition to buying directly from Branco International, any Museum Company store in a mall near you will carry the watch.

For more information, contact Branco International, 91 Main St., Kings Park, NY 11754; (516) 544-4604; fax (516) 544-4145—*DS*••

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COOL PRODUCTS

by Richard Nass

This is a long overdue column. I've received quite a few candidates recently for the "Cool Product" award, and here are the winners. First is the Courier V.Everything/ V.34 modem from U.S. Robotics, Skokie, Ill. I ran the modem at 33.6 kbits/s for a while before upgrading to the x2 technology at 56 kbits/s. I must admit I had to get help from Tech Support to do the upgrade. But I did get it done eventually and the modem tops out at about 45 kbits/s. They tell me the reason I can't reach 56 kbits/s is probably due to my "dirty" phone line. But I haven't encountered any compatibility problems. For more information, call them at (847) 982-5001, or access their web page at *http://www.usr.com.*••

If you use the Pilot (from U.S. Robotics) or some other type of computer that requires pen input, I strongly suggest that you take a close look at a stylus offered by the Cross Pen Computing Group. These guys have been in the pen business for a long time; they should know something about how to build a type of device that's comfortable to use. I also came across the Cross Stylus at Comdex. The PR person literally grabbed me in the aisle and said, "Try this." At first, I was skeptical, but after trying it out, I must admit I was amazed. I've been a Pilot user for about a year and have gotten pretty good at inputting data with the provided stylus. But the Cross Stylus really makes a difference. Why? Because it's comfortable in your hand, and it makes the characters easier to recognize for the system (at least it did in my case). The offerings from Cross start at $12.50. You can contact the company by calling (401) 333-1200, or access their home page on the World Wide Web at *http://www.cross-pcg.com.*••

At the recent Spring Comdex trade show, I came across an interesting product that's worthy of the Cool Product label—the NoiseBuster Extreme portable stereo headphones from Noise Cancellation Technologies Inc., Stamford, Conn. By placing a microphone in the earpiece of the headphone, it transmits an anti-noise signal that cancels out the unwanted background noise. This is a technology that's been around for a while, but I haven't seen it in a low-cost consumer product before.

The best test I could think of for the headphones was on an airplane, where engine noise tends to drown out what is being fed into the supplied headphones. Well, on the flight back from Comdex, it worked like a charm. It even ships with the adapter that's required for the jacks found on planes. For $69, it's a must for someone who spends a lot of time on planes. Call the company at (203) 961-0500, or see their web site at *http://www.nct-active.com.*••

The next product is a 7-Gbyte hard-disk drive from Maxtor Corp., Longmont, Colo. The EIDE DiamondMax 1750 drive is the answer for anyone afraid of SCSI (or doesn't want to pay the extra cost for it). It fits a 3.5-in. form factor and boasts an areal density of 1.2 Gbits/s.

What surprised me more than anything was how easy it was to install the drive. To make room for the it, I had to eliminate my 5.25-in. drive (which hasn't been used in quite a while). The hardware installation was relatively simple, about what you'd expect. It was the formatting and partitioning that I was somewhat concerned about, knowing the limitations inherent to IDE.

The directions said to insert the included floppy disk, boot the system from that disk, and let the drive format itself. There was only one slight problem—my unit came with no floppy disk! So I went to Maxtor's home page and downloaded the executable installation file. I then ran that file, and the rest was a breeze. It asked me to write down all the configuration information that it provided, then asked me how I wanted the drive partitioned. I chose the default settings and the installation continued. It named each of the partitions D though G and renamed the CD-ROM drive as H. Now, I just have to figure out what to do with 7 Gbytes of storage. One important note: The drive sells for $499. For more information, call (800) 2MAXTOR or (303) 447-0044. Their web address is *http://www.maxtor.com.*

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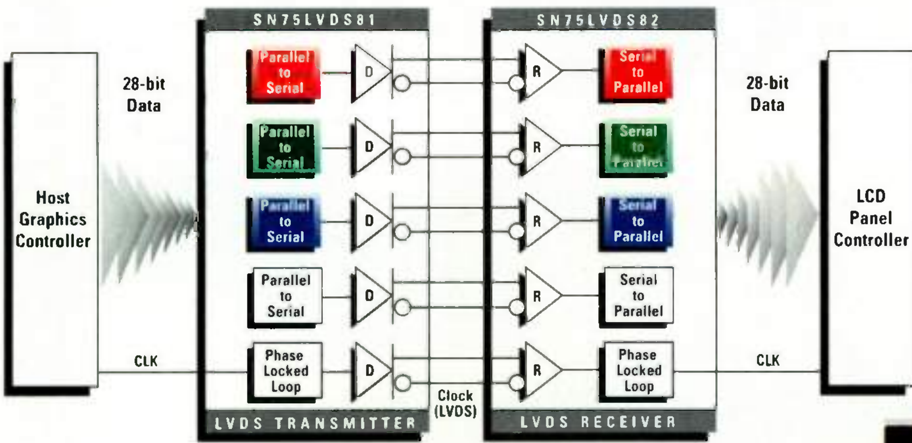

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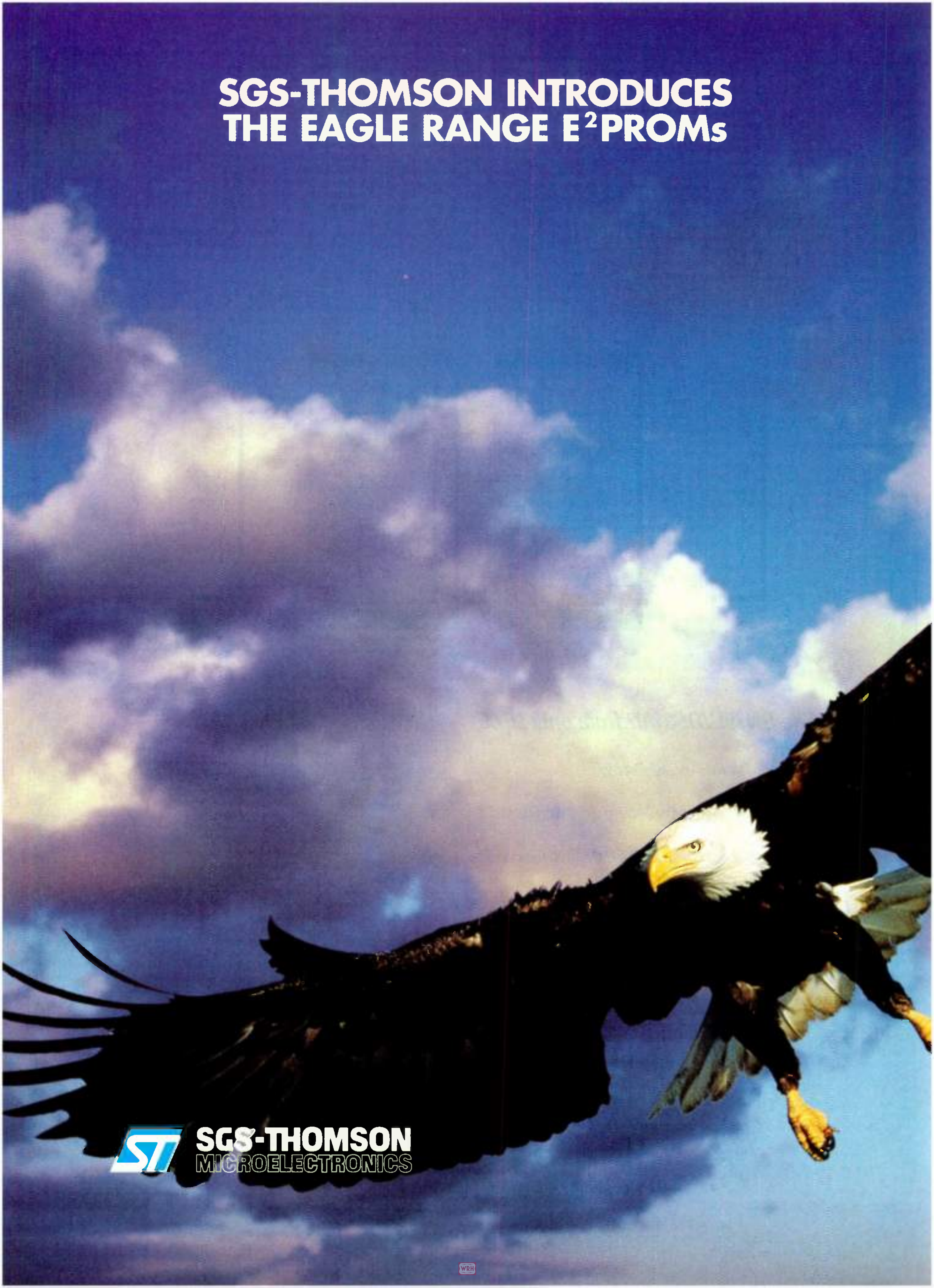
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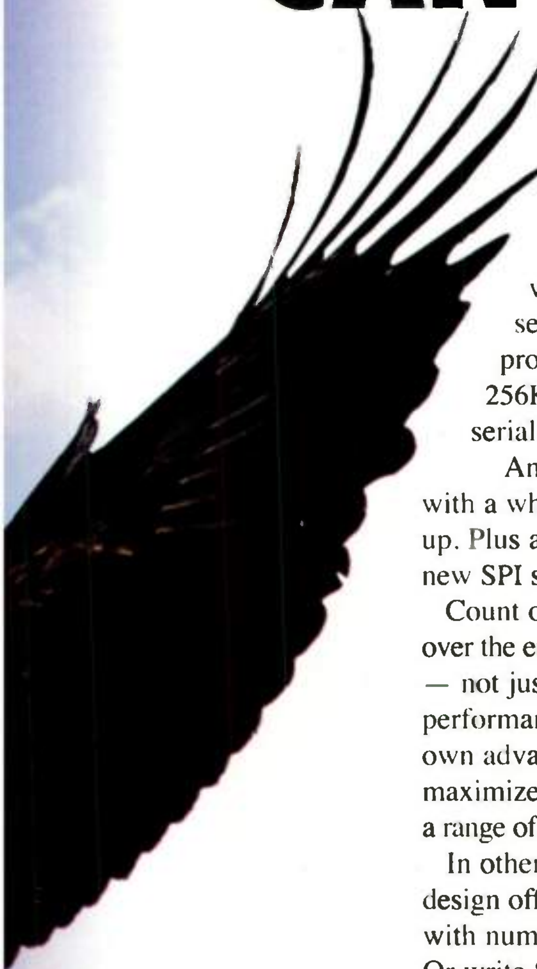

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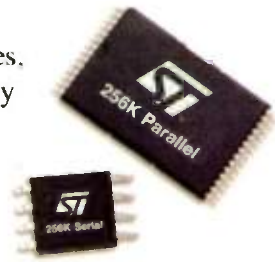

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SciTech MGL 3.1 is the newest version of SciTech Software's professional graphics library for Windows 3.1x, 95, and NT, as well as DOS. SciTech MGL 3.1 is currently available in a public beta version from SciTech's web site: *http://www.scitechsoft.com.*

Designed to eliminate the algorithms required to calculate the positions of individual dots that are "lit up" in graphics, according to Tom Ryan, director of marketing for SciTech, SciTech MGL 3.1 saves the software developer from programming all that graphics code. Commercial, high-performance graphics can be created with the library in a quick and efficient manner due to the new addition of OpenGL API support.

The OpenGl API allows programmers to work with 3D technology from the software level to the hardware level. Applications can be created within windows or in full-screen mode, rendering directly to hardware. Three OpenGL implementations are supported: Mesa (freeware clone), Microsoft's MSOpenGL, and Silicon Graphics' Cosmo OpenGL.

Another new element of SciTech MGL 3.1 is the Game Framework. It allows developers to "get up and running quickly," says Ryan, "by acting as a template for creating graphics applications." Ordinarily, developers must write a great deal of code to deal with switching between windowed and full-screen modes, as well as available color depths. However, by using the the Game Framework within SciTech MGL 3.1, the developer works with Windows for on-the-fly switching. For example, one of the most popular games available, Quake, by idSoftware, was recently brought into the Windows realm via SciTech's MGL 3.1, yielding WinQuake.

Other applications for the graphics library include CAD packages, digital slot machines, space shuttles, satellite control, concert and theater lighting, and digital scanners found in airport security. In the airport security application, SciTech MGL 3.1 technology would be used to display fine detail of baggage contents.

For more information, contact SciTech Software Inc., 505 Wall St., Chico, CA 95928-5624; (916) 894-8400; fax (916) 894-9069.••

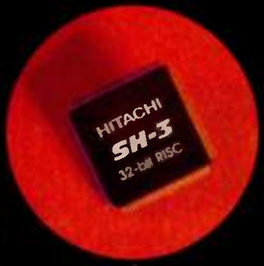
Visual Encyclopedia is the fruit of a strategic licensing agreement between FirstFloor Software and Market Power. FirstFloor is supplying its Smart Delivery technology and Market Power is bringing its Visual Matrix application to the table to form the Visual Encyclopedia project. The partnership is targeted toward sales organizations that use LANs, WANs, or Internet applications in order to retrieve and exchange their latest marketing and sales information.

FirstFloor's Smart Delivery is a web page and document push technology that comprises intelligent agents and off-line viewing. Additionally, the technology allows users to distribute documents in any format. By pairing Smart Delivery with Visual Matrix, sales professionals are able to pick up audio and video clips, competitive information, presentations, pricing guides, and product information without leaving the Visual Matrix application.

Monitoring selected documents, Visual Encyclopedia also will send web pages along to the user, alerting him or her of updates and changes. Going along with the marketing schematic, Visual Encyclopedia also will target specific audiences for document distribution and notification. As a result, subscription groups can be formed on the basis of only the most relevant fact and figures.

Additionally, users can navigate directly to information housed within Visual Encyclopedia. Indexed material is viewed from Visual Matrix. All the user has to do is click on the link. The technology-enabled selling tool is designed to produce a more competitive sales organization.

For more information, contact Market Power Inc., 101 Providence Mine Rd., Suite 104, Nevada City, CA 95959; (916) 265-5000; fax (916) 265-5171; Internet: http://www.MIP net.com.••



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ISLPED '97 Shows What's Up In Ultra-Low-Power Digital Systems

New Hardware And Software Techniques For Cutting Digital And Mixed-Signal System Power Featured At The Conference On Low-Power Electronics And Design.

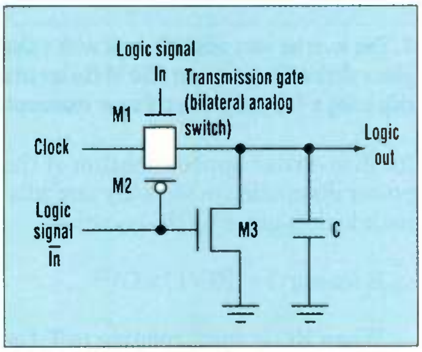
Frank Goodenough

Many system designers these days hear the words "cut the power" long after they've stopped hearing "make it keep up with our 400-MHz microprocessor." However, little do they know that there are groups of digital IC and logic designers working to cut the power required by all digital and mixed-signal systems. For the most part, the digital guys go after the fCV^2 problem in which charging and discharging of the capacitive load at every FET gate on every clock cycle generates unacceptable power dissipation.

These digital designers are working in arcane fields such as "adiabatic" or "charge-recovery logic," "low voltage differential current-switch logic," "multithreshold CMOS," and "cycle accurate macro-models for RT-level power analysis." They use phrases like "clock-powered microprocessors," "pre-charged gates," and "optimized memory hierarchy to exploit temporal locality in the memory accesses on array signals."

But you shouldn't be misled by these terms. These same designers will be presenting papers at the upcoming ISLPED '97 (International Symposium on Low-Power Electronics and Design '97) at the Monterey Convention Center, Monterey, Calif., Aug. 18-20 (see "Want to go?").

The conference includes 42 papers running in two parallel tracks—one will cover systems and CAD, the second will cover circuits and technology. A pair of invited keynote addresses will discuss "Technology solutions towards multifunctional and low-voltage/low-power cost-effective radio transceivers" and "low-power CMOS design through V_{th} control and low-swing circuits." A panel discussion will address the challenge of "Low-power design without compromise."



1. An adiabatic logic circuit can consist of just three FETs. FETs M1 and M2 form a transmission gate, and M3 forms a "pull-down" circuit.

The conference also features a pair of invited tutorials aimed at the working designer: "Low-voltage technologies and circuits—an industrial perspective," and "Power estimation and optimization at the logic level."

Less Power, More Features

Though this year's symposium sports papers from many in the academic world, it also has papers authored by designers from companies such as Analog Devices, Sony Corp., and Toshiba. As these papers point out, the future may not hold out for 100-A microprocessors running off 1-V rails sporting power cables that look like truck-battery cables or audio "Monster Cables." But don't hold your breath. Minimizing or cutting power use just gives microprocessor designers more features to add—and the power to allow them to do it.

Work that will pose a challenge for advanced-microprocessor designers is described in the paper "A clock-powered microprocessor." It will be pre-

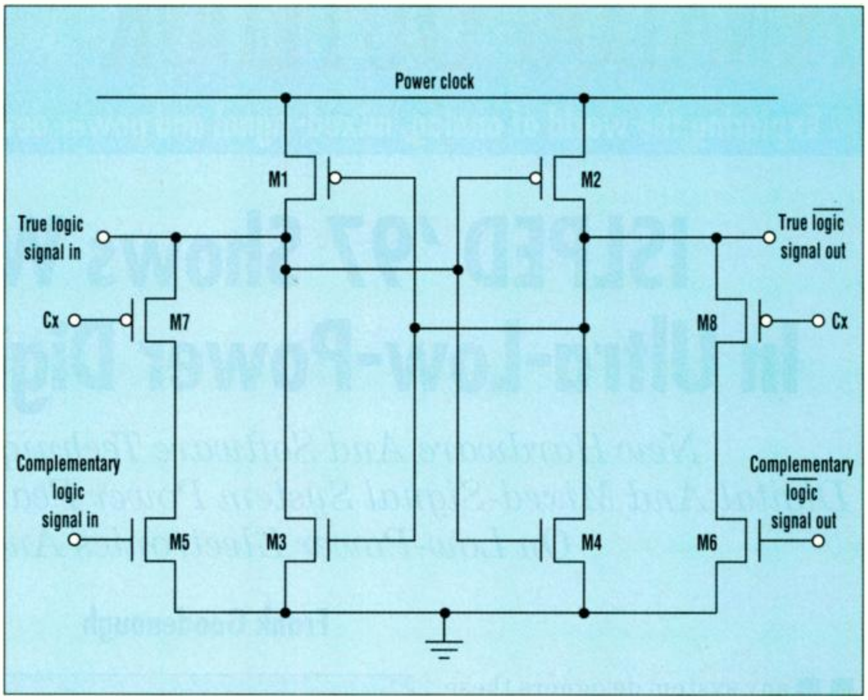
Want To Go?

The International Symposium On Low-Power Electronics and Design (ISLPED '97) will be held at the Monterey Convention Center, Monterey Calif., Aug.18-20. For additional information, contact ISLPED '97, c/o Meeting Hall Inc., 571 Dunbar Hill Rd., Hamden, CT 06514; phone and fax (203) 287-9555.

sented by a joint team from the University of Southern Calif., Marina del Rey, Calif., Rockwell, and Sony. They describe the AC-1, a 0.5-µm n-well CMOS 16-bit microprocessor that executes general-purpose programs. Running at 58.8 MHz, the processor's clock-powered CMOS logic cuts power under these operating conditions to just 26 mW for supply voltages from 1.8 to 2.5 V *(Fig. 1)*. Using conventional logic, the device would nominally dissipate four 4 to five times that power.

In clock-powered logic, the clocks directly charge and discharge the large on-chip capacitive loads *(Fig. 2)*. In this circuit, the input (in dual-rail form), controls a transmission gate (a bilateral analog switch) and a pull-down FET. When the input is a logic zero, the pull-down FET holds the output low. When the input is high, clock power passes to the output via the transmission gate. In conventional logic circuits, the clock line controls the FET gates, which in turn steer charge from the supply rail to the output or from the output to ground.

Clock-powered logic becomes low-power logic when the path from the clock source to the output charges adiabatically. During adiabatic charging, the clock transition time T is made greater than the RC delay in the path from clock to output. A simple but useful first-order approximation of the power dissipation in virtually any adiabatic logic is given by the equation:

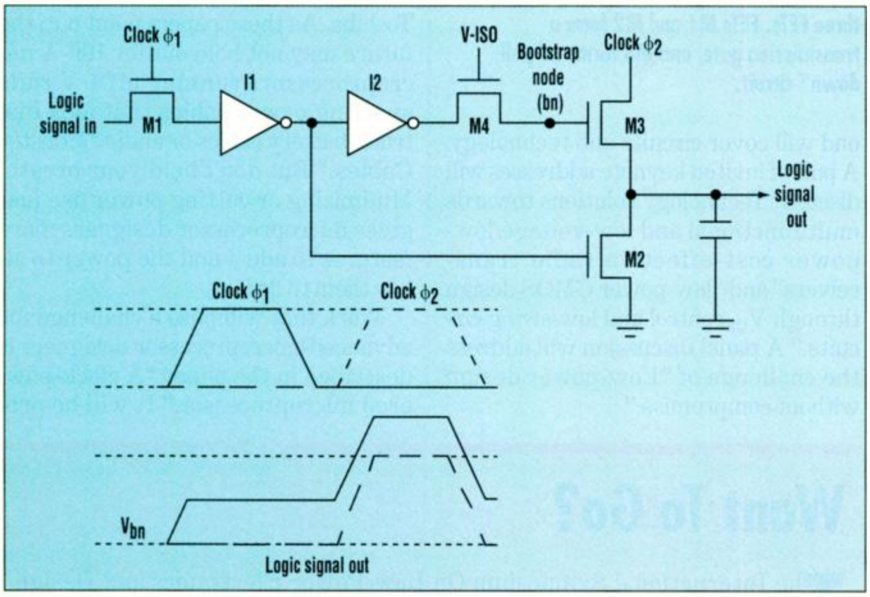


3. This inverter runs adiabatic logic with a single phase clock. Earlier designs required multiple phase clocks. Designers put 736 of the inverters and part of the power-clock generator on one chip using a 1.2-µm process. Power consumption was about half that of conventional logic.

$$E\ (\text{energy}) \approx (RC/T) \times CV^2$$

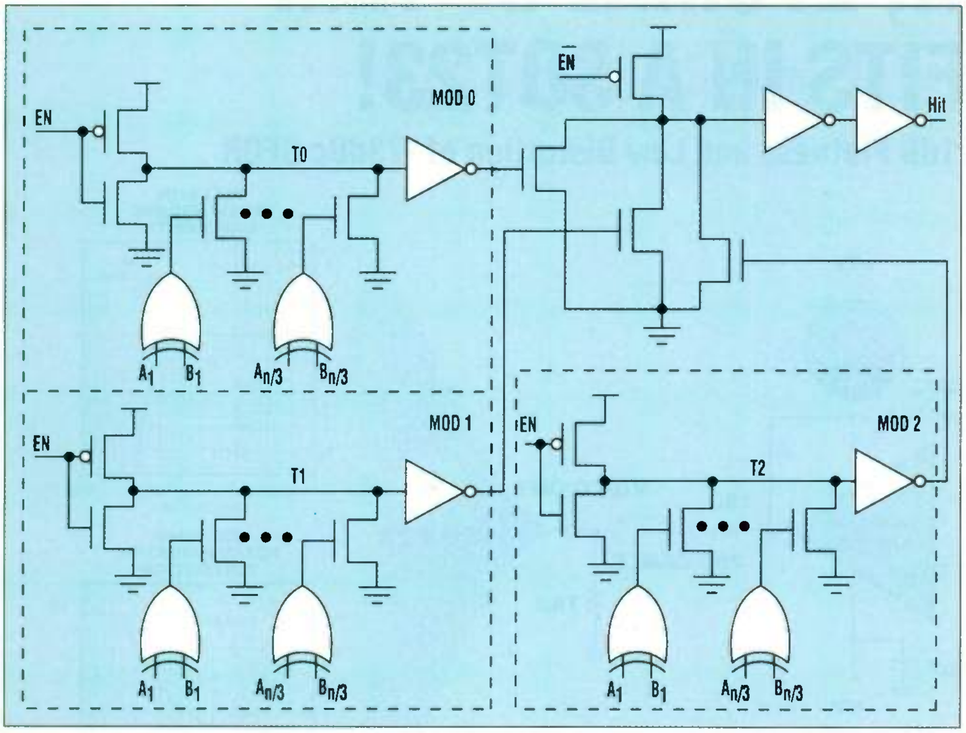
When RC is small relative to T, the energy dissipation per clock cycle becomes less than CV^2 and energy is theoretically saved. However, the practical disadvantages of adiabatic logic include the overhead circuitry required, extra capacitance which must be charged and discharged each cycle, and the fact that the logic levels must be greater than twice the process' threshold voltage.

Using Spice, the team investigated a number of circuits for optimum performance and robustness. These circuits ranged from the simple one shown in Figure 1 to the circuit finally chosen, a bootstrapped CMOS-clocked buffer shown in Figure 2. Input data is sampled on ϕ_1. The FET M1 and inverters I1 and I2 form a conventional CMOS latch. FET M4 isolates the "boot node" from the output inverter I2 when the "boot node" voltage exceeds V_{iso} + a threshold voltage. For normal operation, V_{iso} runs one threshold voltage above the inverter's supply rail. When the input goes high, the "bootstrap node" charges to the inverter's supply rail forming a channel between M3's source and drain. The rising edge of ϕ_2 raises V_{bn} along with it, via M3's gate-to-channel capacitance. When sufficient charge accumulates at the "boot node," the clock pulse passes through



2. This bootstrapped clock buffer adapted to adiabatic logic design techniques was used throughout the AC-1 microprocessor in lieu of conventional logic in order to reduce power consumption. The AC-1 is a 16-bit, 58.8-MHz, 0.5-µm, n-well CMOS processor, developed jointly by the University of Southern California, Rockwell, and Sony, that consumes just 26 mW at 1.8 to 2.5 V under these operating conditions.

Circle 134 - For U.S Response
Circle 135 - For International



4. Low-threshold-voltage logic cut power and delay in this digital comparator designed at Texas Instruments. Based on HDVT, it's called hierarchical, reduced-swing, dual V_t logic.

FET M3 (from drain to source) to the output.

The paper describes the buffer and the microprocessor's architecture, as well as additional adiabatic circuits in more detail. It also describes how the team tested the chip's performance and measured its dissipation and processor core which took close to 13,000 FETs (17% were pFETs).

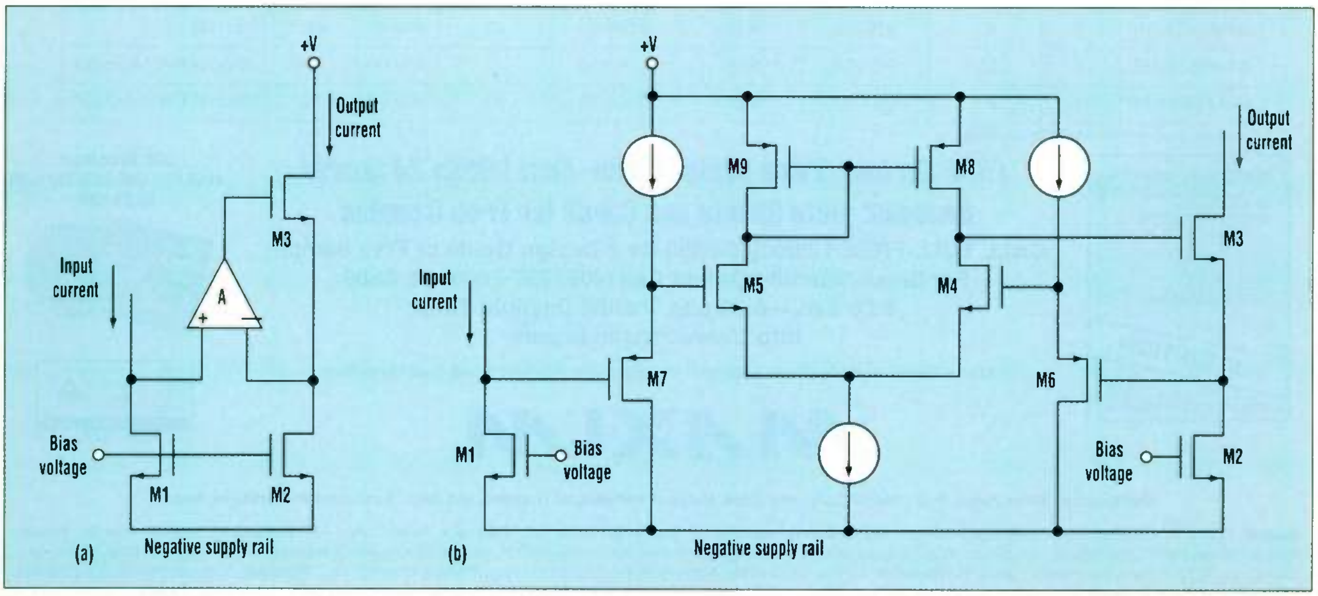
Indicative of the varieties of adiabatic logic being worked on, a paper by a team from the University of California, Davis, and the University of Colorado, Boulder, describes CMOS adiabatic logic that works with a single-phase clock/ac-power source, whereas others require a multi-phase clock. The team came up with a logic gate known as a CAL (Clocked Adiabatic Logic) Inverter *(Fig. 3)*. Cross-coupled CMOS inverters (FETs M1-M4) provide the memory function.

The team put 736 of these inverters on a single chip in a 1.2-µm process, along with part of the power-clock generator. Power consumption was roughly half that of conventional logic at 40 MHz.

Cutting The Power

As noted earlier, several major semiconductor companies are at least looking at low-power techniques. A team from Texas Instruments (TI) will present a paper describing their work at improving the performance of a 0.18-µm process running at 1.8 V. They investigated the delay, power, and area of several critical digital-library circuits needed for advanced low-power microprocessor designs.

The team worked on a proposed hybrid dual-threshold-voltage (HDVT) circuit architecture. Their goal was to increase the speed of high-threshold voltage (V_t) MOSFETs by 21% while reducing the leakage power dissipation of low-V_t FETs by an order of magnitude for combinatorial logic. Other goals were laid down for sequential logic and data paths. For data paths, the team came up with a comparator that cuts the delay by 50%



5. Low-power analog designs are in development. This 20-MΩ (output impedance) current source (a) is built with 9 MOSFETs (b) on a 2-µm CMOS process. The input impedance of the current source is close to the ideal of zero because the input FET, M1, is biased in the linear region.

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Circle 137 - For International

over any prior architecture *(Fig. 4)*. Based on HDVT, it's called a hierarchical, reduced-swing, dual-V_t logic (HHRSL).

Behind the team's goals lie some of the problems faced when going to sub-0.5-µm processes. Gate lengths and gate-oxide thicknesses drop, mandating a drop in supply voltage. However, while power dissipation drops with the square of the supply voltage, propagation delay degrades as well, as an exponential function of the supply voltage minus the threshold voltage.

As a result, to both further reduce power dissipation and propagation delay, MOSFETs sporting multiple threshold voltages are crucial, particularly when the supply voltage drops into the 1-V range. However, FETs with a low V_t must be distributed judiciously throughout a circuit or IC to maintain noise immunity and prevent subthreshold leakage currents that can increase dissipation. Early in the process, the team concentrated on chip architectures optimizing the use of dual-threshold logic (logic using MOSFETs with both high and low threshold voltages). The paper describes a variety of functions adaptable to this technology, the potential problems involved, and how to beat them. Adaptable circuits include the passgate (analog switch) multiplexer, the tri-state inverter, and sequential registers and several comparators including the HHRSL circuit mentioned earlier *(Fig. 4, again)*.

The HHRSL comparator works this way: The voltage swing of the wired-OR outputs (HO, H1, H2, HIT) are reduced when the comparator is enabled (EN = 1), then node HO rises until PO is turned off by inverters I1 and I2, which occurs when they sense the voltage on node HO. When a mismatch is detected, N6 turns on discharging node HO through the large nFET N4. If the voltage on node HO is below the trip point of inverter I3, N4 is switched off and the ratio between the pull-ups (P0/P1) and the pull-downs (N5/N6) determines the voltage on node HO. This reduced voltage swing allows for fast rise and fall times at the cost of reduced noise margins.

In addition, low-V_t FETs further cut power and up speed while cutting noise margins. This comparator is insensitive to fan-in, making it a natural for low-power, high fan-in designs.

As noted earlier, analog ICs are not immune to assaults aimed at cutting the power of basic building blocks. Papers at ISLPED '97 describe work on functions from CMOS current sources to charge-pump-assisted CMOS op amps. This includes digital-to-analog converters (DACs), 1.8-GHz voltage-controlled oscillators (VCOs), and delta-sigma frequency-to-time converters operating as demodulators.

Current sources are the basic building block in most analog ICs. Therefore, a low-power, low-voltage CMOS current source would be a boon to most analog IC designers. A paper by a team from Washington State University, Pullman, describes just such a device *(Fig. 5)*. Conceptually, the current source consists of op amp A, and a trio of n-channel MOSFETs M1, M2, and M3. The first pair are biased in nonsaturation while M3 is saturated. The ideal current source sports an input impedance of zero and an output impedance of infinity. The input Z of this current source is not zero, but is close to it because the input FET M1 is biased in the linear region. The input resistance is given by:

$$R_{in} = 1/[\beta (V_{gs} - V_t)]$$

Using this equation to design the chip provides an input resistance of about 1000 Ω and permits operation at input voltages as low as 0.1 V. Output resistance is nominally the drain-to-source resistance of M3 times the gain of the op amp. In the final implementation, it was measured to be about 20 MΩ, making it suitable for use in DACs and op amp bias circuits. The final current source was implemented in a 2-µm n-well CMOS process. The amplifier consists of M2, M3, M4, M5, M6, M8, and M9. The p-FET level shifters (M6 and M7) set the dc-output voltage to keep M3 in saturation and keep the output voltage high. The presentation at the conference will show the current source used to develop the "tail" current of an op amp's differential input stage and as a bias-current source.

HOW VALUABLE	CIRCLE
HIGHLY	570
MODERATELY	571
SLIGHTLY	572

Circle 138 - For U.S Response
Circle 139 - For International

Board-Level Connectors For High-Speed Systems

Long Considered A Mechanical Problem, These Connectors Are Now At The Forefront Of Design As Transfer Rates Climb Into The Hundreds Of Mbytes/s.

SCOTT MICKIEVICZ, AMP Inc., MS 39-01, P.O. Box 3608, Harrisburg, PA 17105-3608; (717) 592-6439.

With new generations of logic devices offering twice the speed of the generation before it, designers are being forced to carefully evaluate the entire signal path of these high-speed systems to avoid problems. An often-underestimated weak link is the connector, which frequently has to deal with hundreds of tightly packed signal lines that can be switching in the gigahertz range. As a result, the electrical characteristics of the connector, and its effect on signal integrity, have come under close scrutiny.

Factors to be considered include impedance mismatches, trace routing, skew, and parasitics due to the affects of inductance and capacitance, and the pc-board material itself. Their effects have led to the emergence of two popular connector topologies—open-pin field and controlled impedance—with their respective advantages of high density and high performance. Depending on the particular application, a combination of the two or a single connector, appropriately partitioned, may be the optimum solution.

Defining High Speed

The first priority is to determine whether the system falls under the rather broad umbrella of high speed. The term high speed itself can be an ambiguous term, used by different people to mean different things. From our perspective, when discussing high speed we are referring to a system in which transmission-line effects must be accounted for. Edge rate is the key here. When the round trip of the signal is longer than the edge rate, the line must be analyzed as a transmission line. In practical terms, the maximum permissible signal path is a generous 15 cm at a 2-ns edge rate, but only 2 cm when edge rates decrease to 250 ps *(Fig. 1)*. The point at which this critical length is exceeded, is the point at which transmission-line design rules start to apply.

Once the expected data rate has been defined, the variety of available two-piece backplane connectors gives designers an array of options. Two popular choices are open-pin-field connectors and controlled-impedance connectors. The latter use ground planes between columns or rows of pins to achieve stripline or microstrip configurations, similar to those used in pc boards. Just like a pc-board design, a key system design technique is controlling the impedance to reduce reflections, ringing, and other unwanted effects of impedance mismatches.

Comparison Of Options

Each connector type has certain advantages in terms of speed, signal density, signal integrity, and cost. A brief comparison of some common AMP two-piece connectors used in high-speed backplane applications is given *(see the Table)*. The basic difference in configurations between open-pin-field and controlled-impedanceconnectors is depicted *(Fig. 2)*.

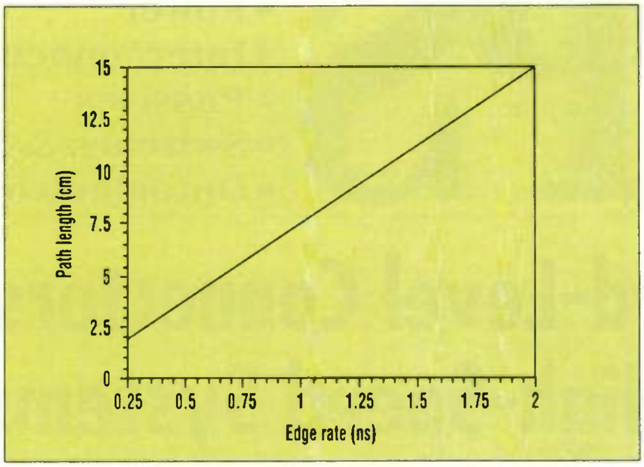
Connectors using open-pin fields have long been the choice for board-to-board applications. As both the signal-to-ground ratio and the arrangement of signal and ground pins affect pulse fidelity, high-speed pulse propagation in these connectors can be improved

TYPICAL TWO-PIECE BACKPLANE CONNECTOR OPTIONS

Type	Connector	Spacing (row by column)	Number of rows	Number of pins
Controlled impedance	SL 100	0.100 by 0.100 in.	4	40 signal pins/in.
	HS3	2 by 2.5 mm	0	100 signal pins/in.
Open-pin field	2-mm HM	2 by 2 mm	5, 5 + 2*	62 pins/in.
			8, 8 +2*	100 pins/in.
	2-mm HM	1.5 by 2 mm	12	150 pins/in.

The "+2" configuration includes a shield as the two outer rows.

by assigning more pins to ground to reduce the circuit impedance. The best arrangement is a staggered signal-ground-signal-ground arrangement to prevent crosstalk between lines *(Fig. 3)*. However, as signal rise times become faster, more pins must be allocated to ground. At rise times over 10 ns, a 5:1 ratio usually provides adequate performance. At 3 to 10 ns, the recommended ratio becomes 3:1. At even higher speeds, a 1:1 ratio is advisable.



1. With data rates running into the hundreds of megabytes/s, high-speed signal pathways are behaving increasingly like transmission lines, and must be analyzed accordingly. When the combination of edge rate and path length falls into the area above the diagonal line, transmission-line design rules apply.

The obvious disadvantage is that up to half the connector resources are dedicated to ground. This is contrary to the desire for high-packaging densities since half the pins are "wasted" to achieve signal-transmission quality. The solution is to offer a built-in ground plane to control impedance and reduce crosstalk. This is the key design advantage of controlled-impedance connectors and it provides greater efficiency in terms of signal pin use as all signal pins are available for signal-carrying purposes.

As with any component, connector selection must be weighed against application requirements. Open-pin-field connectors offer the highest pin density, but the density of usable signal pins will vary with the signal-to-ground ratio. But by carefully selecting the connector, partitioning signals, and assigning grounds prudently, these connectors will meet a wide range of needs well into the picosecond range. Controlled-impedance connectors extend performance even further, making them the choice for high-end applications pushing the envelope of performance and density. Plus, they have a constant signal-pin density since pins don't have to be assigned to ground.

Packaging Density

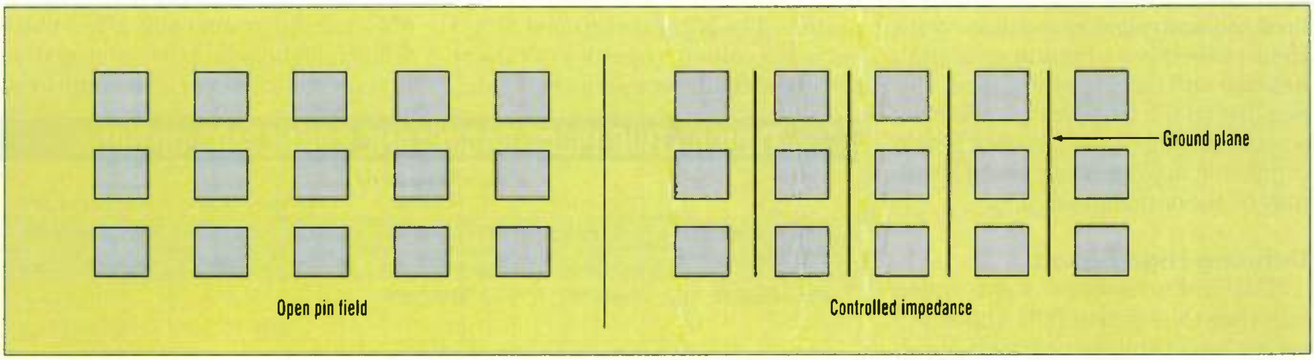
The drive toward higher densities in packaging includes connectors, of course. But because a connector also is a mechanical device, there are some practical limits on size. Backplane connectors typically have centerline spacings of 2.0 mm or 2.5 mm between pins. A common measure of a connector's capability is the number of pins it provides per linear inch, and more importantly, the number of signal pins. The number of signals per linear inch directly affects the practical size of boards having requirements for a large number of I/Os. While traditional connectors offer four rows of pins, newer designs are now offering eight or ten to provide a greater signal density per linear inch.

While conventional wisdom may say that a 2.0-mm connector is better than a 2.5-mm connector when it comes to packaging density, conventional wisdom isn't always right. The prudent designer must consider a number of factors before making a connector decision. Since conventional wisdom would favor the 2-mm connectors, let's look at the case for the 2.5-mm connectors.

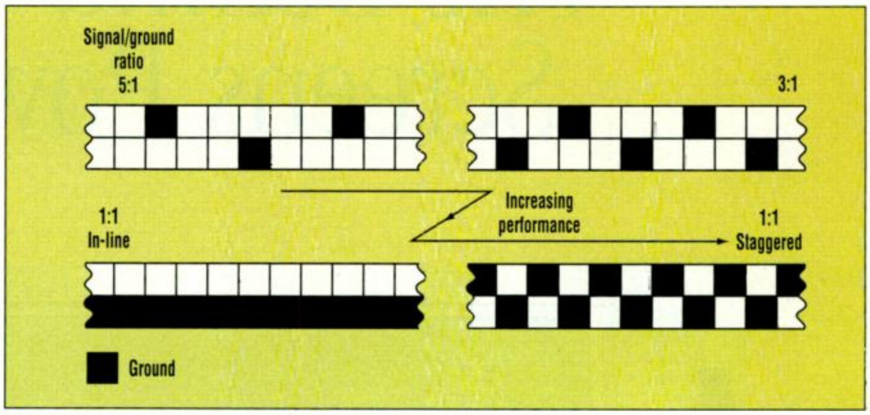
Trace routing—A 2.5-mm pin spacing makes it easier to route traces between the pins. Easier trace routing can result in fewer board layers, fewer problems in resolving problems with skew from uneven path lengths. It also allows multiple traces to run between pins.

Skin effect—Another consideration affecting trace routing at high speeds is skin effect. At the very high frequencies of emerging communication systems like Sonet and Fibre Channel, the small cross-sectional area of traces can produce significant skin-effect losses as the energy propagates only on the outside of the conductor. Skin effects can be reduced by using larger traces. A 2.5-mm spacing will allow larger traces with more convenience. Here again, new dielectric materials allow greater design flexibility in trace widths and the thickness of board layers since the height and width of the trace is a factor in determining characteristic impedance.

Skew—An important effect that must be considered in designing a con-



2. Controlled-impedance connectors use ground planes between each row of signal pins to provide a consistent impedance and a constant number of signal pins per inch. This design gives such connectors the edge in overall performance.



3. Signal integrity in a high-speed circuit requires generous use of ground pins. The highest-speed circuits require a 1:1 staggered relationship of signal to ground pins.

nector into the system. Since each row of a connector typically has a different length, due to the right-angle daughtercard connector, the connector introduces skew if multiple rows are used for parallel data. Skew can be easily corrected by introducing different compensating path lengths in the board traces.

Capacitance—Large backplane connectors are through-hole devices using plated-through holes (PTH). The capacitance of the PTH is a function of the surface area of the hole and the dielectric constant of the board material. Since thick boards have deep PTHs, the increase in surface area increases the capacitance. Higher capacitance is of concern for two reasons: It can slow the rise time of a signal, and it can increase crosstalk from capacitive coupling between lines. A larger separation between pins decreases the coupling and lowers crosstalk.

Alternative board materials can be used to lower capacitance (and to provide faster propagation speeds). The choice of board material directly affects board stackups allowed to maintain the required impedances. Traditional FR-4 fiberglass epoxy boards have a relatively high dielectric constant of 4.5, which directly limits how thin board layers—and by extension PTHs—can be. Characteristic impedance for microstrip and stripline circuits, after all, is determined solely by the geometrical relationship between the signal line and ground plane and by the dielectric constant of the material separating them. Other materials, such as Teflon, GETEK, and Rogers 3000 PTFE, have lower dielectric constants—around 3 or less—that will allow thinner multilayer boards to be fabricated.

Partitioning Resources

Since the signal-to-ground ratio in a connector depends on the edge rate of the signals, the designer should carefully evaluate the needs of various signals. High-speed signals with picosecond edge rates require a 1:1 ratio. Lower-speed signals, including control signals, can get by with fewer ground pins. The same signal-to-ground ratio does not have to be consistent throughout the connector. Slow-speed signals can be allocated to one end of the connector at a 5:1 or 3:1 signal-to-ground ratio. High-speed signals at a 1:1 ratio also can be grouped together.

Depending on the system, several levels of partitioning can be used. Such partitioning makes more effective use of available connector resources by reducing the number of pins dedicated to ground. An alternative is to use more than one connector. For example, use a controlled-impedance connector for high-speed signals and an open-pin-field connector for medium- and low-speed signals.

Scott Mickievicz graduated from Penn State University with degrees in physics and mechanical engineering. He has worked with AMP as a mechanical engineer since 1993.

HOW VALUABLE	CIRCLE
HIGHLY	560
MODERATELY	561
SLIGHTLY	562

UPDATE: BOARD-LEVEL CONNECTORS & SOCKETS

Manufacturer	Device	Description	Price & availability	CIRCLE
3M, Electronic Products Div. **Austin, Texas** **Sales Dept. (800) 328-0016 ext.111**	303 Series	Low-profile shrouded headers come in eight popular sizes and in straight or right-angle versions with one-size tail and wipe-area length. Features include gold flashing and end windows for screwdriver disconnect assistance.	34 positions, straight;$0.362 each per 1000.	573
Aries Electronics Inc. **Frenchtown, N.J.** **Frank Folmsbee (908) 996-6841** **fax (908) 996-3891**	Series 931/941	Series 931 are horizontal and vertical lock/eject box headers, while Series 941 are vertical and right-angle box headers on 0.100-in. centers. Both use the company's Series 981 IDC receptacles and come with 10 to 64 pins, brass-alloy contacts, and a contact resistance of 30 mΩ max.	10-pin, Series 941, $0.17 each per 1000; 5 weeks ARO.	574
	RF Sockets	Test sockets target for QFPs target ultra-high-frequency applications of 10 GHz and above and feature a patented microstrip technology. The sockets have a loss of 1 dB at 10 GHz, a self inductance of less than 0.01 µH, and can be used at temperatures from -65° to 170°C.	84 pins, $1.700 each for four; 4 to 6 weeks ARO.	575
Circuit Assembly Corp. **Irvine, Calif.** **Monica Allphin (714) 855-7887** **fax (714) 855-4298**	CA-MRS Series	This line of Micro Ribbon Sockets features a proprietary IDT blade-to-blade contact design and is configured as a cable-mount mating connector for SCA, SCA-2, and VESA interfaces. Comes with a two-piece convoluted cover and retainer for easy assembly. Available positions range from 68 to 80.	$99 each in quantity. 12 to 16 weeks ARO.	576
Comm Con Connectors Inc. **Duarte, Calif.** **Robert Farnum (818) 301-4200** **fax (818) 301-4212** **http://www.commcon.com**	Caterpillar headers	This line of caterpillar headers come with 2-mm, 0.050-in., and 0.100-in. center spacings, with up to 40 pins per assembly. The end-to-end stackable headers feature high-temperature plastic construction for temperatures up to 260°C and use tin-plated contacts.	$0.02 per contact; available now.	577
EDI Corp. **Las Vegas, Nev.** **Milos Krejcik (702) 735-4997** **fax (702) 735-8339**	28D3/SO-SD 28D6/SO-SD	Targeting 300- and 600-mil-wide DIP plugs, respectively, these emulator adapters for microcontrollers in SOIC packages come in two parts. One part solders to the pads in place of the package; the other part attaches to the emulator plug. All contacts are always aligned and coplaner with no wicking.	Both types are $108; stock.	578
ELCO Corp. **Myrtle Beach, S.C.** **Sales & Mktg. (803) 946-0414** **fax (803) 626-5186**	Press-fit DIN	Right-angle press-fit DIN connector eliminates the secondary soldering operation with the company's VARIPIN compliant pin that mates directly with the through hole of the pc board. Available with 2, 3, 4, or 5 rows, the connector contact uses gold over palladium nickel.	$0.02 to $0.03 each per 100,000; stock to 9 weeks.	579
Fujitsu Takamisawa America Inc. **Sunnyvale, Calif.** **Sales Dept. (800) 380-0059** **fax (408) 745-4971** **http://www.fujitsuta.com**	FCN-078 Series	Available in 144-position (single slot) and 2 by 72-position (dual-slot, stacked) versions, this line of surface-mount socket connectors targets SO DIMM applications (8 to 16 Mbytes). Both feature dual, positive-locking mechanisms for each slot, as well as latches for stabilization. Packaging is in trays for automatic pick-and-place equipment.	144 positions, $4.45; 2 by 72-pin, $4.65 each per 10,000.	580
Methode Electronics Inc. **Rolling Meadows, Ill.** **Sales Dept. (847) 392-3500** **fax (847) 392-9404**	Header 8	Designed to accept voltage regulator modules, this header targets low-voltage Pentium Pro processor applications. The header is made from high-temperature plastic, high-performance, gold-plated copper-alloy contacts, and die-cast latches.	Under $2 in quantity; 4 weeks ARO.	581
Mill-Max MFG. Corp. **Oyster Bay, N.Y.** **Carla De Riso (516) 922-6000** **fax (516) 922-9253**	Series 114-117	Specifically designed to improve surface-mount soldering joints, these stub-tail DIP sockets feature a unique floating contact with 0.008-in. vertical travel. Each pin reacts to capilliary action, thus ensuring voidless joints. The sockets have a profile of 0.166 in. and tolerate temperatures of up to 215°C.	16 positions, gold plated, $0.79 each per 1000; 7 days.	582
Molex Incorporated **Lisle, Ill.** **Sales Dept. (800) 78-MOLEX** **fax (630) 969-1352**	EBBI SCA-2	These SCA-2 connectors attach disk drives to backplane arrays in servers and RAID systems through a single connector interface.The receptacles feature blind-mating guides, integral grounding contacts, and are designed for use with 2.5- to 3.5-in. SCSI and Fibre Channel disk drives.	40 circuits, $1.91 each per 50,000; four weeks ARO.	583
Ranoda Electronics Inc. **Miami, Fla.** **Lawson Williams (305) 593-0129** **fax (305) 594-3973**	Ultra-SCSI	The three-in-one Ultra-SCSI connector doubles pin density to 0.050-in. centers, increases data pin count from 50 to 68, and doubles user pins to 12. The connector handles temperatures up to 260°C and currents of 1 A for data lines and 3 A for power lines. Power-line contacts are on 0.2-in. centers.	$1.60 each per 200,000; 2 to 3 weeks ARO.	584
Samtec Inc. **New Albany, Ind.** **Danny Boesing (800) SAMTEC-9** **http://www.samtec.com**	TOLC and SOLC Series	The high-density TOLC quad-row terminal strips mate wth the SOLC stamped socket strip to provide up to 200 I/Os in less than one square inch. Stack height choices are 6.35, 8, 10, and 12 mm and the devices are a drop-in replacement for other stamped and formed connectors.	$0.10 per mated line; less than 3 days.	585
Thomas & Betts Corp. **OEM Division** **Memphis, Tenn.** **Sales Dept. (800) 344-4744**	F1D Series	These one-piece, fine-pitch (0.050-in. centerline) cardedge connectors feature cantilever beam contacts with up to 150 dual positioned signal and ground pins in an alternating array. The connectors handle 500-ps rise times and limit near-end crosstalk to 5% with an impedance of 50 Ω.	$7.35 each per 1000; stock to 4 weeks ARO.	586
	Series A and Series B USB Connectors	Designed to provide a single shielded "plug-and-play" solution for peripherals, these receptacles have options that include single or stacked, right-angle or vertical, and come standard in a through-hole design. An SMT version is coming. A back shield provides enhanced EMI or RFI protection.	$0.50 each per 10,000; 4 weeks ARO.	875
WPI/Garry Electronics **Salem, N.J.** **Bill Alman (609) 935-7560** **http://www.WPI-Interconnect.com**	ZIF Sockets	This line of ZIF sockets features a snap-lock mechanism to ensure high retention force with zero-insertion/withdrawal forces. Other features include a wiping action, low profile, inclined contact design, and a side-to-side spacing of 0.100 in. between ICs. Up to 12 sizes are available.	From $3 to $5; available now.	588
Wells Electronics Inc. **South Bend, Ind.** **Sales Dept. (219) 287-5941** **fax (219) 287-0356**	Series 680	Offering a small socket outline for efficient use of burn-in board real estate, these test/burn-in sockets are specially designed for QFPs. The devices feature an open-top, ZIF design and tolerate temperatures up to 150°C. Sockets are available for the 14 by 20, 100-lead QFP.	$45 each per 100; available now.	589

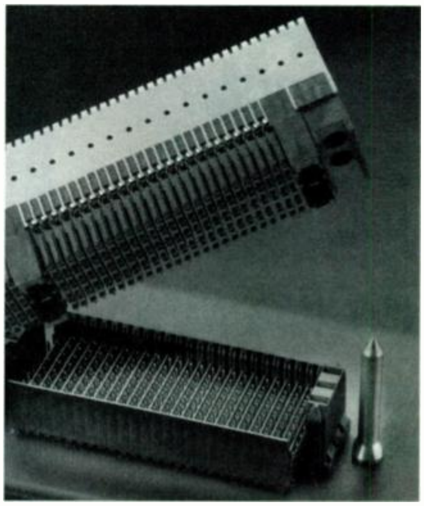
PRODUCT FEATURE

Backplane Connector Compresses Up To 101 "Real" Signals Per Linear Inch

Struggling to satisfy escalating I/O demands, many interconnect designers are slamming against the basic laws of physics that limit the number of high-speed signals can fit in a given area without an appreciable degree of signal degradation. Already approaching the limits of present-day board or backplane connector technology, board designers are welcoming any solution that promises to extend the capabilities of their systems. One possible answer could be the Very High Density Metric (VHDM) connector developed by Teradyne Inc.

Offered as the next generation in backplane interconnects, the VHDM is a controlled-impedance connector that comes in six- and eight-row versions and packs up to 101 "real" signal pins per linear inch. With its integral continuous shielding, the VHDM permits all available pins to be used for transmission of signals with rise times down to 200 ps.

The connector uses press-fit contacts on both sides of halves of the terminating interfaces. The daughtercard pin spacing is on a 2- by 2-mm grid while the separable interface and backplane press-fit pin spacing is 2 by 2.25 mm. Features include a high-temperature, glass-reinforced polymer for the connector insulators and C7025 contact material to achieve a contact resistance of 10 mΩ for the A row and 20 mΩ for the H row. Other specifications include a signal contact engagement force of 0.4 N (typical), a contact life of 250 cycles, a signal current rating of 1 A continuous at 70°C, and a voltage rating of 750 V. A modular design provides for flexibility in layout and configuration. Pricing is $0.18 per mated line. Small quantities will be available in the fourth quarter of this year. Production quantities will be available in early 1998.



Teradyne Inc., Connection Systems Div.
44 Simon St.
Nashua, NH 03060
Colleen Gross (603) 791-3573
fax (603) 791-3050
morrison.wayne@tcs.teradyne.com

CIRCLE 590

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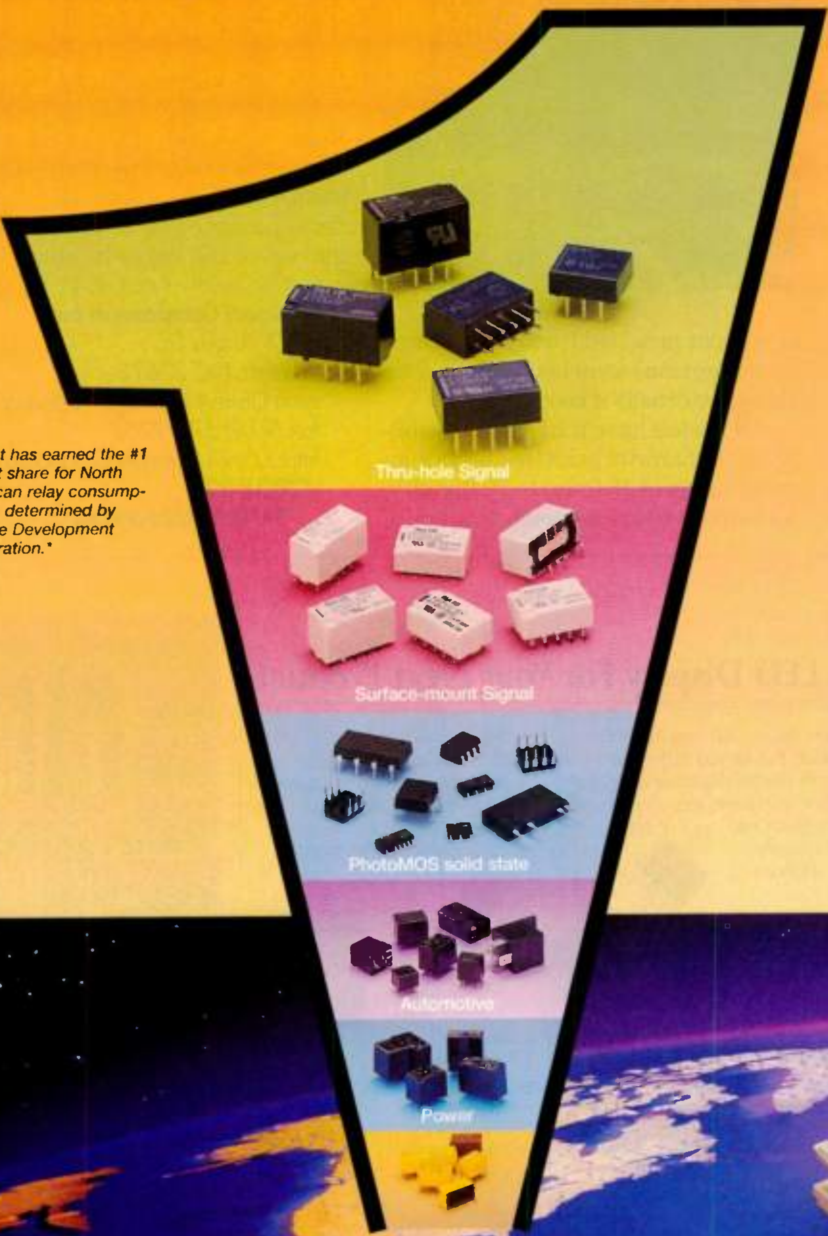

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READER SERVICE 121

PRODUCT FEATURE

10- To 40-W Dc-Dc Converters Push Price/Performance Envelope

Newport Components Inc. Raleigh, N.C., has introduced a line of 10- to 40-W dc-dc converters that promises to set new standards for price and performance for such devices. A longtime leader in the sub 5-W market with its M Class, D Class, and TM Class (surface-mount) converters, Newport has recognized the current and future market for higher-power dc-dc converters, especially in industrial control, instrumentation, telecom, and datacom applications.

Dubbing its line the NPH Series, Newport kicks off its debut with the NPH15S, a 15-W, isolated converter that measures 50 by 25 by 10 mm and comes with an efficiency rating of 89%. The converter features a constant frequency of 350 kHz to minimize filtering requirements, an input-to-output isolation of 1500 V, an industry-standard pinout, and a surge rating to over 25 W. Protection includes over temperature and non-latching current limiting to ease starting into difficult loads. While reverse-polarity protec-

tion is not provided (to save on power consumption) a series diode can be added externally if necessary.

All models have a 2:1 input capability with characteristics that include an input range of 18 (min) to 72 (max) V, an output voltage setpoint accuracy of 0.5%, a line regulation of 0.1%, and a load regulation of 0.5%. In situations where higher power or N+1 redundancy is required, the NPH line has optional synchronization. Synchronization is achieved by supplying a negative-going pulse, typically 9 V and of 150-ns duration, to one of several optional control pins provided on each side of the barrier. The signal is applied via a 1-nF capacitor and a 9.1-V zener diode connected between the pin and the primary common terminal.

Other control inputs include: voltage trimming on the secondary side which allows voltage adjustment within the capabilities of the power circuit; a shutdown control to stop the converter and keeps its current consumption below 1 mA at 48 V.

Newport Components Inc.
6321 Angus Dr.
Raleigh, NC 27613
Lynn Dismuke (919) 571-9405;
fax (919) 571-9262
http://www.newport.co.uk/ed
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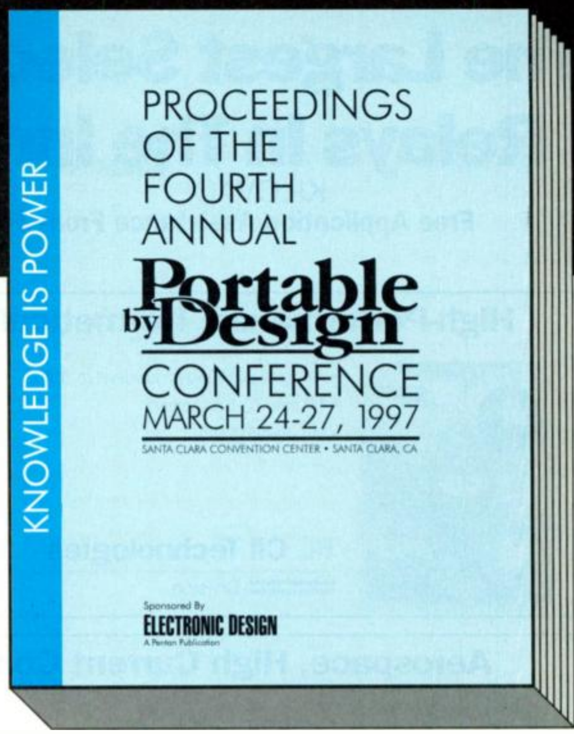

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PASSIVES & OPTO

Low-Resistance Resettable Fuses Target Telephones

The TR600-160-RA-B-0.5 PolySwitch line of resettable fuses have on-resistances ranging from 4 to 7 Ω and are binned so that all parts in a single pack-

age are within 0.5 Ω of each other. Targeting ISDN, HDSL, and ADSL applications, the fuses have a 60-V operating voltage, a 600-V maximum interrupt voltage, a 0.16-A hold current, and a 3-A maximum interrupt current. Agency approvals include UL1459, Bellcore 1089, FCC Part 68, UL, and CSA. The footprint is 16 by 10 mm and the device height is 12.6 mm above board. Typical pricing is $0.45 each depending on volume; delivery is six to eight weeks.

Raychem Corp., Electronics Div., *300 Constitution Dr., MS 110/7568, Menlo Park, CA 94025-1164; Sales Dept. (800) 227-7040; http://www.raychem com.* CIRCLE 592

Low-Power Fiber-Optic LEDs Have High Brightness

The IF-E96 and IF-E97 are low-power and high-brightness red LEDs, respectively, that mate with standard, 1000-µm-core, plastic optical fiber cable. The devices feature an internal micro-lens for efficient coupling, a connectorless interface, an output wavelength of 660 nm, and a spectral bandwidth of 20 nm. The IF-E97 outputs up to 300 µW, has a switching time of 0.5 µs and a forward voltage drop of 1.7 V(max), and dissipates up to 100 mW. The IF-E96 outputs up to 125 µW, has a switching time of 0.1 µs and a forward drop of 1.8 V(max), and dissipates up to 60 mW. Both devices have a capacitance of 30 pF. Pricing is from $1.60 to $4.73 and delivery is from three weeks or less.

Industrial Fiber Optics, *627 S. 48th. St., Suite 100, Tempe, AZ 85281; Sales Dept. (602) 804-1227; fax (602) 804-1229.* CIRCLE 593

PASSIVES & OPTOELECTRONICS

Board-Mount Potentiometers Have Low Noise

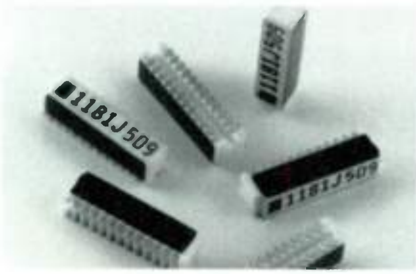
The XV092 Series of low-profile board-mount potentiometers target professional and consumer audio ap-

plications. The devices offer snap-in mounting in both vertical and horizontal configurations and feature a unique film element to reduce noise and wobble characteristics. The series' total resistance ranges from 5 to 500 kΩ in linear, audio, and reverse-audio tapers. The maximum operating voltage is 50 V ac or 20 V dc and the power rating is 0.05 W. Total rotational angle is 300°. Pricing starts at $0.20 each in quantities of 5000.

Noble USA Inc.*, 5450 Meadowbrook Industrial Court, Rolling Meadows, IL 60008; Tom Guarise (847) 364-6038; fax (847) 364-6045; http://www.nobleuse.com.* **CIRCLE 594**

In-Line Resistor Network Has Narrow Termination Pitch

The Series 753 surface-mount resistor networks, which come in a 24-pad device with 22 bussed resistors, feature a



termination pitch of 0.025 in. The networks are suited to operating frequencies over 1 GHz. A 12-pad version also is available. Pricing is less than $0.80 each in production quantities.

CTS Resistor Networks*, 406 Parr Rd., Berne, IN 46711; Sales Dept. (219) 589-3111; fax (219) 589-3243; http://www.ctscorp.com*
CIRCLE 595

AlInGaP LED Lamps Are Low Cost

Offered as a new industry price/performance standard for high-brightness LEDs, the HLMP series of AlInGaP lamps come in 5-mm (T 1) and 3-mm (T 1-3/4) versions. The LEDs come with output wavelengths of 626 nm (red), 615 nm (orange), and 590 nm (amber) and with output intensities and viewing angles ranging from 180 to 1100 mcd and 15° to 110°, respectively. The forward current is 20 mA. Packaging options include clear, diffused, and tinted lenses. Pricing is $0.10 each per million.

Hewlett-Packard Company Inquiries*, 5301 Stevens Creek Blvd., P.O. Box 58059, Santa Clara, CA 95052-8059.*
CIRCLE 596

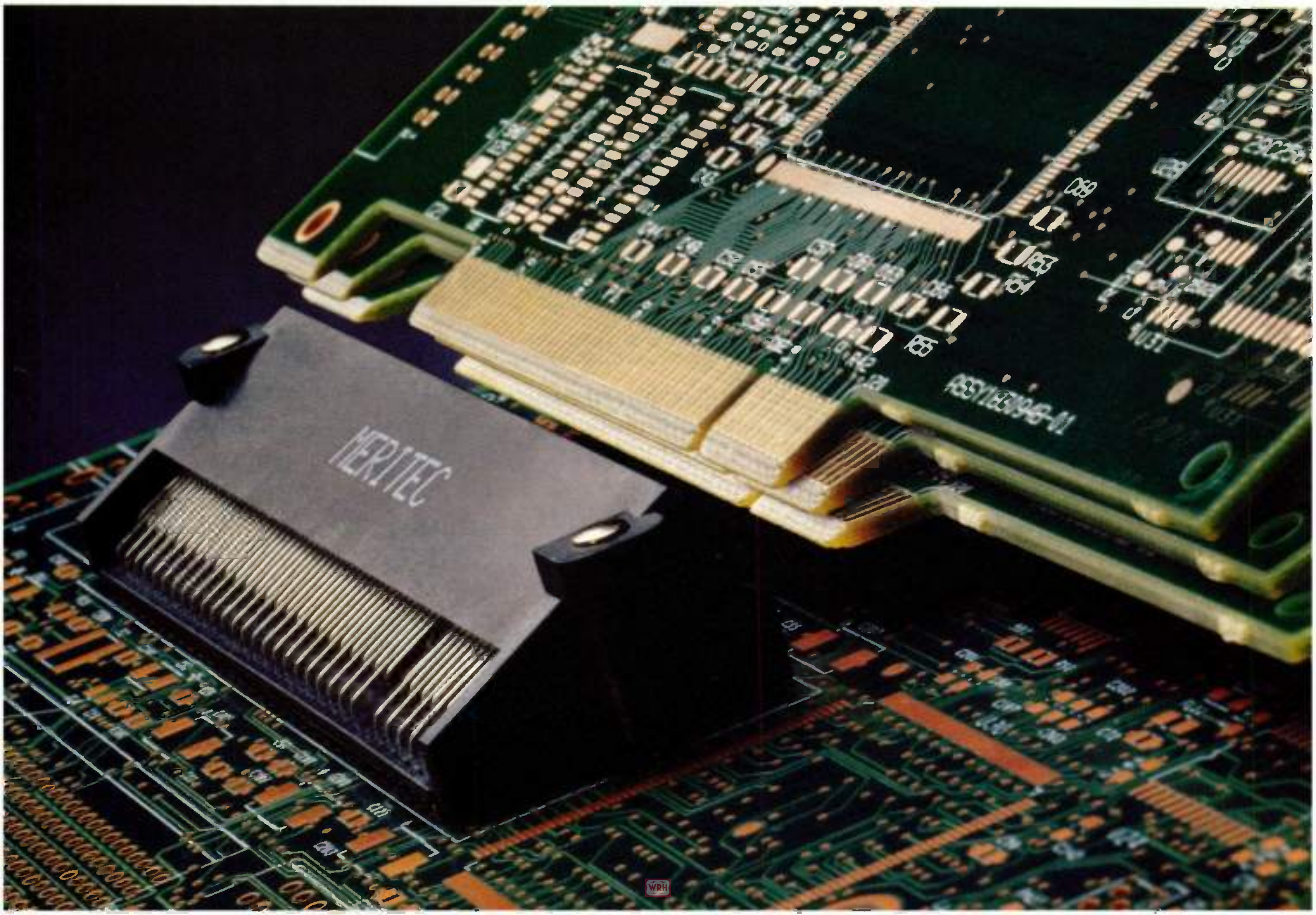
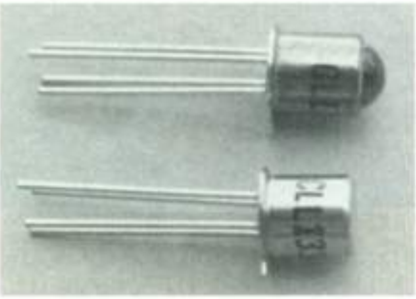


Photo IC Comes With Adjustable Gain Control

Offered as the first adjustable gain-control photo ICs, the CLL133 and CLL133W allow designers to select the optical sensitivity at which the sensor output changes state. Available



with a domed glass lens or a flat window glass lens, respectively, the devices have an adjustable range of 7:1. The V_{CC} range is 4.5 to 18 V, maximum supply current is 3.5 mA, and the output sinks 16 mA at 400 mV max. The devices track an 880-nm infrared diode and have typical optical thresholds of 40 and 480 nW, respectively. Pricing is $2.08 each for the CLL133 and $2.02 each for the CLL133W in lots of 1000. Samples are available from stock.

***Clairex Technologies Inc.**, 1845 Summit Ave., #403, Plano, TX 75074; Albert Bomchill (972) 422-4676; fax (972) 423-8628; http://www.clairex.com*

CIRCLE 597

Miniature Transceiver Module Is IrDA-Compliant

Engineering samples are now available of the the MiniSIR2 IrDA 1.0-compatible miniature transceiver module. The 115.2-kbit/s transceiver comes in a leadless SMT package measuring 9.4 by 3.8 by 3.8 mm and is housed in a metal shield for maximum EMI protection. Although the module is IrDA-1.0-compatible, it also is capable of data rates up to 1.152 Mbits/s. The module operates off a supply voltage as low as 2.7 V, requires 90 µA, and can drive a 40-pF load at CMOS/TTL levels. Agency approvals include CENELEC EN60825-1 and IEC TC76825-1 for Class 1 certifications. Shipping is tape and reel. Pricing is $2.59 each per 50,000 per year.

***Novalog Inc.**, 151 Kalmus Dr. K-1, Costa Mesa, CA 92626-5975; John Chimoures (714) 429-1120; fax (714) 549-5711; http://www.novalog.com.*

CIRCLE 598

LED Line Breaks Through Cost Barrier

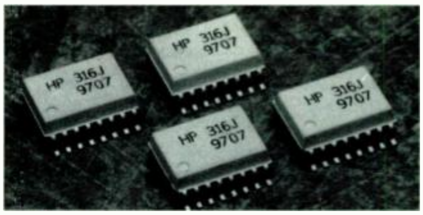
The Hi-Value line of T 1 and T 1-3/4 LEDs are offered as the first such devices to break the 3-cent barrier, in quantity, to date. Available with diffused lenses in wavelengths of 695 (red), 565 (green), and 585 (yellow), the devices' low cost is the result of the elimination of gold wherever possible, along with the addition of two high-speed lines to produce 500,000 per day. Pricing is less than $0.03 each per 10,000.

***Lumex Opto/Components Inc.**, 290 E. Hellen Rd., Palatine, IL 60067; Sales Dept. (800) 944-2790; fax (847) 359-8904; e-mail: sales@lumex.com; http://www.lumex.com* **CIRCLE 599**

PASSIVES

Gate-Drive Optocoupler Supplies Up To 2.0 A

The HCPL-316J gate-drive optocoupler supplies up to 2.0 A and comes with integrated desaturation detection and fault-status feedback. Other features include user-configurable inverting, noninvert-

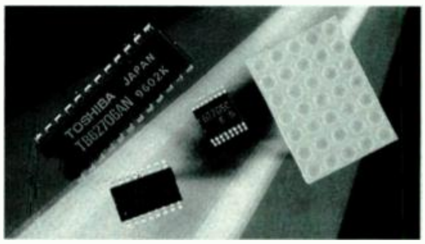


ing, automatic reset, and automatic shutdown functions. The operating voltage range is 15 to 30 V, and the switching speed is 500 ns. The device comes in a 16-pin surface-mount package with 15 kV/µs minimum common-mode rejection. UL, CSA, and VDE 0884 approval apply. Pricing is $2.90 each per 5000.

Hewlett-Packard Company, Components Response Center*, 3175 Bowers Ave., M/S 88U, Santa Clara, CA 95054-9929; (800) 537-7715 ext.9935; http://www.hp.com.* **CIRCLE 600**

Color LED Display Exhibits A High Level Of Uniformity

To overcome the problems associated with achieving optimum bi-color dot-matrix display uniformity, the HIPER display combines carefully screened LEDs with Toshiba's constant-current driver series. The combination enhances display performance by effectively elim-



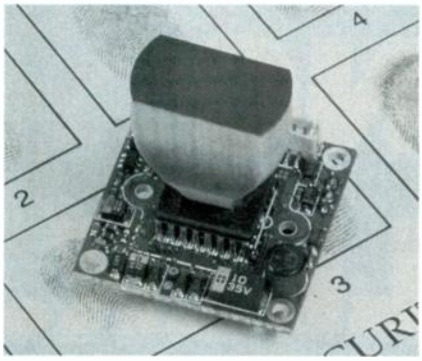
inating the variables that contribute to brightness and color inconsistencies. The displays come in 0.8- to 5-in. sizes with matrices of 4 by 4, 5 by 7, 5 by 8, 8 by 8, and 16 by 16 LEDs. Pricing starts at $1.95 per 10,000, depending on size.

Marktech Optoelectronics*, 5 Hemlock St., Latham, NY 12110; Carrah Daley (800) 98-4LEDS; fax (518) 786-6599; e-mail: marctek@aol.com* **CIRCLE 601**

PASSIVES & OPTOELECTRONICS

Miniature Fiber-Optic Image Sensor Combines All Functions

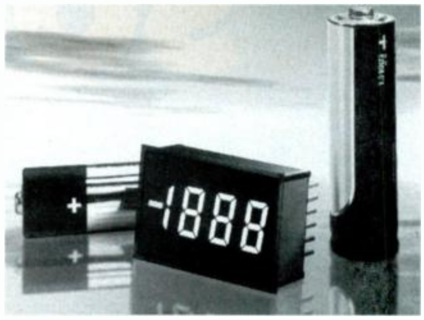
The FO-CCD series of black-and-white image sensors combine a CCD, power supply, and fiber-optic connector on a pc board measuring 32 mm^2 by 18 mm high. The modules have a resolution of 121 lines/mm, can be



specified with or without EMA, and are available with straight or tapered fiber optics that deliver magnification to 3X. The pixel format of the 1/3-in. CCD is 512 by 492 and the module runs off 9 V dc which is supplied via an on-board connector. Targeted markets include fingerprint identification in financial terminals and security for medical information. Pricing is $325 in quantity.

***Hamamatsu Corp.**, 360 Foothill Rd., Box 6910, Bridgewater, NJ 08807-0910; Sales Dept. (800) 524-0504; fax (908) 231-1218.* **CIRCLE 602**

LED Panel-Meter Display Has Low Power Requirements



The DMS-20PC-RL Series 3-1/2-digit panel meter comprises 0.37-in., bright-red LED displays and consumes 7 mA from a 5-V supply. Standby operation reduces current drain to 0.5 mA. Readable from up to 15 ft., the meter measures 35 by 12 by 22 mm and has an operating temperature range of 0° to 60°C. The available differential input voltages are ±200 mV, ±2 V, ±20 V, ±200 V and the input impedance is 1 MΩ or 1000 MΩ depending on input voltage range.The CMRR is typically 86 dB. Display test and display enable functions are also included. When the display is disabled, the meter's current drain drops to 0.5 mA, allowing it to be used with battery-operated equipment. Meanwhile, the internal analog-to-digital converter remains operational so that when the display is turned back on, no warm-up time is required. standard. Pricing is $31 each per 100 and delivery is four to six weeks.

***Datel Inc.**, 11 Cabot Blvd., Mansfield, MA 02048; Roy Cabral (508) 339-3000 ext.152; fax (508) 339-6356; e-mail: rcabral@mcimail.com*

CIRCLE 603

The IEEE P1451.2: A Smart Transducer Interface For Sensors And Actuators

At Last, A Proposed Standard Allows Any Sensor Or Actuator To Be Interfaced With Systems And Networks, Independent Of The Network Used.

KANG B. LEE, National Institute of Standards and Technology (NIST), Bldg. 233, Room B102, Gaithersburg, MD 20899-0001; (301) 975-6604; *e-mail: kang.lee@nist.gov.*

LEE H. ECCLES and LARRY MALCHODI, Boeing Commercial Airplane Co., P.O. Box 3707, MS14-ME, Seattle, WA 98124-2207; (206) 655-2824; -5695.

The advent of microcontrollers and low-cost analog-to-digital converters (ADCs) has given rise to a new type of transducer, characterized by having a digital output in some form of computer-compatible format. Some have a built-in microcontroller that gives them the ability to provide built-in linearization and error correction. This allows inexpensive devices to provide greater accuracy previously unavailable. More importantly, they give the potential for much simpler wiring than is possible using older analog technology. This translates into lower installations costs. So, what does it take to obtain these lower costs?

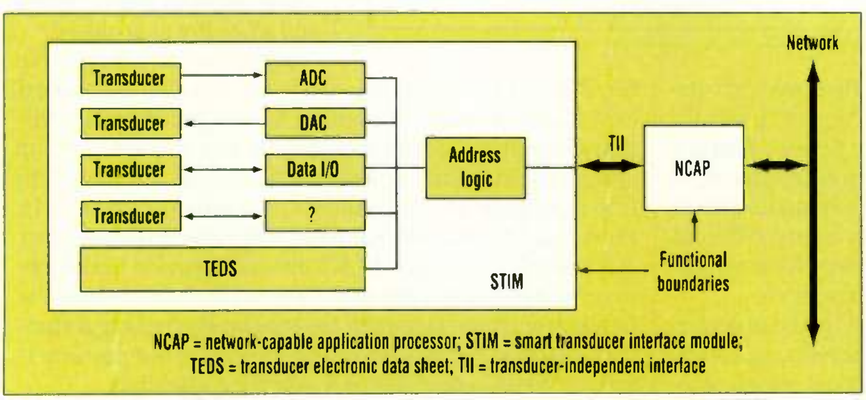
This is difficult to answer right now, because while there are smart sensors, there are few standard interfaces for them. A popular interface for smart transducers is RS-232. While many transducers support RS-232, they all use a different protocol. RS-232 is a point-to-point interface, so the wiring is almost as complex as the analog wiring, unless receive and repeat protocols are used to allow many transducers to be connected in series. An alternative is RS-485, which supports multidrop buses. Again, while the interface is standard, the protocols are not, so transducers from different manufacturers won't work together. Clearly what's missing is a standard interface.

This was the problem Boeing faced while developing and testing its new 777 Airplane *(see "Simplifying testing of Boeing's 777," p. 98)*. Various Fieldbus committees have been trying for years to solve this problem, but to no avail. The IEEE P1451 set of standards tries to solve at least part of the problem. IEEE P1451.2 defines an interface that transducer manufacturers can build to, independent of the network the transducer is being used in. Three different entities are defined within the standard: The smart transducer interface module (STIM) that contains the transducers; the network-capable application processor (NCAP), which is the interface to the larger network; and the transducer-independent interface (TII) that interfaces the STIM and the NCAP *(Fig. 1)*.

The TII, some characteristics of the STIM, and the method of communicating between the NCAP and STIM are all standardized by IEEE P1451.2. This allows the same smart transducer to be used on many networks by providing the appropriate NCAP.

A STIM may contain up to 255 transducers of seven different categories defined: Four different sensor types, an actuator, an event detector, and a general transducer. Sensors provide the ability to acquire data and can have different timing characteristics. An actuator takes data from the NCAP, converts it to the appropriate form, and makes it available to the outside world or uses it within the STIM. An event detector can be included to detect alarms or other discrete functions. A general transducer is any type of transducer whose timing does not match the standard.

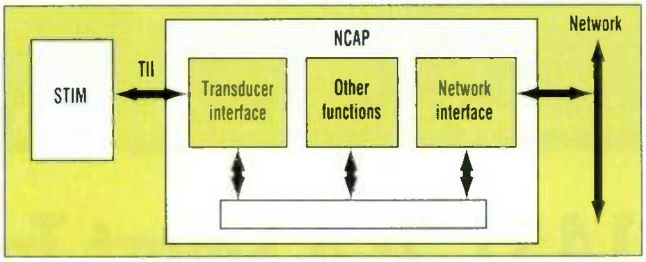
Eight different transducer elec-



1. The P1451.2 specification defines three entities: A smart transducer interface (STIM), a network-capable application processor (NCAP), and the transducer independent interface (TII).

tronic data sheets (TEDSs) are defined by the standard. They allow the system to identify the particular transducer that is installed. They also provide information about the timing required between the NCAP and the STIM. Some TEDSs apply to the complete STIM, and others to a single channel. Contained within the TEDS is information defining the physical units for the data being produced by a sensor or supplied to an actuator. Calibration constants for each transducer and a standard method of applying them are defined to further help companies to build NCAPs that will work with these transducers. The method of interconnecting the various devices within the STIM is outside the scope of the standard.

Within the NCAP, the network interface is a function of the network involved and is different for each network *(Fig. 2)*. Transducer interface hardware is defined by the standard that gives an object-oriented description of functions required by an NCAP.



2. As far as an NCAP is concerned, the network interface is a function of the network supported and is different for each network. The transducer interface hardware is defined by the P1451.2 standard.

One example of this type of function is the engineering-units conversion logic. It is assumed that most NCAPs will provide this function, but again, it is not required. Other functions that might be implemented in some NCAPs but not others would be things like Fourier Transforms. Since these "other functions" are only needed for special applications, general-purpose NCAPs probably will not include this capability. IEEE-P1451.1 provides the capability to add more functions, but how this is to be accomplished is up to

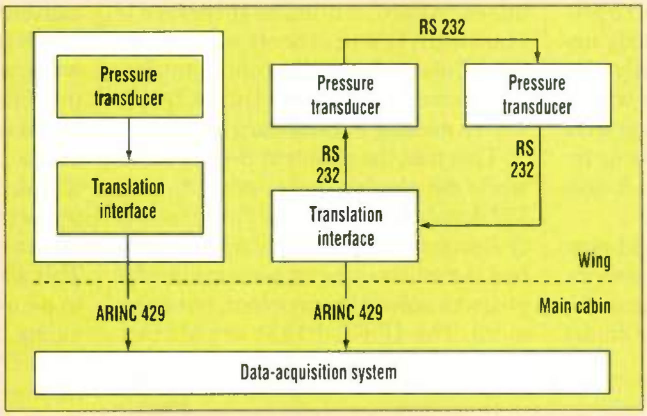
Simplifying Testing Of Boeing's 777

A major concern in an airplane-certification program is the size and amount of cables that go between the data-acquisition system in the airplane and transducers in the wings. Placing cables through the wings require modifying the airplane's structure. Modifications are expensive to plan, create, and repair after the test program. Because of the cost associated with these cables, Boeing's Flight Test Group has been vigorously researching methods to reduce and eliminate their number and complexity. We see the use of "smart sensors" as the best method to achieve those goals.

When Boeing's Flight Test organization selected transducers for use in testing the 777, we investigated several "smart sensors." They had the potential for many benefits, such as fewer cables, simpler wiring, and compensation for environmental effects. Because of the potential benefits, we used two different "smart" pressure sensors during the test program *(see the figure)*. A major drawback was that the sensors each used a different output format. Even if sensors from two different manufacturers produced the same electrical output, they used a different protocol, so a different interface was required for each sensor type. That is not only annoying, it is expensive.

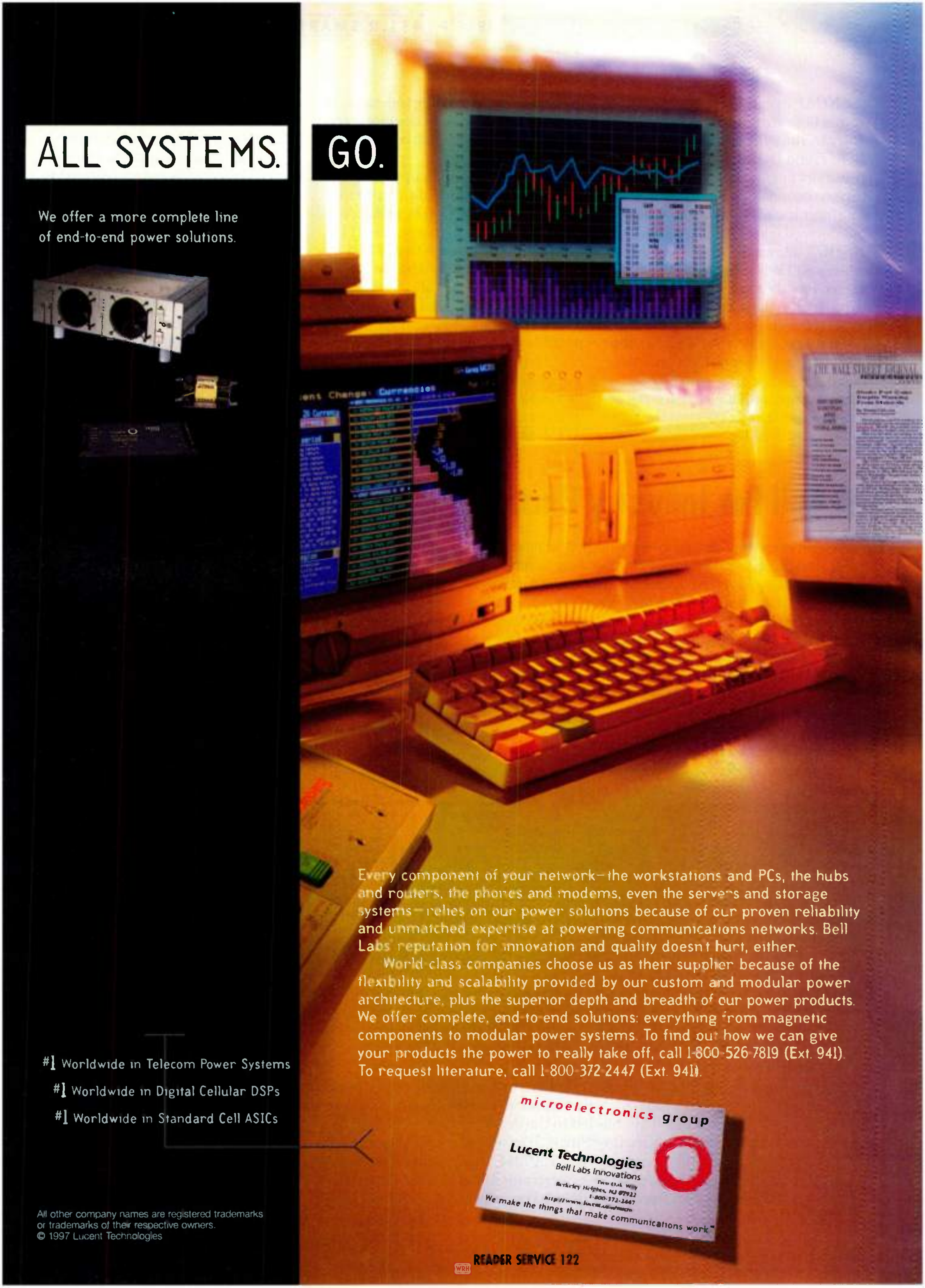
The first pressure sensor was modified by the manufacturer to output its data in an ARINC 429 format, a common avionics data bus format in which Boeing has considerable experience. The thought behind requiring this kind of output was that it was simple to interface into the data-acquisition system. This sensor did not achieve the goal of reducing the number of cables, but it did allow us to gain some experience with using smart sensors in the data system.

The other pressure sensor had an RS-232 output that allowed multiple sensors to be daisy-chained. This sensor system required manufacturing a unique interface that would control the sensors and convert the data into ARINC 429 format. Again, this format was chosen because it was easy to interface to the data-acquisition system. For the 777 test program, we connected four sensors to the interface box and cut the number of cables required. A side-effect of the translation interface was uncertainty in timing between when the data was sampled and when it was acquired.



After the test program for the 777 was complete, we decided to develop a standard that would eliminate the output format problem. In addition to eliminating the redesign that was required for our system each time a new sensor was selected, we wanted to find a simpler way to connect them into our system. In short, what we wanted was an appropriate "Fieldbus" that is standard. The IEEE-P1451 does not provide that; however, it does make a big step forward in defining how the fieldbus will interface with the sensor. By making a standard that transducer makers can use, half of our problem is solved. We can now proceed to selecting a fieldbus.

Lee Eccles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the NCAP manufacturer.

Ten lines are incorporated in the TII *(see the Table)*. The first three, DIN, DOUT, and DCLK, perform the data-transport function and use the SPI interface common on microcontrollers. The functions of the remaining lines are not derived from any other standard. NSDET allows the system to detect when a STIM is removed from or connected into the system without having to reinitialize the entire system.

NINT is the service request or interrupt line. The NCAP may use it to generate an interrupt for a processor, but still may not be able to respond to the interrupt until it completes the active process. This is because the same interface is used for reading and writing data as is for reading the status to determine the cause of the interrupt. The NCAP is expected to be slow in responding to interrupts.

The NCAP must supply to the STIM 75 mA at 5 V dc. Any more power must be supplied by using a secondary power connector on the STIM. The standard requires that STIM interface logic be powered by the NCAP so that the NCAP can always read status from the STIM if installed.

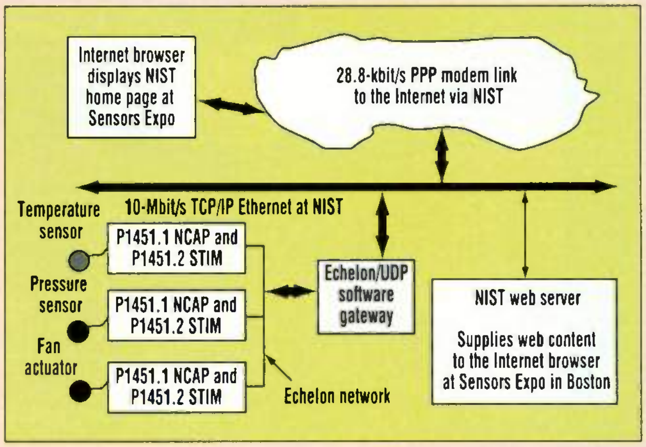
Many system configurations are possible with this standard. One concept that interfaces to popular networks like Ethernet, LonWorks, and DeviceNet appeals to transducer manufacturers *(Fig. 3)*. It shows that a STIM can be applied equally well with any NCAP. The STIM doesn't care how it communicates with the system. The NCAP isolates it from the network.

The calibration constants stored in the TEDS would be used to convert to physical units in each NCAP using the method described in IEEE P1451.2. The system would see the same data no matter which NCAP the STIM is plugged into. This is important to the user as well as transducer manufacturers since it allows the system designer to select a network based on system requirements and not what transducers are available for a given network.

The system designer can settle on which network or networks meet the system requirements, and then purchase a single type of NCAP for each

A Call For Industry Participation

Sensors are used in a wide range of applications from industrial automation to patient-condition monitoring in hospitals. With the advance of silicon and MEMS technologies, more "smarts" are integrated into sensors. The emergence of smart-sensor and control-network technologies has created new business opportunities as well as problems for sensor manufacturers and system integrators. Control networks provide many benefits for transducers (defined here as sensors or actuators). The advantages are a significant reduction of installation and maintenance cost by eliminating large numbers of analog wires, reduction of downtime, and improvement in overall system reliability. However, the proliferation of control networks results in many networks being available for designing distributed measurement and control systems. It becomes too costly for transducer manufacturers to support multiple network protocols. Besides, there's no standard interface between transducers and microprocessors to enable self-identification. The industry must thus standardize the interface between sensors and control networks.



Engineers and computer scientists at NIST are working with industry to develop a common communication interface for smart transducers. This has led to the development of two Draft Standards for the "Smart Transducer Interface for Sensors and Actuators," IEEE P1451. One draft, P1451.2, defines the Transducer Electronic Data Sheet (TEDS) and its data format, the Smart Transducer Interface Model (STIM), the digital interface, and a communication protocol. It enables the easy connection of transducers to network microprocessors. Another draft standard, P1451.1, defines a network-independent common object model for smart transducers and interface specification for model components in the Network Capable Application Processor (NCAP).

The benefits of these common interfaces are: 1. Allow users to select the transducer(s) best suited to solve the measurement or control problem independent of the control network. 2. The same transducer works on multiple control networks. 3. Allow self-identification of a transducer when it is connected to a network microprocessor, thus self-configuration can be achieved. 4. Simplify connectivity of smart transducers to control networks.

Since the proposal for developing smart-sensor interface standards was accepted by the Committee for Sensor Technology of IEEE's Instrumentation and Measurement Society in Sept. 1993, five workshops were held to address the interface issues, and two working groups were formed to develop the draft documents. One approach by committee members is to continuously demonstrate to the sensor community the concept and implementation of the smart transducer interface at conferences and workshops. A proof of concept for self-identification sensors was demonstrated at Sensors Expo in May '95 using LonWorks, SDS,

(continued on page 102)

network *(Fig. 4)*. Then, any STIM can be connected to any NCAP and function as it was designed. The figure shows a simple single-channel STIM measuring acceleration. The system will see a number expressed in m/s^2 and can then display the parameter in "g's" or any other appropriate units. If the STIM is replaced with one having an accelerometer with a different range, the system will display the data the same way without any other changes.

The next STIM is a little more complicated *(Fig. 4, again)*. It shows a pressure sensor with a temperature sensor attached to it. The NCAP can combine the output of both sensors by using the method described in IEEE P1451.2 to provide a temperature-compensated pressure output. The last STIM is a device that measures the pressure in a hydraulic ram and its position. It's programmed by the manufacturer to use this information in a feedback loop to control the hydraulic ram. It also contains a set of limit switches to generate alarms if the ram is driven too far. Any one of these devices could be plugged into the standard NCAP for that system.

Channel Groupings

It's anticipated that many STIMs will contain channels with some built-in relationship to each other. One manufacturer might build a three-axis accelerometer with Channel One being the x axis, Channel Two the y axis, and Channel Three the Z axis. Another might use Channels Seven, Two, and Four for the three axes. By creating a channel grouping and identifying which channel represents each axis, the system can determine this information without defining it in the standard.

A second use for channel groupings is to define the relationship between virtual actuators and the channels they control. For example, an event detector has three possible configurable parameters: The mode, which determines the edge or edges are reported; the threshold setting; and the hysteresis. The mode is simply two bits and can be controlled by a control command or

(continued from page 100)

and DeviceNet control networks.

The most recent demonstration was held at the Sensors Expo May 13-15, '97, Boston, Mass. NIST collaborated with a group of companies from industry including sensor, instrumentation, and electronic interface manufacturers, system integrators, and users to demonstrate the implementation of IEEE P1451.2. The purpose of the demonstrations was to show the capability of the common transducer interface between sensor and network that allows the "plug and play" of sensors to networks.

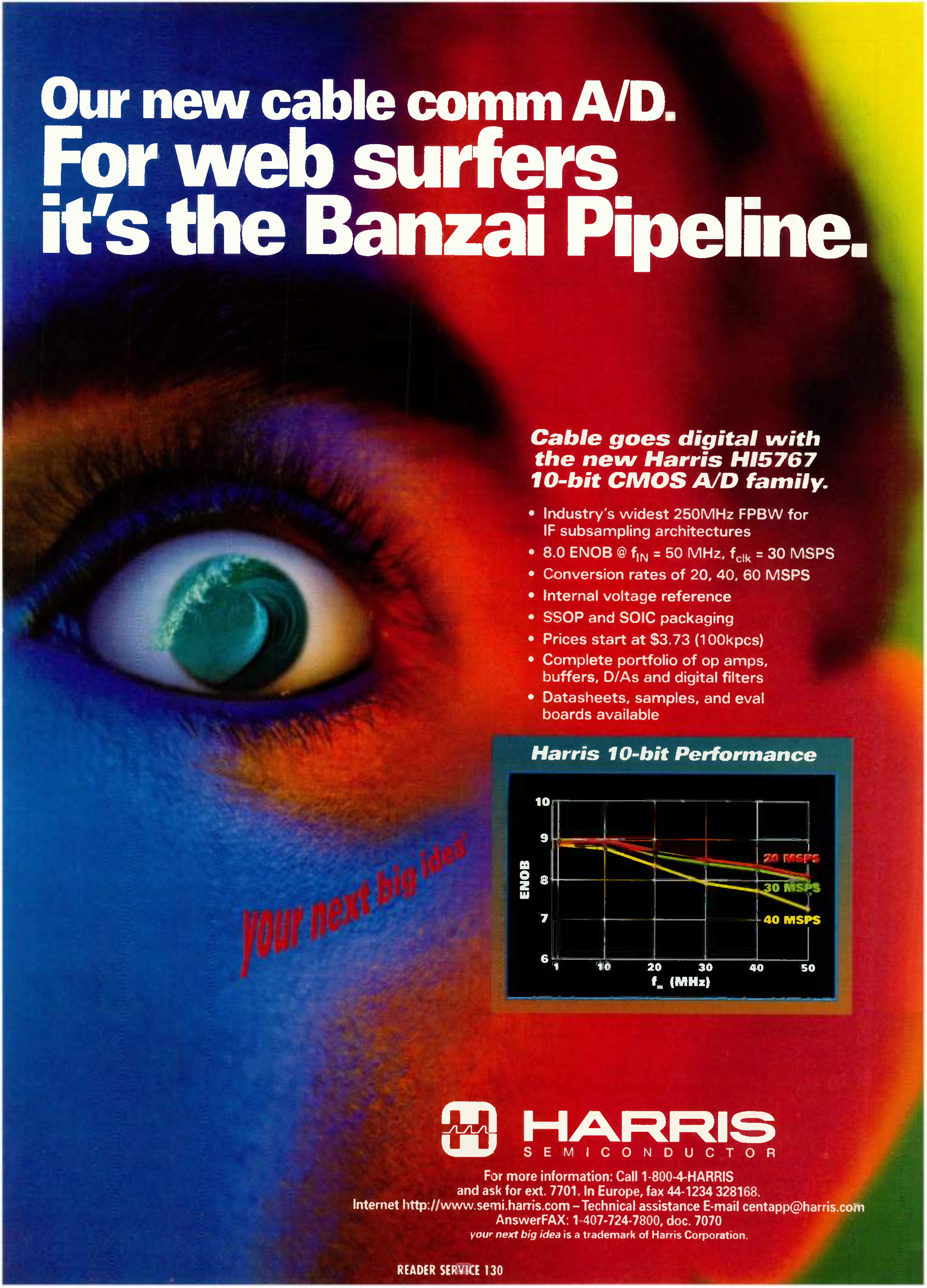
The demo consisted of the implementation of the interface in hardware and software (STIM as defined by P1451.2) and application systems that illustrate the features of the interface specification. The proposed standard is appropriate for a simple single-channel transducer or up to 255 input/output channels. An example application would be to make a correction on one channel dependent on another channel such as temperature. Another would be to derive a measured value such as mass flow from a combination of measured values. Analog Devices, Endevco, Optek Technologies, and Weir-Jones showed examples of a few channels on a STIM. Simple single-channel STIMs were demonstrated by both AB Networks and Electronic Development Corp. The proposed standard transducer interface provides device interchangeability, giving users more of a choice. Moore Products and Lucas NovaSensor showed how sensors, selected for cost, resolution, accuracy, and other reasons, can be easily interchanged.

The proposed standard supports the traditional paradigm of host-based applications. Application logic can reside in the STIM or NCAP, enabling the benefits of fully distributed applications. For example, Boeing showed a fully distributed measurement and control application on the Hewlett-Packard Vantera architecture that uses a publish/subscribe communication protocol. Strain gages mounted on the wings of a model airplane broadcast sensor data to the network through an Ethernet node. This information was used by software residing in another NCAP to control the actuators; in this case, the stepper motors.

The sensors and actuators were connected as nodes on the Ethernet, each of whose nodes had a built-in micro-Web server. Visitors could access manufacturers' information and data from the sensors using a Web browser via custom Web pages. In addition, the NIST staff demonstrated the remote access of P1451.2-compatible smart sensors through the Internet using the P1451.1 object model. The demo showed that sensors and actuators connected to a LonWorks control network set up in a lab at NIST can be accessed via the World Wide Web. The temperature sensor in the room was scanned and the cooling fan was remotely controlled by the visitors using Internet and Web-based technology through modem and commercial telephone service. Live audio/video is used to provide feedback for real-time confirmation of remote-command execution. The implication of this technology is so great that managers, engineers, or technicians can remotely read and check the condition of sensors and the status of control systems across the country or even around the globe. This opens up a whole new world for sensor and control applications.

The demonstration topology illustrated essentially allows remote control of IEEE P1451.2 nodes via the Internet *(see the figure)*. The actual transducers are connected to an Echelon control network located at the NIST facility in Gaithersburg, Md. An NIST-developed software gateway that maps the Echelon network to the P1451.1 object model is used to access the Echelon control network from the Internet. This attachment allows the demonstration to remotely access, control, and display specific IEEE P1451.2 sensor/actuator information using a standards-based Internet infrastructure.

It is important to implement the smart interface standard into as many application systems as possible such as factory automation, process control, building automation, machinery system monitoring, and automated measurement and control, etc. to evaluate the adequacy of the specifications. For those interested in participating as an evaluation site for the standard, or for further information, contact Kang Lee of the NIST at (301) 975-6604; e-mail: *kang.lee@nist.gov*.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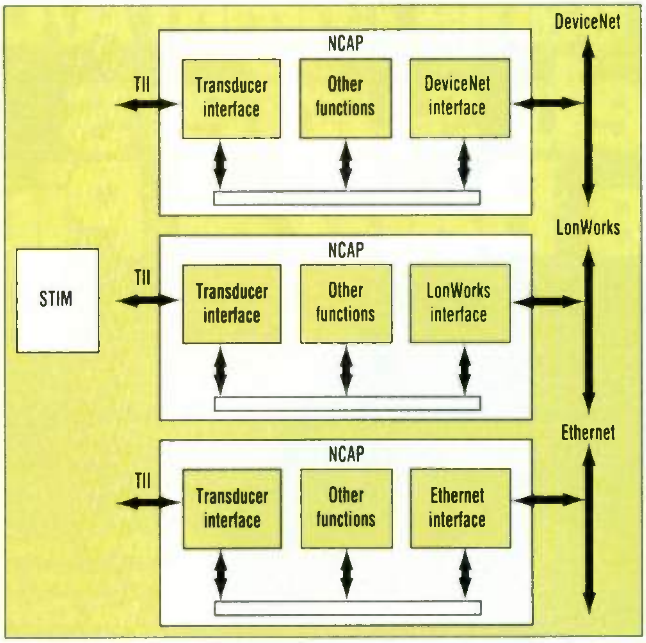
through the use of a virtual actuator. However, for threshold and hysteresis values, the is more complicated.

The end-user knows that the threshold should be set to some value in the physical world, but does not know exactly how it is represented in the STIM. By using a virtual actuator, which is a channel and may have a calibration TEDS, users can specify the threshold in physical units and the NCAP or STIM can convert that to the internal form and value required by the event detector. The general rule is that if the control channel could benefit from having a calibration, then channel groupings and virtual actuators should be used to control the channel. If an arbitrary pattern of bits is required (i.e., a gain setting), then the use of a control command is simpler.



3. From a transducer manufacturer point of view, this concept of interfacing transducers to networks is most appealing. That's because it supports popular networks like DeviceNet, LonWorks, and Ethernet.

Eight TEDS Memories

Eight different TEDS memories are defined in the standard; two are required and six are optional. In general, they are divided into two categories. In the first category, they contain data in a machine-readable format primarily intended to be used by the NCAP. The second category is for TEDS that contain data in a human-readable format. The two mandatory TEDS are in the machine-readable category: The meta-TEDS, and the channel TEDS. The calibration TEDS and the generic extension TEDS are both optional machine-readable TEDS. The human-readable TEDS are all optional—the meta-identification TEDS, the channel-identification TEDS, the calibration-identification TEDS, and the end-user application-specific TEDS. The human-readable TEDS blocks may be in more than one language with different encoding schemes.

The meta-TEDS contain the data that describes the entire STIM. The first entries contain the revision of the standard and the version number of the TEDS. It includes the number of channels in the STIM and the worst-case timing required to access these channels. This information allows the NCAP to access the channel information. Also included in the meta-TEDS are channel groupings that describe the relationships between channels.

A channel TEDS for each channel in the STIM gives the details on the particular channel. The meta-TEDS lists the worst-case timing for the entire STIM and the channel TEDS lists the actual timing parameters for the individual channel. It also lists the type of transducer, the format of the data word being output by the channel, the physical units, the upper and lower limits, the accuracy, whether or not a calibration is supplied, and where it is to be performed.

The calibration TEDS is optional. It contains information to allow sensor data to be converted from the raw format in which it is sensed into physical units called out in the channel TEDS. For actuators, it contains the constants to allow data in the physical units supplied by the system to be converted into the format needed by the actuator output. It also contains the last calibration date and time and the calibration interval. This allows the system to determine if the calibration is out-of-date. For calibration constants to be useful, the algorithm for applying them must be supplied.

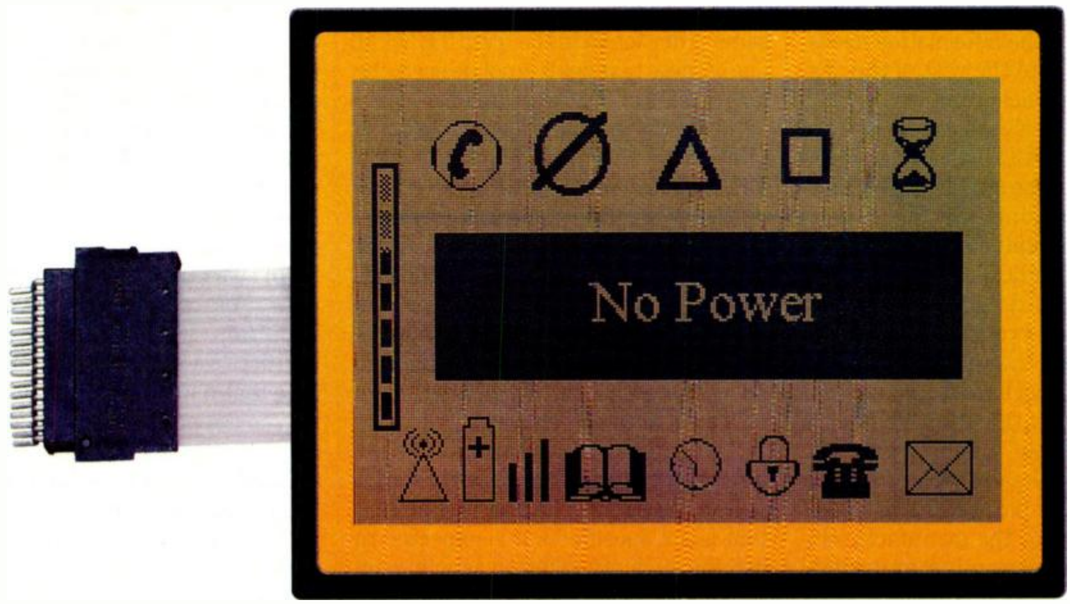
If a different algorithm is to be used in a clean fashion, a new calibration TEDS extension needs to be defined and included in the channel TEDS. The algorithm supplied in the standard allows other channels in the STIM to be used to correct the output of a different channel. Each channel being used can be segmented so that the calibration can be represented as an array of n-dimensional surfaces. This extremely powerful process will require most calibration labs to develop new processes and software to deal with it.

The generic extension TEDS is provided to allow industry groups to provide additional TEDS in a machine-readable format, something not anticipated by the working group. If such a TEDS is present, it's identified in the channel TEDS. The structure of

SIGNAL AND CONTROL LINES FOR THE TRANSDUCER-INDEPENDENT INTERFACE

Line	Driven by	Function
DIN	NCAP	Address and data transport from NCAP to STIM
DOUT	STIM	Data transport from STIM to NCAP
DCLK	NCAP	Positive-going edge latches data on both DIN and DOUT
NIOE	NCAP	Signals that the data transport is active and delimits data-transport framing
NTRIG	NCAP	Performs triggering function
NACK	STIM	Serves as both trigger and data-transport acknowledge
NINT	STIM	Used by the STIM to request service from the NCAP
NSDET	STIM	Grounded in the STIM and used by the NCAP to detect the presence of a STIM
POWER	NCAP	Nominal 5-V power supply
COMMON	NCAP	Signal common or ground

Get Unplugged from Old Display Ideas



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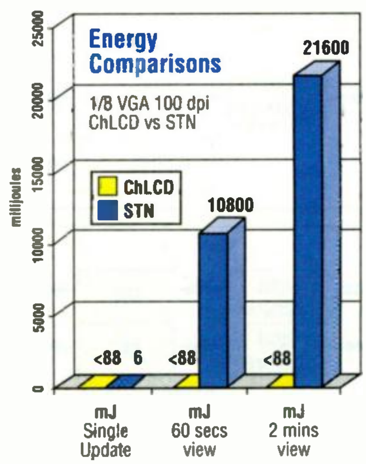

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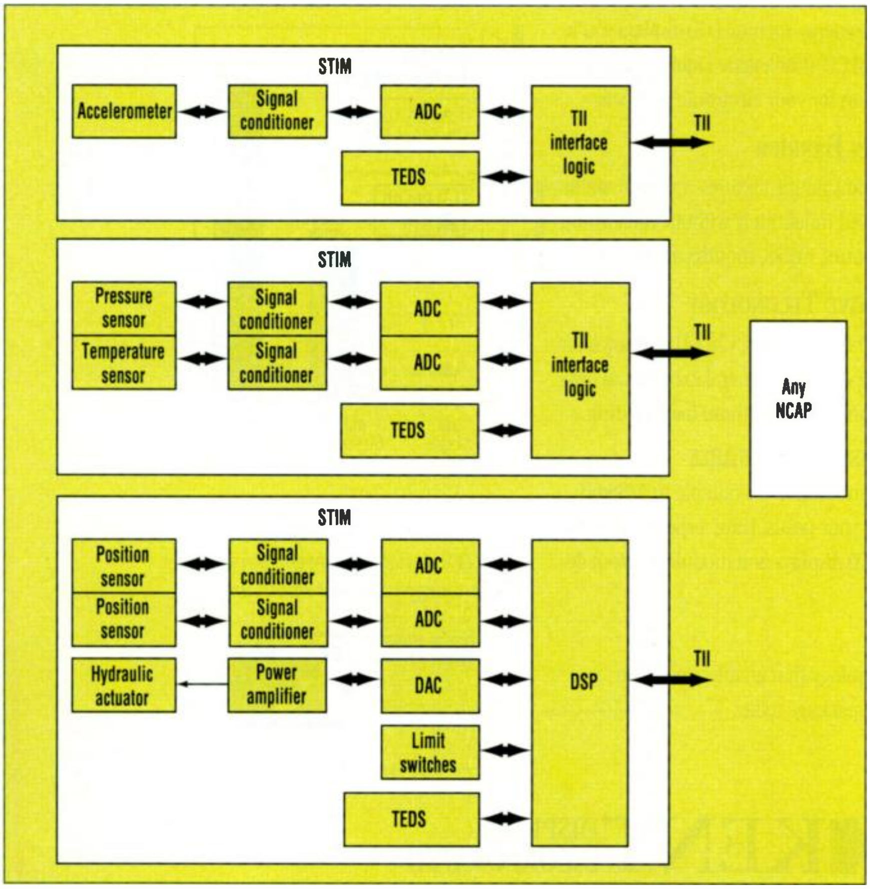
the TEDS is not defined in the standard except for the information necessary to link it into the rest of the system. The second field contains a TEDS identifier, which if zero, is a prototype generic extension TEDS not defined in an extension to the standard. No information on parsing this prototype TEDS can be obtained from the standard and a "standard" NCAP will not be able to use it. Additional information must be supplied to an NCAP that is capable of accepting it. This TEDS is expected to be machine-readable.

The meta-identification TEDS is a "human-readable" memory that the system may wish to retrieve from the STIM for display purposes. This TEDS contains fields for the manufacturer's name, the model number and serial number of the STIM and a date code. A length field is included for each text field. It also contains a field that may be used to include a description of the STIM similar to what would be found on a printed data sheet. The name of each channel grouping is included in this TEDS. These names must appear in the same order found in the meta TEDS. If one of these text fields is not desired, the length for that field is set to zero.

The channel-identification TEDS is similar to the meta-identification TEDS. It is most useful when transducers from other manufacturers are built into a STIM. The channel-identification TEDS allow the same information to be supplied for each channel as the meta-identification TEDS supplies for the STIM. Channel groupings are not included in this TEDS since they only exist at the STIM level.

The calibration-identification TEDS is provided as a place for calibration details in the STIM. The information content is not specified but is expected to include such information as who performed the calibration and what standards were used.

The end-user application-specific TEDS also is not detailed by the standard. The number of languages and the language code fields are defined but the contents are left up to the end-user.



4. From a user's perspective, this arrangement is most suitable for interfacing transducers to networks. It allows the system designer to settle on which network(s) to use that meet system requirements and to purchase a single type of NCAP for each network.

To specify physical units, the standard requires the use of seven SI units plus radians and steradians. A method of encoding the units into a series of 10 bytes is specified. By combining the nine units defined in the standard, almost any physical units can be specified. The encoding allows the specification of dimensionless quantities that is the ratio of two quantities having the same units. For example, strain is expressed in m/m. The log10(U) and the log10(U/U) also are included. Digital data that may represent such information as the position of each switch in a bank of switches is allowed. Units such as hardness, represented by an arbitrary scale, can be identified.

The biggest complaint is that "the units that I need are not in there." For example, a user may want to display degrees Fahrenheit, and the standard only allows degrees Kelvin. The intent of the standard is to provide a set of physical units that will allow the transducer to be calibrated the same way, regardless of the application or the part of the world in which it will be used. So, the standard describes a universal set of physical units and leaves it up to the system to convert it to the form that the user wants to see.

If this standard is accepted by industry, then any misunderstanding of what the transducer is producing for an output is eliminated *(see "A call for industry participation," p. XX)*. This removes chances for error between the transducer manufacturer, the calibration laboratory, the system software, and the user, and should result in more robust systems. However, it is true that you probably don't want to see "m^2kg/s^3A" when what you expect is "volts."

Kang Lee is leader of the NIST's Sensor Integration Group, and Chairman of the Technical Committee on Sensor Technology in the IEEE's Instrumentation and Measurement Society.

Lee Eccles designs test equipment for Boeing's Flight Test System Development Group.

Larry Malchodi is lead engineer at Boeing's Data Systems Equipment Design Group.

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MODERATELY	558
SLIGHTLY	559

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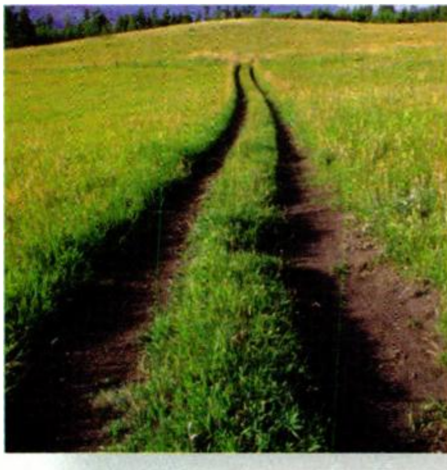

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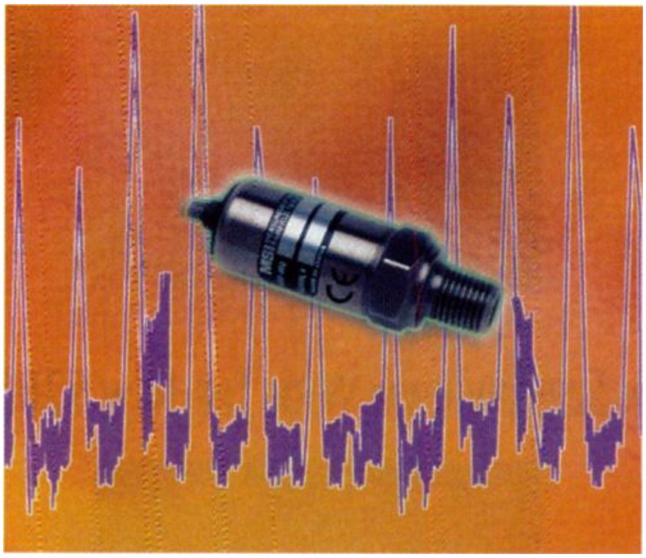
SENSOR TECHNOLOGY WATCH

CE Approval Means Understanding And Conforming To The EEC EMC Directive

Every piece of electronic equipment manufactured or imported into Europe must meet the European EMC Directive to obtain the "CE" mark of approval. This mandatory directive, effective as of Jan. 1996, sets the stage for reducing EMC susceptibility for safety or economic reasons for applications in automotive, aerospace, industrial, commercial, and consumer markets. This directive, 89/336/EEC, is widely regarded to be the most comprehensive, complex, and possibly contentious directive ever to emanate from the European Economic Community (EEC).



Measurement Specialties Inc.'s MSP-400 series of pressure transducers are designed to minimize EMI in hostile environments.

Electromagnetic interference (EMI) is a form of environmental pollution that can be generated from low-power digital circuits to high-power radio antennae. Different forms of EMI can cause electrical and electronic malfunctions in safety-critical control systems and ignite flammable or hazardous atmospheres. Reported examples of EMI are:

• Malfunctions of aircraft navigation equipment during use of cell phones.

• A particular make of car would stall on a stretch of highway near a high-power radio transmitter.

• Instrument panels of police cars fluctuate during radio communications.

• Malfunctions of gasoline and diesel pumps due to mobile phones.

Unique design practices must be adopted to provide immunity from EMI. Basically, a device, equipment, or system must function satisfactorily in an EMI environment without significant errors. EMC can be problematic in situations where several electronic systems or equipment are packed in a compact installation and located close to powerful EMI emitters in applications such as aircraft, ships, and surface transportation. The system integrator or manufacturer must have detailed knowledge of the installation and the surrounding environment to reduce EMI susceptibility. The EMC directive has two distinct operational modes:

• The ability of an electronic system to operate as intended without generating EMI which could interfere with other systems.

• The ability of a system to operate within specifications in an environment where EMI is present.

The essential requirements of the EMC directive are that the electronic equipment or systems shall be constructed to meet the following:

• The generation of EMI does not exceed a level allowing surrounding equipment to operate as intended.

• An adequate level of intrinsic immunity to electromagnetic pollution so that it can operate as intended.

Once the manufacturer meets this criteria, he/she can issue a declaration of conformity that must be kept available to the enforcement authority for 10 years once the product is placed on the market. The CE mark should be affixed to the product or to its package. Misuse of the CE mark in the form of nonconformity will result in heavy fines and eventual withdrawal of the product from the market.

The European Organization for Electrotechnical Standardization (CENELEC) has generated a set of generic standards to deal with the industrial sector. The standards cover low- and high-voltage apparatus.

For low-voltage apparatus, the emissions standard, EN 50081, has two parts *(Table 1)*. Part 1 covers the domestic, commercial, and light-industrial environment, while Part 2 deals with the industrial environment. For general immunity, standard EN50082 is used *(Table 2)*. EN 50082 Part 1 deals with domestic, commercial, and light-industrial environments, while Part 2 deals with industrial environments. Let's review the major requirements for each of the standards for Part 1 and 2.

Performance Criteria

The EMC directive has three criteria. Criterion A specifies that the apparatus shall continue to operate as intended with no degradation of performance below the manufacturer's specifications. There may be some cases where the performance level may be replaced by a permissible loss of performance. The product specifications shall contain this vital information. Criterion B specifies that the apparatus shall continue to perform as intended with no degradation in performance. However during testing, degradation in performance is allowed. No loss or change of stored data or operating state is allowed. The manufacturer must specify boundaries of degradation. Criterion C specifies that temporary loss of function is allowed during testing provided that the loss of function is self-recoverable.

Measurement Specialties Inc. (MSI) had first-hand knowledge in obtaining

TABLE 1: EN50081 TESTS

Part 1	Part 2
Radiated emissions from 300 to 1000 MHz for equipment operating above 9 kHz	Radiated emissions from 300 to 1000 MHz for equipment operating from 150 kHz to 1 GHz with relaxed limits below 30 MHz
Conducted emissions from 150 kHz to 30 MHz	Conducted emissions from 150 kHz to 30 MHz

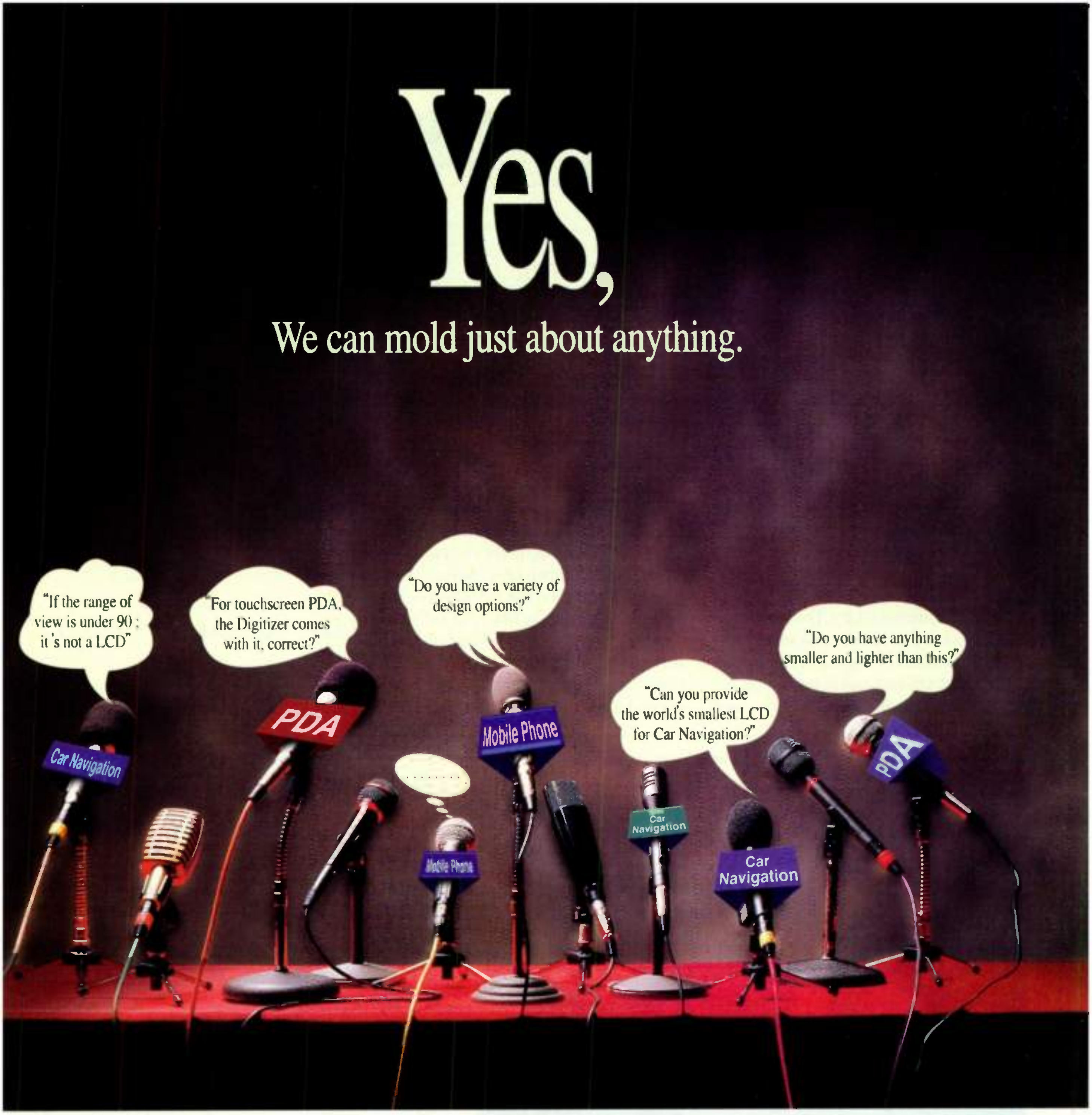


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TABLE 2: EN50082 TESTS

Part 1	Part 2
ESD of 8 kV, air-discharged to enclosure	ESD of 8 kV, air-discharged to enclosure, 4-kV contact discharged
Electrical fast transients, 5/50 ns, 0.5/1 kV applied to all power and I/O lines	EFT, 5/50 ns, 2 kV, 5 kHz applied to all power and I/O lines
Magnetic field, 50 Hz @ 3 A/m	Magnetic field, 50 Hz @ 30 A/m
Conducted immunity on all I/O and power lines, 0.15 to 100 MHz at 3 V	Conducted immunity on all I/O and power lines, 0.15 to 100 MHz at 10 V

CE approval while designing its MSP-400 series of pressure transducers. To meet the EMC directive and EN50082 Part 2 requirements, the product was specifically designed to handle hostile EMI environments in industrial, off-road, and surface-transportation applications. The electronics and the layout of the pc board were carefully designed to minimize the electrical interference in like electrostatic discharge (ESD), electrical fast transients (EFTs) and conducted susceptibility. Transient suppressors are used across the supply and output lines to clamp electrical transients that are fast and repetitive in nature. These transients can be anywhere from 50 to several thousand volts. Without EFT protection, the sensitive electronic elements will cease to function in applications such as compressors, pumps, motors, switching contactors, and the transducer will fail.

The package's design minimizes EMI in hostile environments *(see the figure)*. Feedthrough capacitors mounted on a plate and electrically connected to all input and output lines provide immunity against conducted electrical interference. Mechancially stacked into the housing, the plate provides a low-impedance path for unwanted RF currents. Use of an all-metal Faraday cage housing and shielded cable minimize magnetic and ESD interference.

As a result, the product is well-suited to hostile environments such as industrial hydraulics, refrigeration, fertilizer sprayers, train-braking systems, water boosters, heavy cranes and lifting equipment, compressors, and pumps. CE certification also means suitability for OEMs and system integrators who are importers and manufacturers of electronic equipment in Europe and Asia.

Contributed by Karmjit S. Sidhu, chief transducer engineer at Measurement Specialties Inc., Fairfield, N.J., where he is responsible for the design, sales, marketing, and applications for the industrial MSP series pressure transducers. He holds a masters degree in Industrial Measurement Systems from Brunel University, U.K. He can be reached at (201) 808-1819.

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Circle 520

Optically Isolated Input, Single-Supply True-RMS Converter

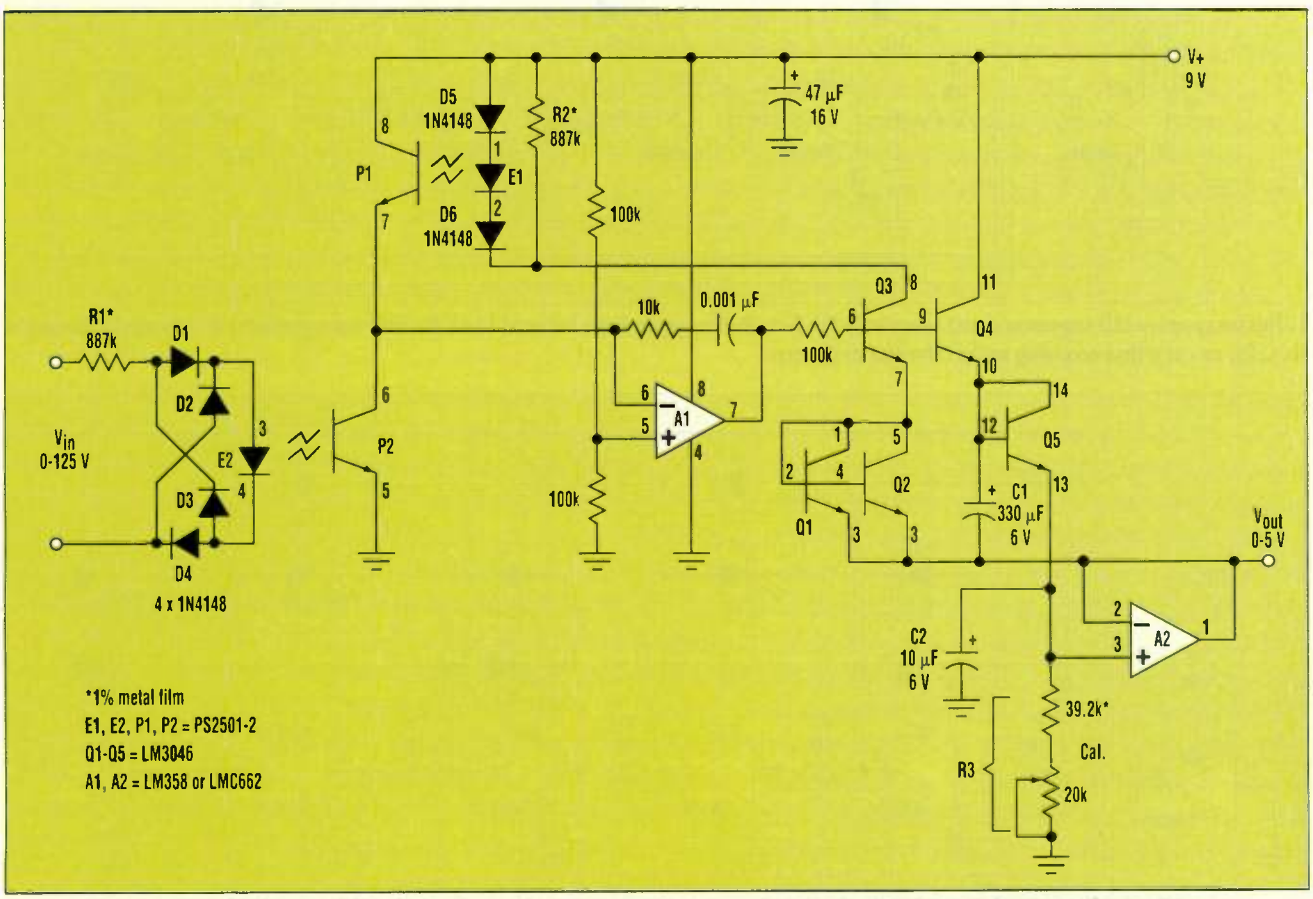
W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina,
Chapel Hill, NC 27599-3290; (919) 966-1358; woodward@net.chem.unc.edu.

With high-performance monolithic rms converters available, why would anyone *design* one? Simple: No commercially available IC, running from a single power rail, can accurately convert signals with a dc component. Nor can any IC accommodate signals that must be galvanically isolated from ground. The rms converter described does both.

The trick that makes this possible is an optically isolated rectifier input circuit *(see the figure)*. Input voltage V_{in}, applied to full-wave bridge D1-D4 and LED E2, produces LED current $I_{e2} = (abs(V_{in}) - V_d)/R1 = abs(V_{in})/R1 - V_d/R1$, where V_d = the sum of diode and LED voltage drops. The coupled gain of the E2:P2 optical pair results in photocurrent I_{p2}. To balance I_{p2}, A1 modulates Q3's collector current I_{q3}, thereby I_{e1} and the E1:P1 optical pair to force $I_{p1} = I_{p2}$. Due to the channel tracking that exists in a multichannel opto like the PS2501-2, when $I_{p2} = I_{p1}$, we can approximate $I_{e2} = I_{e1}$. LED and rectifier diode voltages will also match well, so $I_{e1} = I_{q3} - V_d/R1$. Thus, $I_{q3} = I_{e2} + V_d/R1 = abs(V_{in})/R1$, making I_{q3} an accurate measure of V_{in} that's (almost) independent of diode voltage drops! Admittedly, this compensation only works for $V_{in} >> V_d$, but that's good enough to maintain 1% linearity for input voltages as low as 10 V rms.

With $I_{q3} = abs(V_{in}/R1)$, there remains the matter of rms conversion of I_{q3}. This computation is based on the log relationship between V_{be} and collector current in Q1-Q5; the equality of this relationship among the five transistors in the LM3046 monolithic array; and the approximation that, for high beta transistors, $I_c = I_e$. Therefore, at any given temperature, there exist constants A and B such that $V_{be3} = A^*\log(I_{q3}) + B$ and $V_{be1} = V_{be2} = A^*\log(I_{q3}/2) + B$.

Thus, $(V_{be3} + V_{be1}) = A[\log(I_{q3}) + \log(I_{q3})/2] + 2B$. Since adding logarithms is equivalent to multiplication, $(V_{be3} + V_{be1}) = A^*\log(I_{q3}{}^2/2) + 2B$. Due to the topology of the circuit and the action of unity-gain buffer A2, $(V_{b3} + V_{b1}) = (V_{be4} + V_{be5})$. Then $A^*\log(I_{q3}{}^2/2) + 2B = A^*\log(I_{q4}{}^*I_{q5}) + 2B$. Cancelling A's and B's and taking antilogs: $I_{q3}{}^2/2 = I_{q4} * I_{q5}$. Capacitor C2 makes I_{q5} = the time average of I_{q4} and therefore $I_{q4} * avg(I_{q4}) = I_{q3}{}^2/2$. Averaging both sides gives $avg(I_{q4} * avg(I_{q4})) = avg\ (I_{q3}{}^2/2)$, and thus $avg(I_{q4})^2 = avg(I_{q3}{}^2/2)$. Taking square roots of both sides yields:



An optically isolated rectifier input, combined with the matched characteristics of a multichannel optoisolator, makes it possible for this rms converter to convert signals with a dc component as well as accommodate signals that are galvanically isolated from system ground.

avg(I_{q4}) = root(avg($I_{q3}^2/2$)). Equivalently, I_{q5} = RMS(I_{q3})/sqr(2). Finally, because I_{q3} = abs(V_{in})/R1 and V_{out} = I_{q5} *R3, we have at last: V_{out} = (R3/R1) * RMS(V_{in})/sqr(2).

The prototype, with V+ = 9 V and R3/R1 scaled for a full-scale V_{in} of 125 V and output of 5 V, demonstrated better than 1% accuracy for V_{in} > 10 V and input frequencies up to 10 kHz. The circuit works accurately with supply voltages from 5 V to 15 V, but due to the way the voltage drops of D5, D6, E1, Q1, Q2, Q3, and R3 add up, $V_{out(max)}$ is approximately (V^+ – 4 V). So, V^+ = 9 V is the minimum, consistent with a 5-V full-scale V_{out}. Current demand is modest at less than 2 mA.

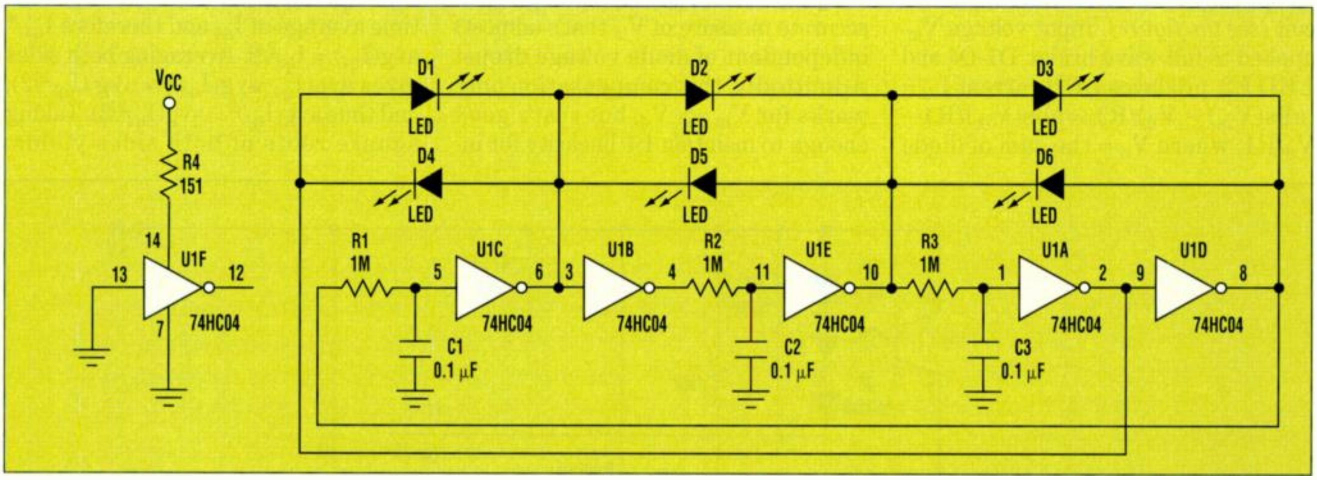
Circle 521

Low-Cost LED Sequencer

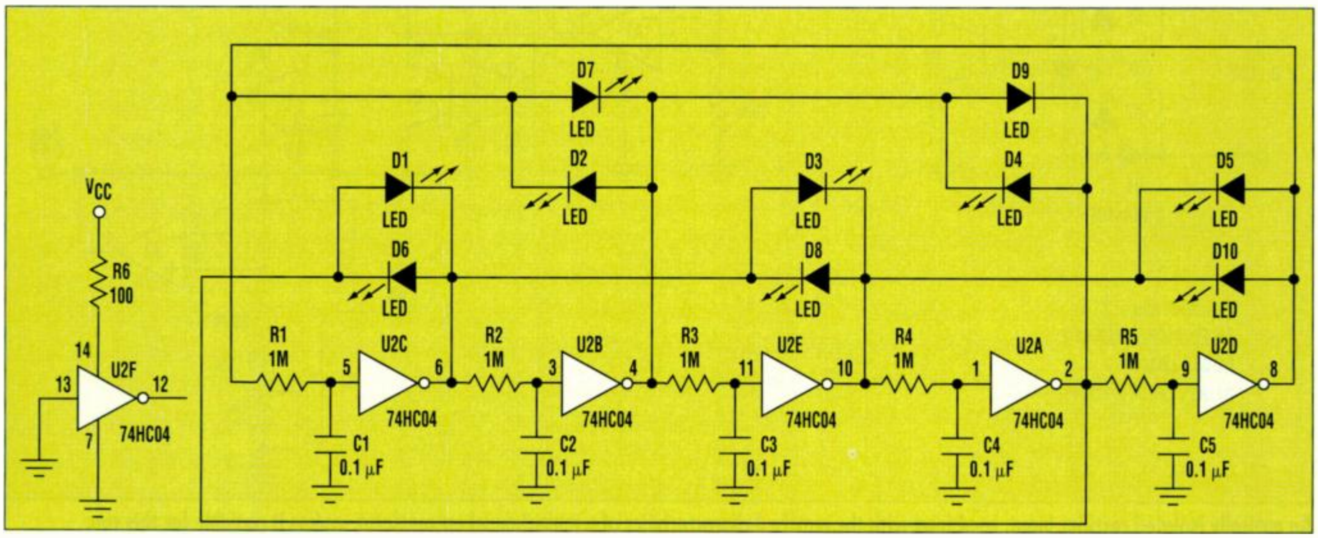
WILLIAM J. HUDSON
4127 McLaughlin #10, Los Angeles, CA 90066.

Cost is always an important consideration in circuit design, but even a couple of pennies often makes a critical difference in electronic toy designs. The circuits presented here for blinking LEDs are based on the 74HC04, one of the most common and least expensive chips available. Its six inverters can easily drive LEDs, and it operates over a wide voltage range, which is ideal for battery-operated circuits.

An odd number of inverters chained together in a loop is an inherently unstable circuit . Two adjacent gates will always have the same output, so the inverters constantly change state in sequence. LEDs, connected between every other output, light only when the gate between the outputs is switching. Resistors with capacitors slow and control the rate



1. This inexpensive LED sequencer circuit operates in the 2- to 9-V range, cycling at around 1 to 2 Hz. This arrangement will sequentially illuminate six LEDs, one at a time according to the reference designator.



2. This expanded version of the Fig. 1 circuit cycles through 10 LEDs with two LEDs illuminated at a time.

at which the LEDs blink. A single resistor to V_{CC} limits current for all of the LEDs, and the voltage drop across this resistor extends the voltage range of the circuit.

The two circuits shown operate from about 2 to 9 V, and cycle at around 1 to 2 Hz. The first circuit lights six LEDs, one at a time, in the order indicated by the number in the reference designator *(Fig. 1)*. The second circuit cycles through 10 LEDs *(Fig. 2)*. Two are lit at a time, with one LED turning off as the next is turning on. Simple variations of these circuit also can cycle through odd numbers of LEDs. Inverters can be fun building blocks.

Circle 522

PC's Printer Port Controls A Frequency Synthesizer

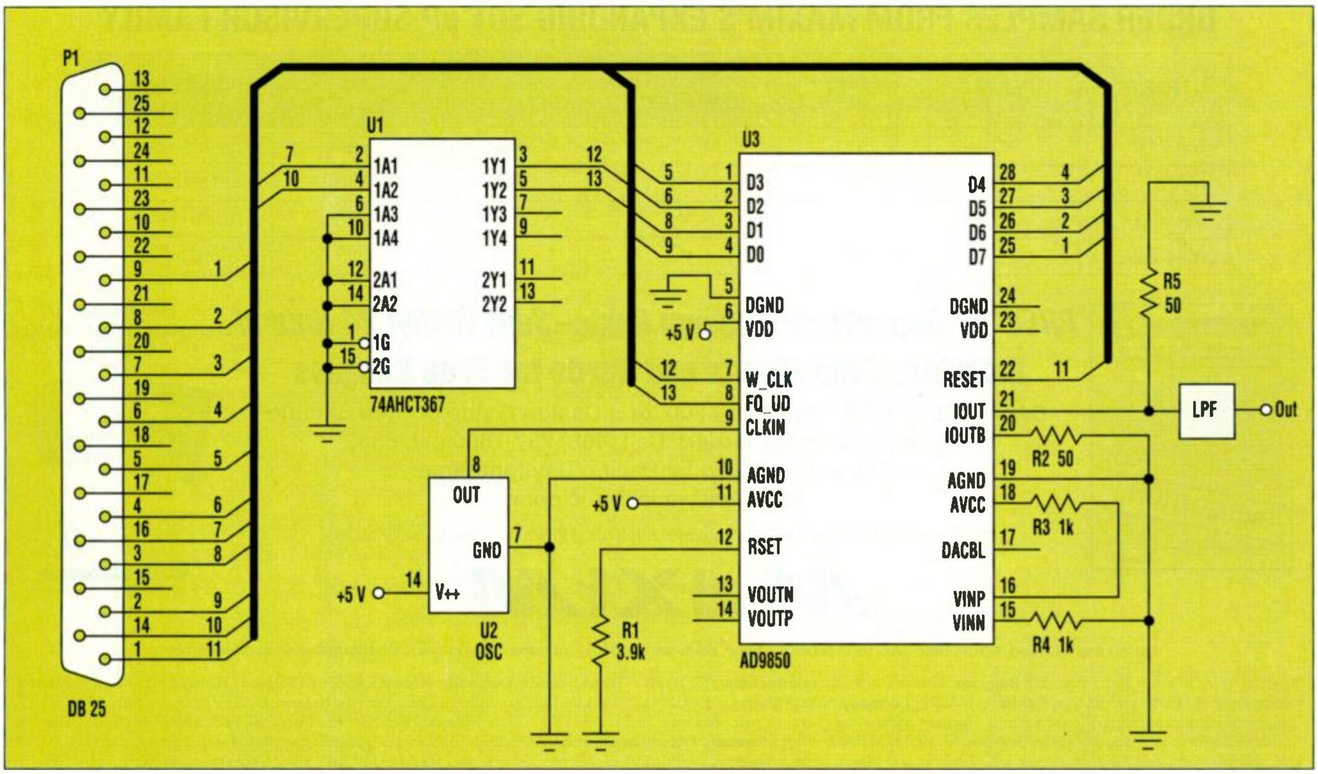
SAMUEL KEREM
Infrared Fiber Systems, 2301-A Broadbirch Dr., Silver Spring, MD 20904; (301) 622-7134; fax (301) 622-7135; e-mail: samuelkerem@juno.com.

The idea presented here offers a way to create a simple, yet versatile and stable, frequency synthesizer (sine and square wave). At the heart of the circuit lies an AD9850 DDS chip *(see the figure)*. The synthesizer is controlled through a PC's printer port (in most cases, the port's address is 0x378).

The program is interactive. You will be asked to enter values for the lowest and highest frequency, number of points (up to 30,000), and the delay in 1-ms increments between the points. The synthesizer provides continuous scanning—"jumping" from point to point from lowest to highest frequency until any key is pressed. Pressing "n" will result in a return to DOS; any other key will prompt you to enter new parameters.

For a single frequency generator, just enter the same lowest and highest frequencies. Pressing "LEFT ARROW" or "RIGHT ARROW" will decrease or increase the frequency by a value equal to 1/step (fine tuning). Pressing "DOWN ARROW" or "UP ARROW" will decrease or increase the frequency by a value equal to 10/step (coarse tuning). These four keys can be used in any order during the scanning process as well. In that case, the synthesizer becomes a generator with a single frequency. Repeated key pressing will allow you to "walk back and forth" within the region of interest. The current value of the output frequency will be displayed after every change.

Resolution of the frequency setting is 1 Hz (it can be as low as 0.03 Hz). The frequency range is from 1 Hz to 50 MHz (with a 125-MHz clock). Stability is achieved by using a quartz clock. "Hopping" time from one point to another is on a microsecond level. The best performance will be obtained with frequencies less than 1/3 of the clock's frequency. Theoretically, though, up to 1/2 is allowable (the user is responsible for obeying the Nyquist theory). A C++ program listing is provided.



This simple frequency synthesizer (sine and square wave) is both versatile and stable and is controlled through the PC printer port.

```
// "PC's Printer Port Controls A Frequency Synthesizer."
// Author:   Samuel Kerem
#include <iostream.h>
#include <dos.h>
#include <conio.h>
#include <stdio.h>

const PRN_DATA = 0x378;
const PRN_CNTR = 0x37A;
const RST_1 = 0x00;  const FQ_UD_1 = 0x00; const W_CLK_1 = 0x04;
const RST_0 = 0x01;  const FQ_UD_0 = 0x02; const W_CLK_0 = 0x00;

main()
{
const float CLOCK = 42.95;   // 2^32/9850 resolution)/10^8 (clock frequency)
                               // for another clock calculate correct ratio
unsigned long st, end, fr;
int del, step;
void syn(unsigned long fr);
char ch='a';
  while(ch != 'n') {
    switch (ch) {
         case 'M': st = end = fr = fr + fr/step;              //right arrow
                   printf("Now frequency is: %8.0f\n",st/CLOCK);
                   break;
         case 'K': st = end = fr = fr - fr/step;              //left arrow
                   printf("Now frequency is: %8.0f\n",st/CLOCK);
                   break;
         case 'P': st = end = fr = fr - 10*(fr/step);         //down arrow
                   printf("Now frequency is: %8.0f\n",st/CLOCK);
                   break;
         case 'H': st = end = fr = fr + 10*(fr/step);         //up arrow
                   printf("Now frequency is: %8.0f\n",st/CLOCK);
                   break;
         default:
             cout << "Enter frequency to start: "; cin >> st;  st *= CLOCK;
             cout << "Enter frequency to end:   "; cin >> end; end *= CLOCK;
             cout << "Delay, please:            "; cin >> del;
             cout << "Number of steps:          "; cin >> step;
             cout << "Scanning, hit \"n\" to stop. any key to change
             parameters" << endl;
    }

    outportb(PRN_CNTR, RST_1 + W_CLK_0 + FQ_UD_0); // reset
    outportb(PRN_CNTR, RST_0 + W_CLK_0 + FQ_UD_0);

    fr = st;
    while(kbhit()==0) {
      syn(fr);
      fr +=(end-st)/step;
      if(fr > end) fr=st;
      delay(del);
    }
    ch=getch();
    if(ch==0) ch=getch();  //if ch is not ASCII--arrows
  }
  return(0);
}
void syn(unsigned long freq){
   int  byte_1, byte_2, byte_3, byte_4;
   byte_1 = freq/0xffffff;        byte_2 = (freq%0xffffff)/0xffff;
   byte_3 = (freq%0xffff)/0xff; byte_4 = (freq%0xff);
   outportb(PRN_CNTR, RST_0 + W_CLK_0 + FQ_UD_0); // preliminary conditions
   outportb(PRN_DATA, 0x00);                       // control word
   outportb(PRN_CNTR, FQ_UD_1 + W_CLK_0 + RST_0);
   outportb(PRN_CNTR, FQ_UD_1 + W_CLK_1 + RST_0);
   outportb(PRN_CNTR, FQ_UD_0 + W_CLK_0 + RST_0);
            // first byte loading
   outportb(PRN_DATA, byte_1);
   outportb(PRN_CNTR, FQ_UD_0 + W_CLK_1 + RST_0);
   outportb(PRN_CNTR, FQ_UD_0 + W_CLK_0 + RST_0);
            // second byte
   outportb(PRN_DATA, byte_2);
   outportb(PRN_CNTR, FQ_UD_0 + W_CLK_1 + RST_0);
   outportb(PRN_CNTR, FQ_UD_0 + W_CLK_0 + RST_0);
            // third byte
   outportb(PRN_DATA, byte_3);
   outportb(PRN_CNTR, FQ_UD_0 + W_CLK_1 + RST_0);
   outportb(PRN_CNTR, FQ_UD_0 + W_CLK_0 + RST_0);
             // forth byte
   outportb(PRN_DATA, byte_4);
   outportb(PRN_CNTR, FQ_UD_0 + W_CLK_1 + RST_0);
   outportb(PRN_CNTR, FQ_UD_0 + W_CLK_0 + RST_0);

   outportb(PRN_CNTR, FQ_UD_1 + W_CLK_0 + RST_0); //freq - out
}
```

Circle 145 - For U.S Response
Circle 146 - For International

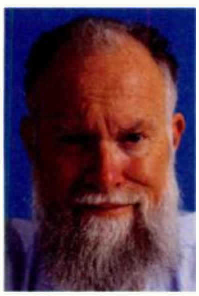
BOB PEASE

What's All This International Business Travel Stuff, Anyhow?

Well, a long time ago, I didn't travel much on business. But that was back in '65. Then, Philbrick sent me to California. I rented a '65 Ford (a much bigger boat than I ever drove before) and went to call on some customers—etc., etc. I survived. I enjoyed it. Then in '69, I went to Japan for a couple of weeks. In '70, I went to England and France, then Germany and Canada.

I survived. I enjoyed the travel—in addition to enjoying talking with some VERY interesting customers (or prospective customers) in interesting countries. But I sure was surprised when the German attendees began to KNOCK on their desks! (That's a sign of approval.)

Recently, I have been doing some more travelling, to as many as 10 cities, to places such as Seattle, Dallas, Chicago, Rochester, and Boston. So far, this has been a lot of fun. I've met a lot of nice people, and friends that had GOOD TOUGH questions for me. I may even be able to set up lectures in other U.S. cities to meet other good friends in the East and South.



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

But I have learned several *caveats* in international business travel. Always keep track of your reservation numbers so nobody can tell you, "You don't have any reservations." And, beware: If you are going to call on a customer who just might happen to be really *unhappy* with your company, because of some technical or business or delivery problem, then make sure you ask your local sales guys to brief you on questions and problems and potential unhappinesses well before you get there. I have learned to take the local country's airline when I go there. Then if the flight is late, the local guys start apologizing to me. (Whereas if I take UA or NW, and the flight is late, for whatever reason, even headwinds, I have to apologize to them.)

I recently read a book written by a guy on his many years of international business travels. Just a slim book, but well worth the price, and good reading. I recall that he was fascinated by the way that turning off one water faucet in a lavatory caused several other faucets to start to flow! A first-class puzzle! I tried to find the book last night by delving down through the top 4 feet of my in-basket, but I couldn't find the book. When he reminds me that I neglected his book, I'll tell you how to buy it.

I will probably be in Brazil as you read this. If your mail queue is very high or long, and you don't get around to reading this until November, I may be stuck in Brazil for *months*. But I'm a big boy, and an experienced traveller. I can live with that. I might even like to spend some cruzeiros there. Hey, Mr. Feynman learned to like Brazil. Now, I gotta give a lecture at WESCON in November (just a couple days before I leave for Nepal) on "International Business Travel for Engineers."

If you have any comments or anecdotes or stories or ideas about such international business travel—amazing things you have learned—or similar—I'd love to hear them before November. Horror stories? Insights? Incites? Send me a letter—or an e-mail.

Lemme tell you an idea I cooked up recently. First, let me mention that I have given my lecture with 402 slides in 3 hours, in 8 or 10 cities. I was even invited to give a private lecture to a big corporation where 110 guys showed up. But they could only allot me 90 minutes. So I chopped out some of the foils, and gave a basic lecture (with special foils added, to heckle them) in about 95 minutes. How did I do it ? Easy—I talked fast. And I asked 'em all to save most of their questions for the end, so they did not count in the 90 minutes. That was probably about 320 foils in 95 minutes. Most people use about 50 or 80 foils for that long of a lecture. Not me. Of course, if you have seen my lecture, you'll know that I have a lot of throw-away foils....

When I go to Brazil, I cannot rush through 400 or 300 foils in 3 hours. If I can do 200, speaking V E R Y S L O W L Y, it will be a miracle. So how do I get my story across?

I got this idea: Subtitles. If a guy knows English pretty well, but his native language is Portuguese, I should show him Portuguese SUBTITLES—just like they do at the opera, when they want to enlighten us—so he will get a quick idea of what I am talking about. NOT just a translation of what the slide says, but an INTERPRETATION of the key words of what I am going to be talking about. Of course I may have to carry 220 foils for me, plus 220 foils for the Spanish audience in Venezuela—plus 220 for the Portuguese audience in Brazil. But I'm a big boy. I'm sure I can carry that in my briefcase.

I'll let you know how this works out with the SUBTITLES. I'll probably write a column after November on the "International Travel" stories. Will I ever run out of good material for a column? Well ....it might depend on the interpretation of "good." I might even be able to give a lecture in Kathmandu after I go hiking in Nepal in November. I could use 220 SUBTITLE foils in Nepali. Show Me Where It Says I Can't Do It!

Namaste.

All for now. / Comments invited!
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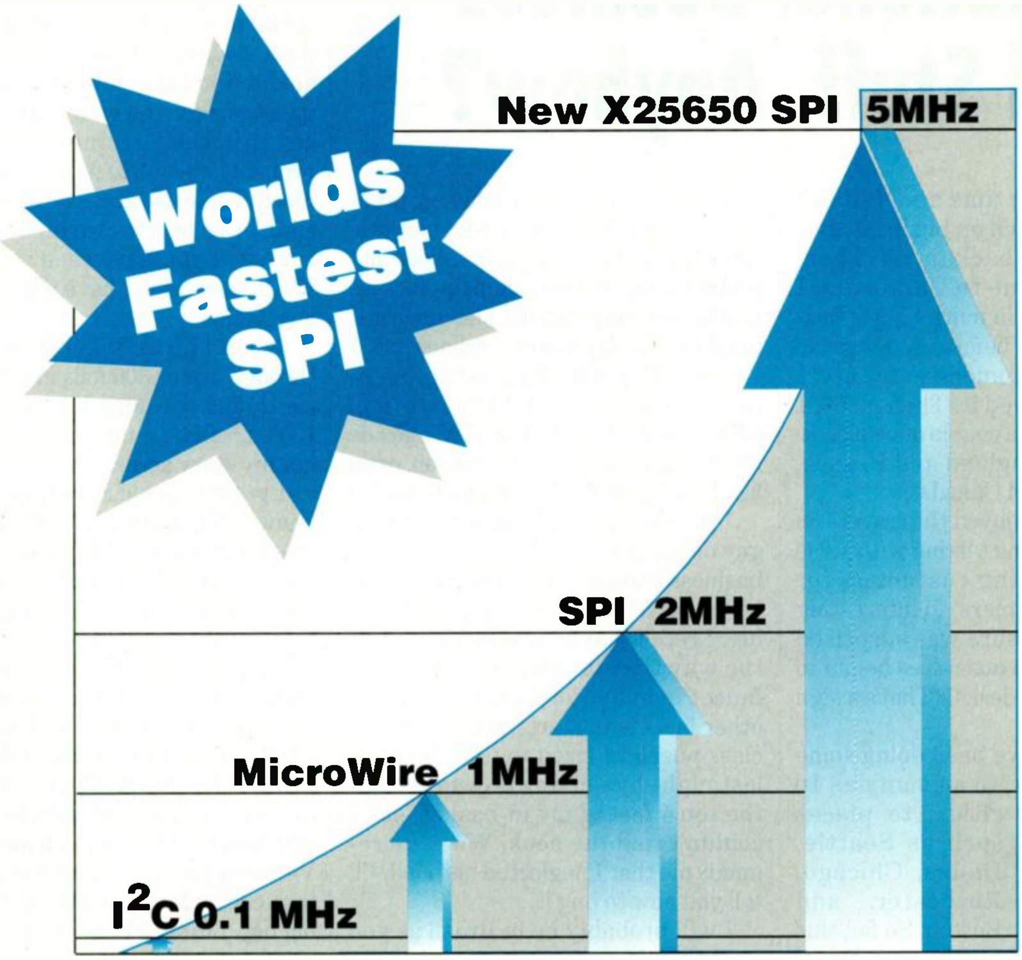

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READER SERVICE 184

Computer Tech Support:

Surviving With (Or Without) It.

Given the complexity of today's computers and software, most users have had some sort of support problem. Contrary to ad hype, bringing a raw new machine to a workable state can be a nightmare. A case in point is my experience bringing up a new Pentium. I'd like to share a major lesson in support work-arounds.

Some time back, the computer fairy dropped a new Pentium computer on me, supposedly ready to "plug in and play." Was it ready to go? "Yes, but..." It came with DOS and Windows 3.1 (before Win95), but no applications. After resolving some initial conflicts, the new machine was finally up and running! The hard drives were the fastest I'd ever used, and PSpice simulations ran faster than I had ever seen; literally a screen blur for small circuits. A warm, fuzzy feeling... but little did I know what was coming!

The first "gotcha" came about when I tried to run standard Internet software, specifically an early Netscape series beta version. It would come up and seem OK, but if news or mail was called, BOOM! A big ugly GPF (general protection fault), pointing a finger to the video driver. Of course, this made that Netscape unusable, and thus began my support story.

Some folks suggested disabling the vendor's 1024x768x256 color driver for the machine's S3 video system. Sure enough, going back to the standard Windows VGA driver cleared the GPF problem, seemingly confirming the S3 driver as the culprit. Others offered that it might be the "buggy" Netscape program. My gut feeling was that this was hokum, but hey, I couldn't argue. Another Netscape version ran just fine with the high-resolution S3 video driver. So the problem became one of confirming for sure if it was the vendor's video driver.

This led me to the vendor's 800 # support service, a varied, but uniformly not helpful exercise. A robot-generated e-mail from the vendor's Web site suggested their Compuserve forum, where I found others complaining about similar video problems. It then seemed the real solution might lie elsewhere, with an updated video driver. But then, the S3 BBS (408 654-5676) showed the vendor's S3 864 chip set driver the same as the one on the BBS. Time to punt?

I had read about mysterious communications problems associated with S3-based video systems, specifically that some drivers turn off COM port interrupts for highest video speed. Aha! Then a test with the "problem" Netscape on a 486 machine with a different video system ran just fine, with no hint of crashes. Progress?

Firing up the Internet browser, and doing an Alta Vista search at *http://www.altavista.digital .com/* got more potential S3 information paths than I'd ever dreamed of. Most importantly, a more recent 864 driver! Installing it fixed the Netscape high-resolution driver GPF problems (or so I thought).

WALT JUNG

Elation over the GPF fix quickly ground to a halt. Using the trace function of the system's TCP/IP software (Peter Tattam's Trumpet Winsock), I found I was getting COM port overrun errors during file transfers. What saved things was the built in buffering of the PPP protocol—robust enough to correct the errors, but with a throughput reduction.

Internet USENET group discussions on this topic ultimately proved invaluable, in particular those by John Navas and Albert P. Belle Isle, *http://users.aimnet.com/~jnavas/ modem/faq.html*, and: *http://www.cerberus-sys.com/~belleisl/ mtu_mss_rwin.html*

As it turns out, the latest S3 drivers have an optional "bus-throttle" switch, which can defeat the S3 video system's COM port control. It is installed within the video driver's [DISPLAY] section of SYSTEM.INI, as:

bus-throttle=on

With this final detail in place, I was able to transfer megabyte files at speeds of 57.6 kbits/s or more, without overrun errors, and with a video mode of 1024x768x64k display colors!

In spite of the fact that this troubleshooting chronology consumed calendar months, I still find the entire experience a positive one. Why? Because real answers can exist beyond the canned and often limited world of vendor support.

While my video driver solutions were totally bankrupt from the vendor support point-of-view, that just wasn't the final answer. The computer related (and other) information available via the Internet is simply immense, as is the speed of access.

Since that first experience, I've also made some more recent and just-as-effective use of the Internet newsgroups. For example, during an upgrade to Win95, when Microsoft's dial-up networking didn't function properly for me, I found lots of generally helpful answers on the USENET news group *alt.windows95*. If you are having trouble getting the dialer to automatically dial on demand without the default prompt pause (as I was), you may want to do this: Download and install the Microsoft ISDN upgrade package from: *http://www.microsoft.com/kb/ articles/q145/9/87.htm* This will bring you directly to article ID Q145987, which specifically addresses this ISDN-related upgrade for Win95. It also happens to fix the dialer prompt problem. And no, you do not need to be using ISDN to take advantage of this particular upgrade.

TIP: The next time you encounter a vacuous tech support response, be resourceful. Check out the Internet news groups. You often won't even need to post a query on a common problem, as others will already be describing how to fix it. Thanks to Peter Tattam, John Navas, Albert P. Belle Isle, Hampton Childress, and the many other knowledgeable users who frequent these groups and share some otherwise obscure technical information.

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A longtime contributor to Electronic Design, he can be reached via e-mail at Walter.Jung@Analog.com.

The M-EZAnalog™ Semicustom Power IC:

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- Fast prototype delivery
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- Low cost

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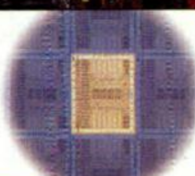

M-EZAnalog™

The semicustom MPD8021 is ideal for a host of analog power applications — motor control, bus interfaces, power supplies, lamp and display drivers, test equipment, and others.

The single-chip MPD8021 takes up less board space and is faster to implement. Micrel combines low-voltage analog and digital circuits with high-voltage DMOS power drivers on one chip.

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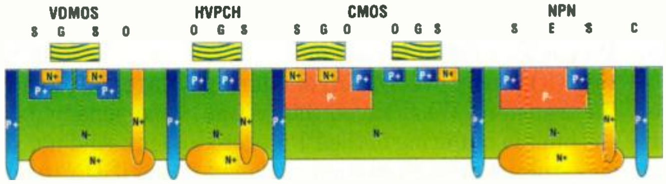

Four of the many types of devices available on the MPD8021. This junction-isolated process includes VDMOS, LDMOS, HVPCH, digital and analog CMOS, NPN, PNP, diodes, capacitors, and resistors all available for discretionary wiring on the same product. VDMOS transistors are not restricted to grounded-source applications.

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Micrel offers quick turnaround to capitalize on product opportunities. We provide six-week prototyping and quick, efficient production turn-on. The MPD8021 is cost-effective, even for volumes of less than 1000 pieces, or for many more. For other customer-specific needs, Micrel Semiconductor provides development programs ranging from project-specific needs to full turnkey solutions.

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READER SERVICE 156

10-Bit, 100-Msample/s ADC With High Bandwidth

The AD9070 is a high-performance, 10-bit ADC with a usable bandwidth of typically 230 MHz, well in excess of the 100-Msample/s sampling rate. The part requires a –5-V supply and an encode clock for operation and may be operated in a positive-ECL environment with a +5-V supply. Power consumption is 600 mW at full sampling rate. It's expected that the part will find broad applications in point-to-point and satellite communications, direct IF sampling, high-definition television, spectrum analyzers, medical imaging, digital oscilloscopes, and transient recorders where the high bandwidth will help the designer eliminate track-and-hold circuitry. The converter is available in a 28-pin ceramic DIP package for MIL-STD-883 applications, and in a 28-pin SOIC package at $68 each in lots of 1000. An evaluation board is available and a TTL version will be released soon. PMcG

Analog Devices Inc., 804 Woburn St., Wilmington, MA 01887; (617) 937-1428; fax (617) 821-4273. **CIRCLE 490**

512-Point Switch IC Simplifies Gigabit Ethernet And ATM

The VSC850 is a 16-by-32 crosspoint switch IC for 1.25-Gbit/s applications. The IC features a 16-by-32 crosspoint switch core with fully differential serial I/Os, a non-blocking architecture with standard TTL interfaces for control logic ,and ECL interfaces for high-speed differential serial I/O. The chip performs with less than 100-ps duty-cycle distortion, less than 200 ps of skew in broadcast mode, and features a total power consumption of under 4.6 W. In addition to applications in Gigabit Ethernet and ATM, the IC should be well-suited for other datacom and telecom switch cores, high-speed routers, Fibre Channel applications, and proprietary computer networks. This part represents the company's first entry in the development of high-bandwidth network switching products. The VSC850 comes in a 208-pin PQFP package, with production quantities now available at $143 each in 1000-piece quantities. PMcG

Vitesse Semiconductor Corp., 741 Calle Plano, Camarillo, CA 93012; (805) 388-3700; fax (805) 987-5896. **CIRCLE 491**

Low-Power, Serial Interface 12- And 16-Bit ADCs

The ADS7812 and ADS7813 are low-power, single +5-V supply, 12- and 16-bit sampling ADCs with internal clock, sample-and-hold amplifier, internal voltage reference, and serial data interface. The analog-to-digital conversion uses a capacitor-based SAR and both parts are pin-compatible. Conversion time is 20 µs while sampling rate is 40 kHz, and SINAD for the 7812 is 72 dB (minimum) and 87 dB minimum for the 7813. Integral nonlinearity is ±0.5 LSB for the 7812 and ±2.0 LSB for the 7813. Input voltage ranges include ±10 V, ±5 V, 0 to 4 V, 0 to 10 V, and a high-impedance 0.3 to 2.8 V. Applications are expected to be in the medical-instrumentation, robotics, industrial-control, test-equipment, and digital-signal-processing markets. Delivery is from stock, with the devices in either 16-pin plastic DIPs or SOICs at $9.25 in 1000s for the ADS7812 and $25.95 for the ADS7813. PMcG

Burr-Brown Corp., 6730 S. Tucson Blvd., Tucson, AZ 85706; (520) 746-1111; fax (520) 746-7401. **CIRCLE 492**

Small LCD Display Module Has Full VGA Capabilities

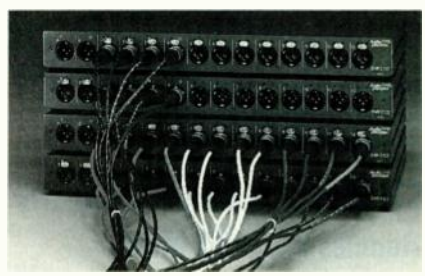
The HS47VGA is the first of several VGA modules that are planned for introduction in 1997. It measures 4.7 in., and features full 640 by 480 VGA functionality and a 30:1 contrast ratio. For design flexibility, the module comes

with or without a backlit power supply and interfaces with standard flat-panel drivers for PCs. The 7.0-mm-thick module weighs 116 g. It's backlit with a cold-cathode fluorescent tube, incorporates a 1:240 duty-multiplex driver, and has non-glare surface texture for all of its 640 by 480 by 3 (RGB) pixels. Pixel dots are 0.13 mm high and 0.03 mm wide, with 0.02-mm spacing vertically and horizontally. The viewing area is 98 mm wide by 74 mm high while the overall dimensions are 140 by 98 mm. The module requires between 15 and 27 V for the LCD drive and 5 V for the two logic circuits with connections on a Molex 30-pin connector. Current consumption is typically 3.5 mA for the LCD and 63.9 mA for the logic. Pricing starts at $325, including the power supply. PMcG

Shoreline Electronics Inc., 2098 B Walsh Ave., Santa Clara, CA 95050; (408) 987-7733; fax (408) 987-7735. **CIRCLE 493**

12-Channel Audio Switcher For Production And Test

The SWR-2122 audio switcher line may be used in broadcast applications for inserting audio test equipment into the broadcast chain for proof of performance or FASTTEST multitone audio testing. In engineering and manufacturing applications, the switchers are used for both test and measurement, as well as large scale production testing with up to 192 channels containing 16 units. The products are available in



both balanced (XLR) and unbalanced (BNC) versions, with a third type built as a patch-point switcher so that a test generator could be inserted while an analyzer measures the output of the previous audio patch-point or device. All of the versions feature channel-selection LEDs and audio performance such as crosstalk better than –140 dB at 20 kHz in the balanced mode. Production quantities of the SWR-2122 switcher are available at $1250 each for the standard version and $1400 for the patch-point version. PMcG

Audio Precision, P.O. Box 2209, Beaverton, OR 97075; (503) 627-0832; fax (503) 641-8906. **CIRCLE 494**

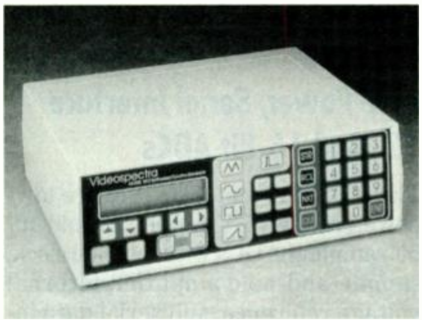
Evaluation Kit Checks Out Fujitsu's MB86831

Designers can evaluate the performance of the MB86831 SPARClite series of embedded RISC microprocessors using a kit that contains all needed tools. The kit includes a 66-MHz MB86831 CPU, an evaluation board, and all required software and documentation in CD-ROM format. The CD holds a data sheet, user manual, evaluation board software and software guide, installation guide, and a DOS-hosted GNU-C cross compiler that's optimized to produce code for any member of the SPARClite family.

Users can debug test code on the board with the GNU GDB software, which runs on Windows. It offers complete debugging commands, including single-stepping, and hardware and software breakpointing. The board will accept faster versions of the series, like the 80-MHz device now available in samples, and the 100-MHz version due out later this year. Users will require a 486-based PC running Windows 3.1 or higher, as well as relevant power supplies and cables. The MB86831 evaluation kit is priced at $99. JN

***Fujitsu Microelectronics Inc.**, Customer Response Center, 3545 N. First St., San Jose, CA 95134-1804; (800) 866-8608; fax (408) 922-9179; http://www.fujitsumicro.com.*
CIRCLE 495

Synthesized Function Generator Handles DC To 12 MHz



The Model 1010 Function Master is a synthesized waveform generator that supplies sine, square, sawtooth, and triangle waves over a range of dc to 12 MHz. The synthesized unit continuously regulates the output to avoid frequency drift. Pulse, burst, and sweep modes also are available, as are a variety of triggering options. The generator delivers rise times of less than 10 ns. An on-board memory stores up to 27 program setups. With the CW pulse mode, the operator can independently adjust the pulse width and frequency. The instrument's front panel features tactile keys and an LCD screen for displaying waveform parameters. Power consumption is 35 W, provided by an external power module. The Model 1010 starts at $1195, with delivery from stock. Options include an analog output, an RS-232C serial port, and a ruggedized portable version. JN

***Pforg Instruments**, 7201 Haven Ave., Suite 323, Alta Loma, CA 91701; (909) 987-4300; fax (909) 989-7320; http://www.earthlink.net/videospectra.*
CIRCLE 496

Automated System Programs Latest Fine-Pitch Packages

The ProMaster 970 automated fine-pitch programming system incorporates a handler and programmer specifically designed to work together to accommodate fine-pitch devices. The system handles memory, microcontroller, and logic ICs. It employs a state-of-the-art, dual-head pick-and-place handler, a new-generation programmer, and a just-developed laser marking system. Control is provided by the company's TaskLink for Windows interface.

The programming system supports PLCC, TSOP, SOP, BGA, QFP, SOIC, and other packages, including emerging types like micro ball-grid array and chip-scale packages. The socketing technology was designed to minimize cost in high-mix applications. The integrated programming system features 256 universal pins with software-switchable ground. Therefore, one adapter is able to support all products in a particular package type.

A laser alignment system is standard, but users also can select a downward-looking, arm-mounted camera for autocalibration of the handler movement and an upward-looking, table-mounted camera for indexing extra large devices. Throughput is specified at 1100 devices per hour, depending on programming time. Support is provided for trays, tubes, and tape as input or output media. The ProMaster 970 is priced at under $300,000. JN

***Data I/O Corp.**, 10525 Willows Rd. N.E., Redmond, WA 98073-9746; (206) 881-6444; fax (206) 881-6856.*
CIRCLE 497

PC-Based Digital Scope Has Advanced Triggering

The DSO-2100 series of PC-based digital oscilloscopes features two-channels of 100-Msample/s, 8-bit sampling with single-shot capture, ad-

vanced triggering, and a 32-kpoint memory. The units' ruggedized enclosure measures 7 by 3.5 by 1 in. and connects to a PC's parallel port through an included DB25 cable. An external 9-V dc supply also is incorporated. The standard model DS0-2102S makes 10 pulse-parameter measurements and has a TV sync trigger. It costs $499.

The math model DSO-2102M makes 45 pulse-parameter measurements; has TV, pulse width, edge count, and width count triggering; does pass/fail testing on 10 sets of pulse-parameter high/low limits; and performs 32-kpoint FFTs for spectrum analysis. The math model is priced at $599. Instrument control and waveform viewing, manipulation, and analysis in color is provided by the company's FrontPanel software. Users can store waveforms in ASCII or binary format, data or voltage scaling, or use commas for direct transfer to spreadsheet programs. Delivery is immediate. JN

***Link Instruments**, 369 Passaic Ave., Suite 100, Fairfield, NJ 07004; (201) 808-8990; fax (201) 808-8786; sales@LinkInstruments.com.* **CIRCLE 498**

DIGITAL ICs

Speedy 16-Bit MCU Packs 128 Kbytes Of Flash

The TLCS-900/H series of 16-bit high-performance microcontrollers now boasts a new member. It offers designers programming flexibility by including 128 kbytes of on-chip flash EEPROM that can be programmed and erased through the controller's built-in single-boot mode. Designated the TMP95FW86F, the chip includes a small, 2-kbyte boot ROM that allows designers to rewrite the flash program storage without having to remove the MCU from the circuit board, thus permitting the system manufacturer to add new software at any time during the product manufacturing cycle. In addition to the 128 kbytes of flash memory, the 100-lead controller includes 4 kbytes of SRAM, multiple timers (two event channels, three 16-bit channels, two 16-bit input capture channels, ten 16-bit output-compare channels, and four channels that provide capture and compare capability), and many other resources.

Some of those additional resources include a 12-channel, 10-bit ADC; three pulse-width-modulation channels; a four-channel microDMA engine; a stepping-motor controller (four phase, two channels); three serial UARTs; 77 I/O lines; and a JTAG text controller to aid in on-chip module testing as well as full system testing. The internal 16-bit CPU has a bank of general-purpose, 32-bit registers and handles a 16-Mbyte linear address space. This enables the chip to deal with large address spaces.

Instructions, which are an enhanced form of the Z80 8-bit command set at the mnemonic level, have been optimized for use with C-language development tools. Lastly, the microcontroller includes four standby modes that help trim the operating power when the chip runs from a 4.5-to-5.5-V supply and over a –40 to +85°C temperature range. Programming and erasure, though, requires a more restricted operating temperature range of –20 to +70°C. In lots of 10,000 units, the TMP95FW86F sells for $40 each. DB

Toshiba America Electronic Components Inc., 9775 Toledo Way, Irvine, CA 92618; Bob Salem, (714) 455-2000; http://www.toshiba.com/taec

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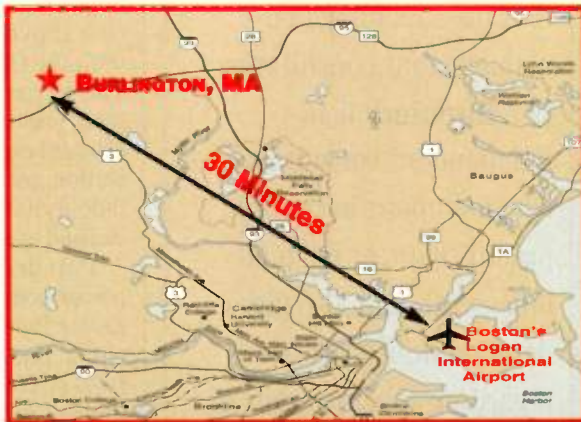

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WRH

REV-B

COMMUNICATIONS

Software Predicts Signal Attenuation

PMod/fc is a software toolset that calculates the attenuation of rf signals propagated through the air. The tools perform rf propagation analysis for earth-space paths using standard models and a global database of atmospheric parameters. Included in the calculations are the attenuating effects of rain, water vapor, oxygen, and hydrosols along an rf path. The tool is suited for systems planners and link analysts concerned with atmospheric impairments, particularly at frequencies above 10 GHz. One tool is used with the OPNET simulation package. The second tool is a standalone application that runs under Windows. Additional capabilities, such as depolarization, combined-effect analysis, and fade dynamics are available for specialized applications.

PMode/fc operates as a receive power node model in OPNET's Transceiver Pipeline by determining attenuation due to atmospheric effects and free-space path loss. It first determines ground-station location, then accesses Stanford Telecom's global library of statistical distributions of rain rates, integrated water-vapor concentrations, and cloud liquid-water contents. These statistics, along with satellite system parameters and accepted models of atmospheric attenuation, are used to calculate total path loss. Pricing is $9000. LG

***Stanford Telecom**, 1761 Business Center Drive, Reston, VA 20190-5333; (703) 438-7924 or 1 (888) 840-PMOD.* **CIRCLE 500**

Data/Fax Modem Card Suits Pentium Hosts

For use by OEMs and systems integrators, a data/fax modem card developed by SMART Modular Technologies transmits data and fax at speeds up to 33.6 kbits/s by using spare processing cycles of the microprocessor found in Pentium-powered computers. The Host Singal Processing (HSP) V.34 Type II PC modem card meets the speed requirements of multimedia applications, on-line services, and the Internet. It's compatible wiht most Pentium-powered computers, data/fax communications packages and operating systems, and CCITT Group III specifications. It also operates under card and socket services, including IBM's EasyPlay and SystemSoft's CardSoft. Advanced error correction with V.42 protocol facilitates safe and clear transmissions. The product is Windows 95 compatible, features Plug & Play support, and complies with all PC card standards. Unit pricing for the data/fax modem card is $75 for quantities over 500. LG

***SMART Modular Technologies Inc.**, 4305 Cushing Pkwy., Fremont, CA 94538; (510) 623-1231.* **CIRCLE 501**

Gigabit Interconnect IC Speeds Buses, Boxes, Backplanes

The VSC7214 is a four channel, multigigabit interconnect IC that provides serialized, duplex transfers of data across buses, backplanes, or across short system-to-system connections. Its four, eight-bit channels have an aggregate bandwidth of 10 Gbits/s, and can be easily reconfigured as a single 32-bit channel. A scalable interconnect architecture of arbitrary size can be created by synchronizing multiple VSC7214s in parallel.

The VSC7214 consists of a quad 8-bit parallel-to-serial and serial-to-parallel, 1.25-Gbit/s transceiver that can operate as either a fully synchronous 32-bit interface or as four independent 8-bit transceivers. Each channel can clock its eight channels at a maximum speed of 130 MHz, yielding a maximum unencoded duplex aggregate data-transfer rate of 8 Gbits/s. The IC includes encoding/decoding to integrate a clock signal and establish error checking, resulting in a total data channel throughput of 10 Gbits/s over four duplex channels. Bit, character, and channel synchronization also are possible, thanks to an on-chip elastic buffering scheme.

Fabricated in H-GaAs, the VSC7214 operates off a single 3.3-V supply and dissipates 4.3 W. It's housed in a 160-pin thermally enhanced PQFP. Sampling now, the VSC7214 is priced at $98 each in 1000-piece lots. LG

***Vitesse Semiconductor Co.**, 741 Calle Plano, Camarillo, CA 93021; (805) 388-3700; fax (805) 987-5896.* **CIRCLE 502**

New From Allegro

Digital Hall-Effect Gear Tooth Sensors For Your Industrial Applications

Continuing our leading-edge tradition, Allegro has now introduced a full line of highly-accurate, fully-functional solutions that include a Hall-Effect IC and a magnet... designed into a small package, as small as 9mm in diameter!

The new ATS610 and ATS611 sensors from Allegro are optimized Hall IC and magnet assemblies that provide a digital output for your industrial gear-tooth sensor applications. The Hall IC uses a patented track-and-hold peak detecting circuit that provides exceptional air gap and accuracy performance.

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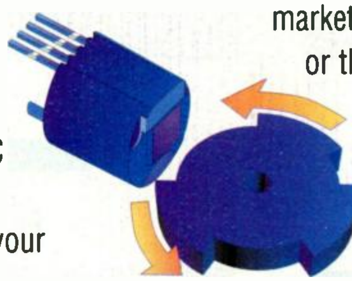

The convenience of the 9mm packaging makes the ATS610 ideal for use in unique applications such as exercise equipment, elevators, gas pumps, garage door openers, machine tools and even agricultural equipment such as seed spreaders!

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SA/SB Package

SC Package

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- ATS610 available in 9mm dia. x 9mm length "SA" package
- ATS611 available in 9mm dia. x 7mm length "SB" package
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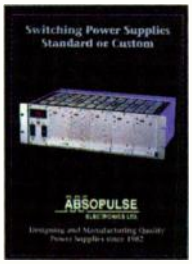

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http: www.unitrode.com

CIRCLE 253

UNITRODE CORPORATION

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CIRCLE 255

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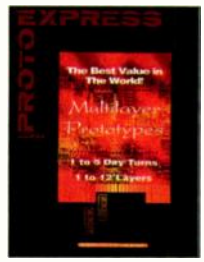

CIRCLE 257

PROTO EXPRESS

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CIRCLE 258

AMERICAN MICROSYSTEMS, INC

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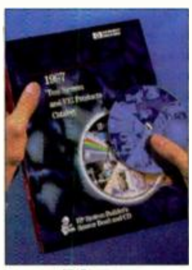

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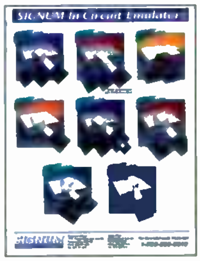

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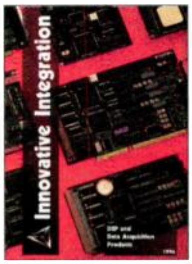

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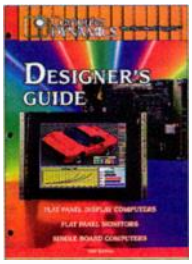

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COMPUTER DYNAMICS

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TANNER RESEARCH

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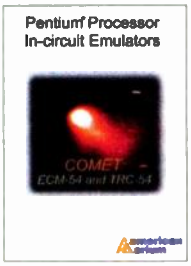
American Arium has been the primary market supplier of Pentium® processor In-circuit Emulators since 1991. In 1995, the company introduced their Pentium® Pro In-circuit Emulator. Recently, American Arium announced the release of Comet In-Circuit Emulators. These were specifically designed for the embedded software developer, with special attention paid to the 66Mz real-time trace engine and ultra-accurate breakpoints. The Comet ECM-54 is a portable low cost solution which provides processor control through the Intel defined, JTAG debug port. Comet TRC-54 is a full featured In-Circuit Emulator with American Arium Data Capture Technology.



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Western Design Center's product selection and developer guide describes our 65C02-BASED CMOS low power IC microprocessors. Included is information about our chips, boards and licensable cores.
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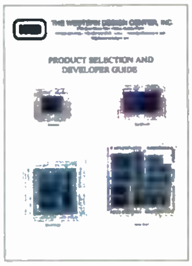

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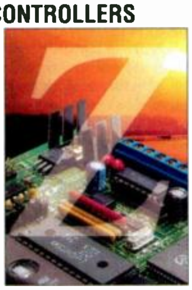

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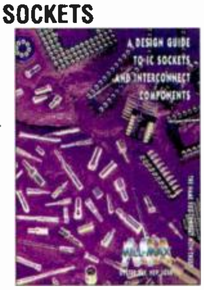

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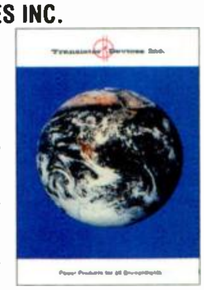

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ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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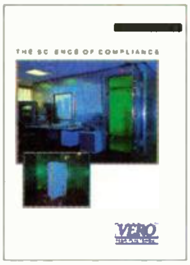

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The 1997 International source Book offers detailed specifications on Ecliptek's through-hole and surface-mount crystals and oscillators. Visit our internet site at http://www.ecliptek.com. Phone: (714) 433-1200, Fax: (714) 433-1234, or E-mail: ecsales@ecliptek.com.

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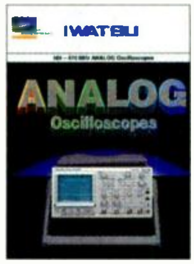

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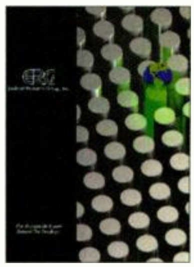

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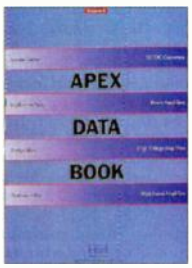

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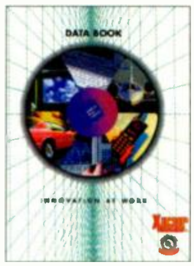

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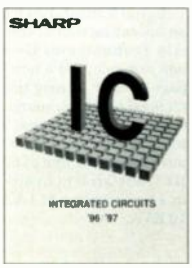

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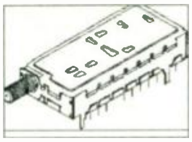

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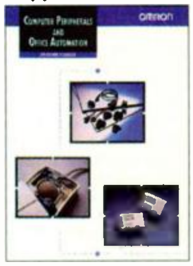

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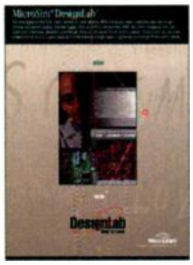

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INTERFACE TECHNOLOGIES

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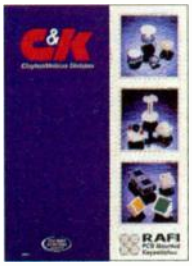

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C&K COMPONENTS, INC.

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The Windows-compatible Instrupedia- Your Interactive Encyclopedia for Instrumentation features more than 60 tutorial and "how-to" application notes to help users learn how to combine hardware and software to built computer based systems for instrument control and data acquisition, analysis, and presentation. Instrupedia includes more than 20 User Solutions.

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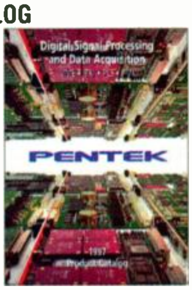

CIRCLE 301

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TRANSFORMER CATALOG

Signal Transformer Co., an operating unit of the Insilo Technologies Group, has just released a new 40-page, 4 color catalog that is an ideal reference source for engineers and buyers. signal Transformer offers the most extensive line of 50/60 Hz transformers available in a power range of 1 VA to 10 KVA.

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SIGNAL TRANSFORMER

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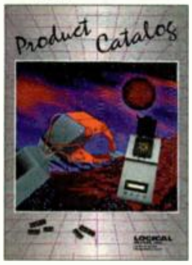
ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

Product Literature News Announcement

Our 28 page four color catalog is an excellent buyers guide for design and production engineers shopping for EPROM /FLASH/PLD/FPGA design, programming, erasing and test tools. The catalog offers products for every budget and level and also includes a host of Socket converters and adapters for DIP, PLCC, TSOP, QFP technologies. For more information call Logical Devices at 800-331-7766. web: http://www.logicaldevices.com



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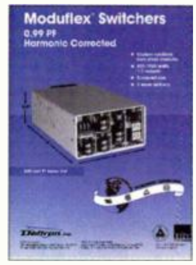

CIRCLE 303

DELTRON INC.

AMPLIFIER SPECIFICATIONS

Techron's new brochure features twelve power amplifiers for power utilities, research, industrial and medical applications including magnetic resonance imaging. The amplifiers operate in power ranges from 50 to 2800 watts. Techron products are used also for chemical analysis, space exploration, vibration test systems, radar installations, automotive research, particle acceleration studies, and noise reduction research.

CIRCLE 304

TECHRON

NEW TEST & MEASUREMENT CATALOG

Keithley offers its new 1997 catalog of test and measurement instruments including DMMs, electrometers, precision sources, voltmeters, source-measure units, power supplies, switch systems and more. Phone: 800/552-1115. FAX: 216/248-6168 http:// www. keithley.com

CIRCLE 305

KEITHLEY INSTRUMENTS

KEPCO HEAVIER-DUTY POWER

Kepco, Inc. has extended its RCW heavy-duty industrial grade power supplies with its new 1500 watt models ranging from 3.3V@300A to 48V@30A. The RCW line now includes models from 350 watts to 750 watts to 1500 watts; are single output modules featuring wide-range input with power factor correction to reduce the harmonics fed back to the mains to below IEC norms; meet EN 60950 safety standard, carry CD mark. Tel: 718-461-7000. FAX: 718-767-1102

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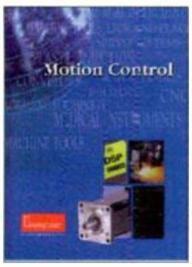
MOTION CONTROL CATALOG

GESPAC' intelligent motion controller uses a 40MHz MC56002 DSP to control 2 or 4 DC, AC or brushless motors. Versions of the board are available for the VME, G-64 and soon for the ISA and CompactPCI buses. The board comes with a powerful PC based software package that helps you automatically determine the mechanical characteristics of the drive assembly and more.



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CIRCLE 308

APPLIED MICROSYSTEMS

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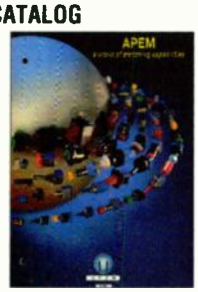
CIRCLE 309

GRAYHILL, INC.

EXPANDED SWITCH CATALOG

APEM's 212 page switch catalog includes the following categories; DIP & Rotary DIPs, Toggles, Rockers & Levers, Pushbuttons, Anti-Vandals, Tacts &Keys, Slides and Industrial controls. A broad family of Control knobs is also offered. Complete specifications and detailed ordering guides greatly simplify switch selection. Many process compatibles and SMT models are offered as well as numerous options and accessories.



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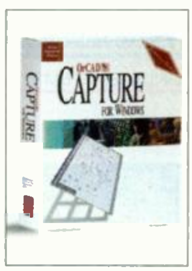

CIRCLE 311

OrCAD

"X86 and 683xx/HC16 Design Tips"

Free application note shows how to use in-circuit emulation to isolate real-time events. Set clock-edge triggers, and then use trace to display system status and the source code leading up to the event. For immediate response: WEB page: www.microtekintl.com Voice: 800-886-7333

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MICROTEK INTERNATIONAL

NEW SWITCHING REGULATORS

Power Trends, Inc. has released a new 80 page full-line catalog for its complete line of Integrated Switching Regulators and DC to DC converters. the catalog introduces significant new products along with extensions to existing product lines. Complete specifications, photos and standard applications are provided for each product along with mechanical configuration options and ordering information.

CIRCLE 313

POWER TRENDS, INC.

TEST & MEASUREMENT ACCESSORIES

The 92-page, full -color catalog includes the complete line of Pomona test accessories. The line includes DMM test accessories and kits, grabbers, oscilloscope probes for a wide variety of electronic and electrical applications, cable assemblies, coaxial adapters, banana plugs, enclosures and IC test clips for popular 2-and 4-sided devices.

CIRCLE 325

ITT POMONA ELECTRONICS

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September 15	8/6/97
October 1	8/22/97
October 13	9/3/97
October 23	9/12/97
November 3	9/24/97
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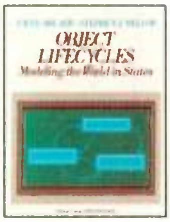
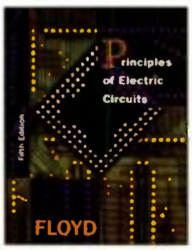


This book approaches domain analysis by showing how to model the dynamic behavior of a system in terms of state and process models. Provides a strictly defined, multi-level formalism powerful enough to be mapped into a variety of designs, and a ready-to-use tailoring of 2167A's analysis DID's, with justification and detailed instructions for compliance. Includes language-independent notation for (OODLE) and strategies for code generation from OOA models using Recursive Design.

251 pp, softcover book, $45.00, Item B2547PM

Principles of Electric Circuits, 5th Edition

Thomas L. Floyd



This edition, complete with a new full-color format features more than 1000 drawings, photographs, charts and diagrams. It provides understandable explanations of complex concepts and non-technical treatment of mathematics, taking a strong applications approach. A unique, innovative feature uses printed circuit boards and a series of hands-on activities to bring chapter material to life by relating chapter theory to real-world applications.

964 pp, hardcover book, $79.00, Item B2768PM

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The International Society for Optical Engineering

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Douglas A. Young

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John P. Borris

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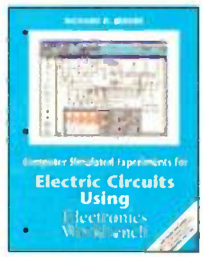

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