ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS-WORLDWIDE

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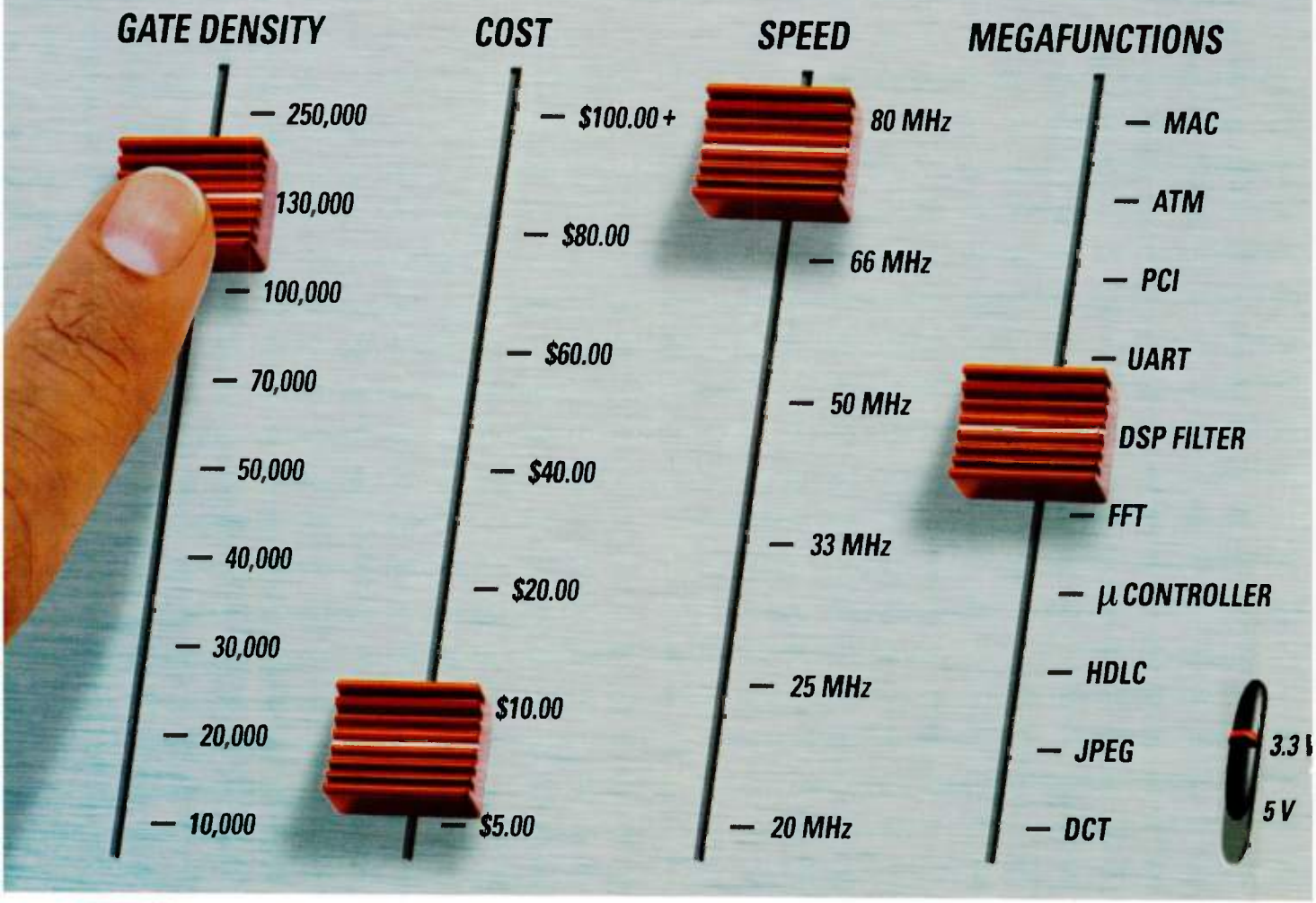
The perfect mix.



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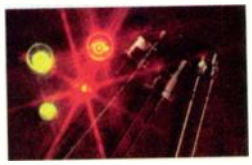

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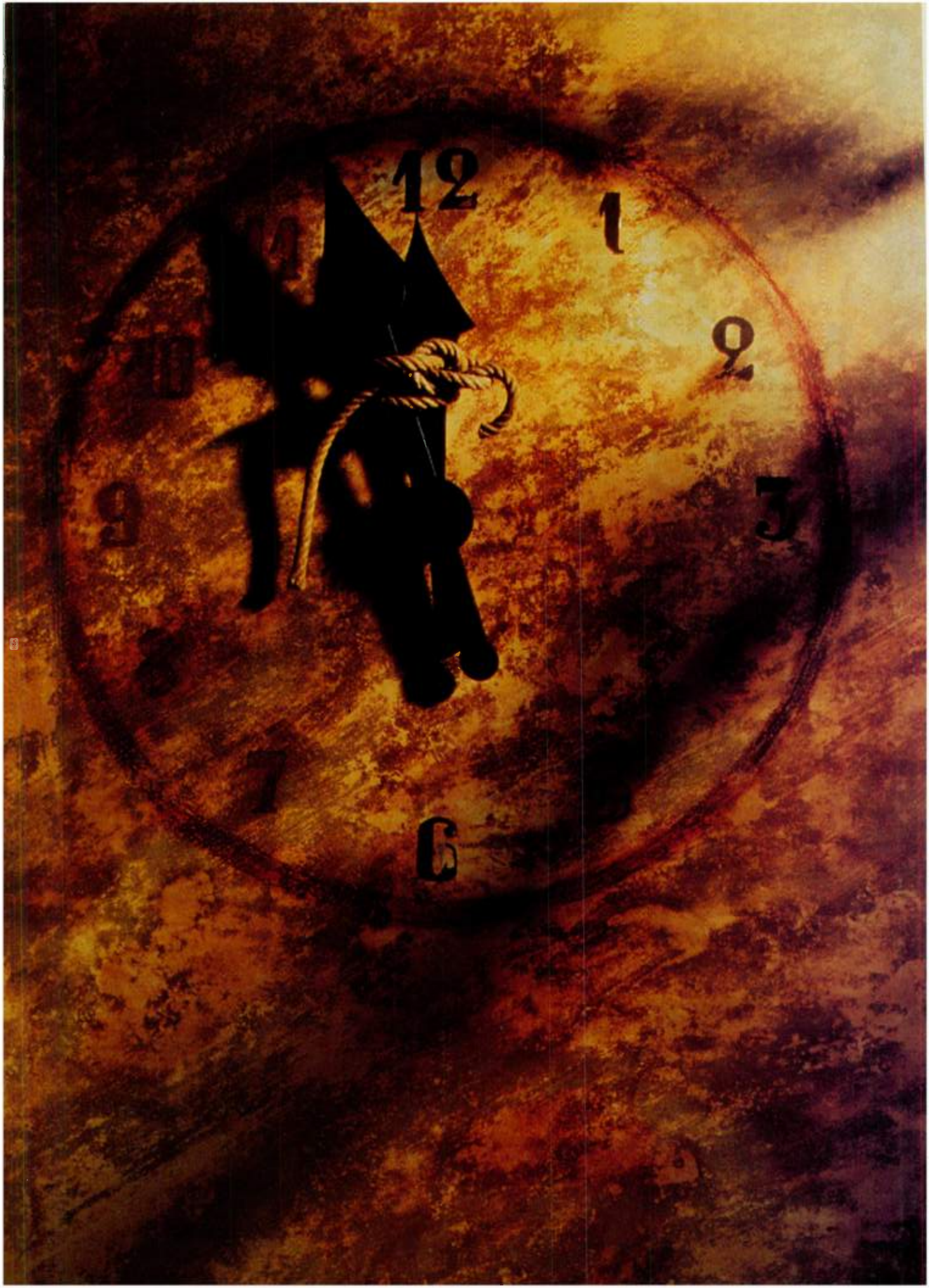
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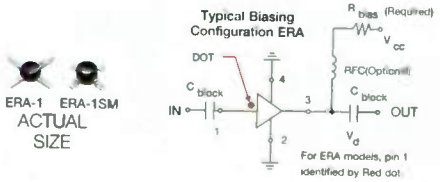

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Osc. Frequency	10kHz or 80kHz, 80kHz*	20kHz or 150kHz, 150kHz**	800kHz
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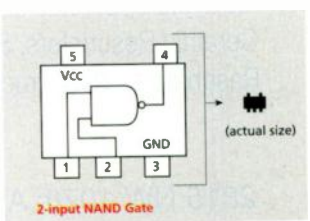
Propagation Delay (typ @ Vcc=5V/CL=15pF)	2.0ns	3.5ns	6.3ns
Output Current (Vcc=4.5V)	32mA	2mA	2mA

Typical TinyLogic Configuration



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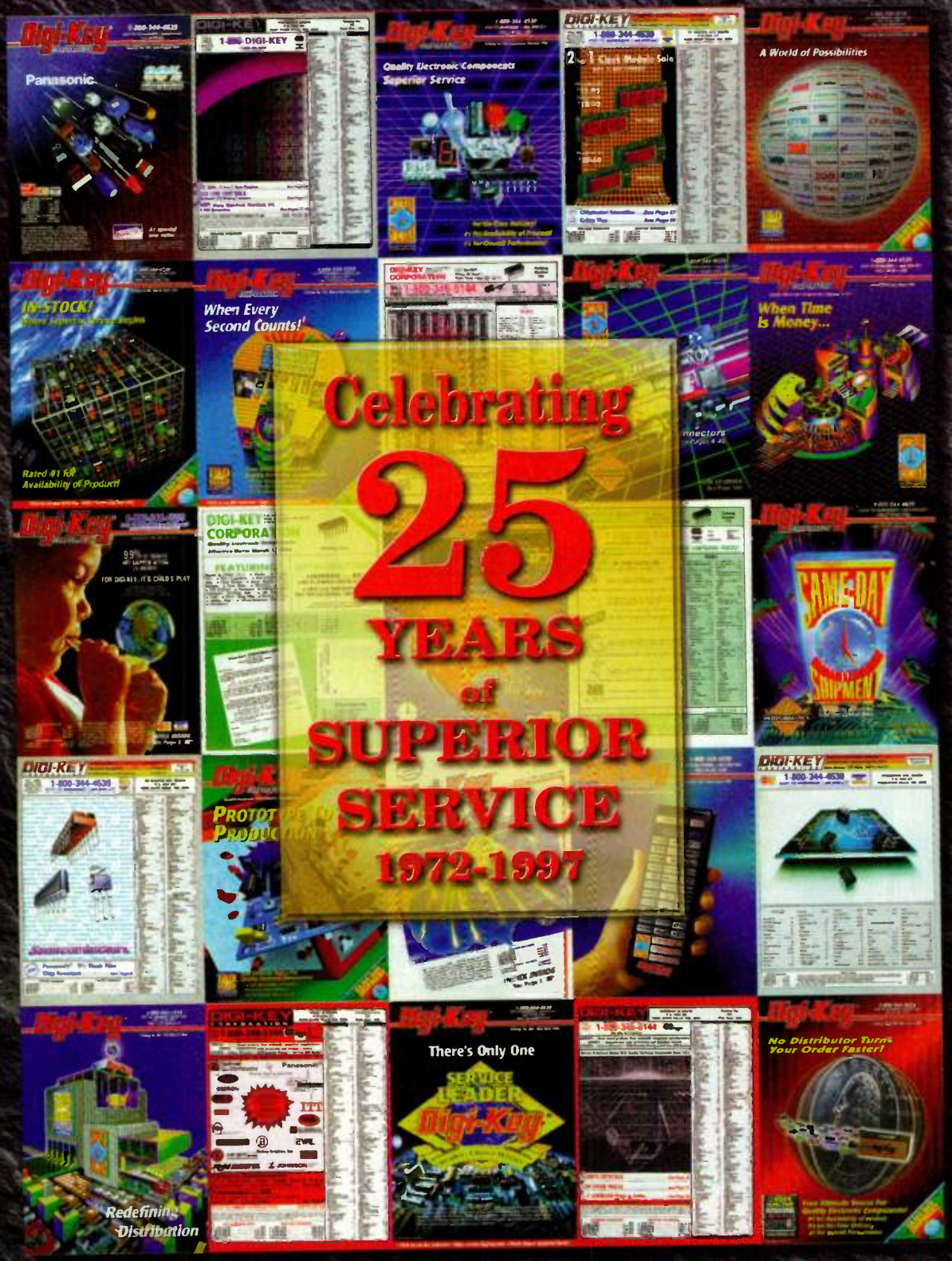

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ICSPAT/DSP World 1997, October 15-17. San Diego Convention Center, San Diego, California. Contact Denise Chan, Miller Freeman Inc., (415) 278-5231; e-mail: dsp@exporeg.com.

IEEE Holm Conference on Electrical Contacts, October 18-22. Wyndham Franklyn Plaza, Philadelphia, Pennsylvania. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Ln., Post Office Box 1331, Piscataway, New Jersey 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

VHDL International User's Forum (VIUF) Conference, October 19-22. Hyatt Regency Crystal City Hotel, Arlington, Virginia. Contact VIUF, (415) 329-0510.

IEEE Telecommunications Energy Conference (INTELEC '97), Oct. 19-23. World Congress Centre, Melbourne, Australia. Contact Robert N.K. Thuan, Network Products-Telstra Corp. Level 14, 242 Exhibition St., Melbourne, Victoria 3000, Australia; +61 3 634 6216; fax +61 3 632 3607

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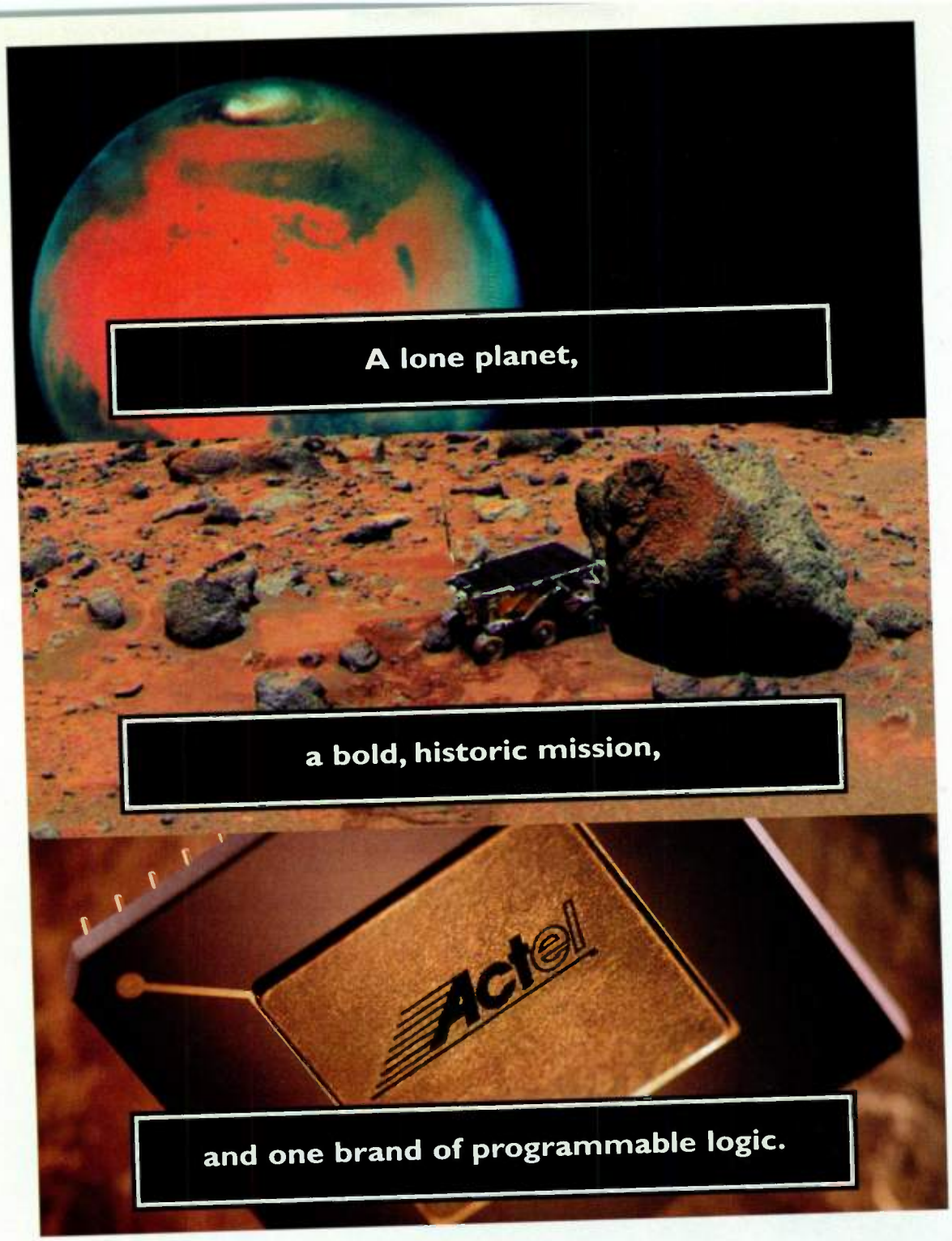

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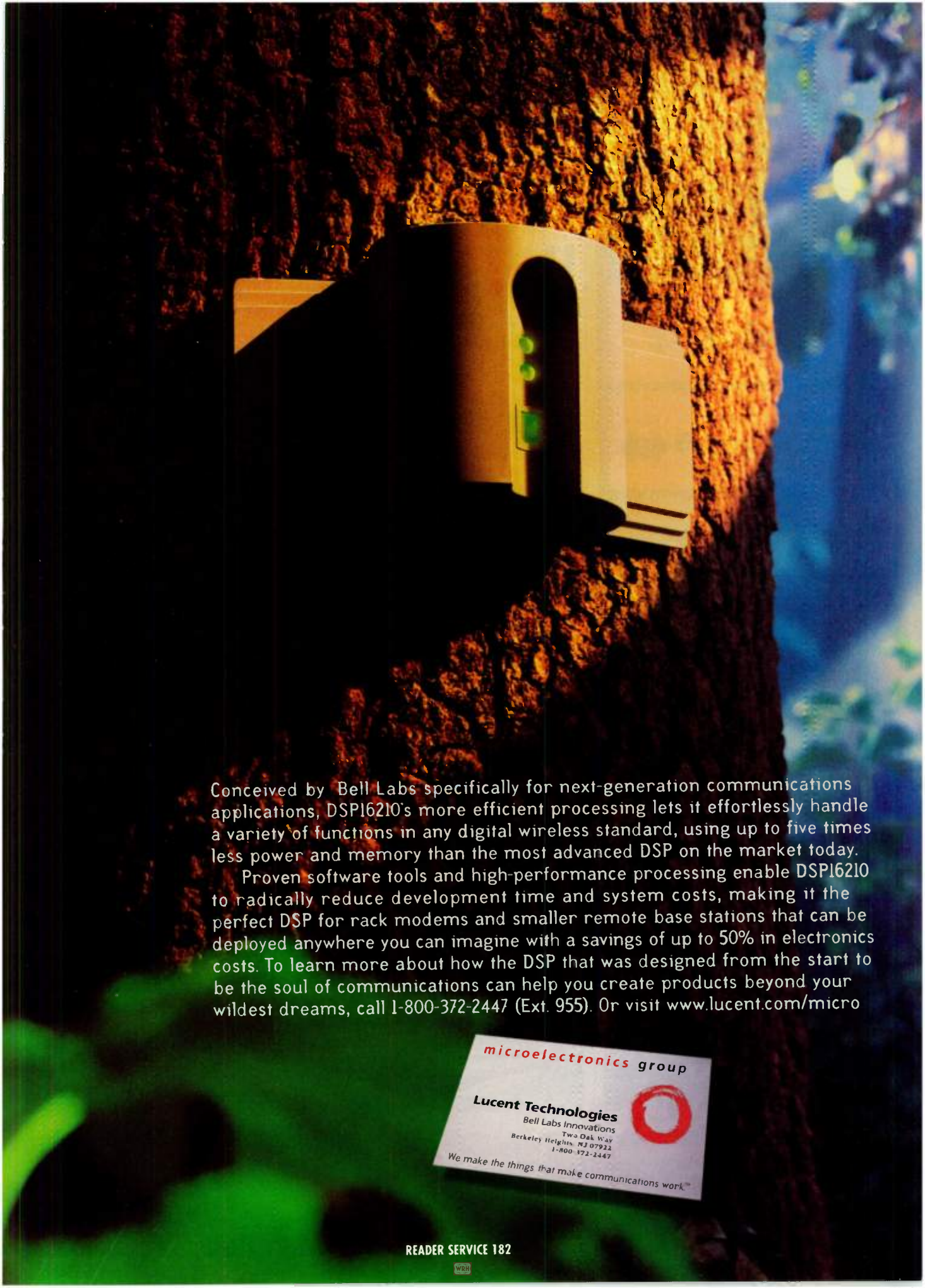
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EDITORIAL

Technophobia—The Designers' Fault?

"You can have great technology and not know how to make proper use of it. And you can have simple technology and it can save your life."
—Akio Morita, chairman of the board and CEO of Sony Corp., from his biography, *Made In Japan*

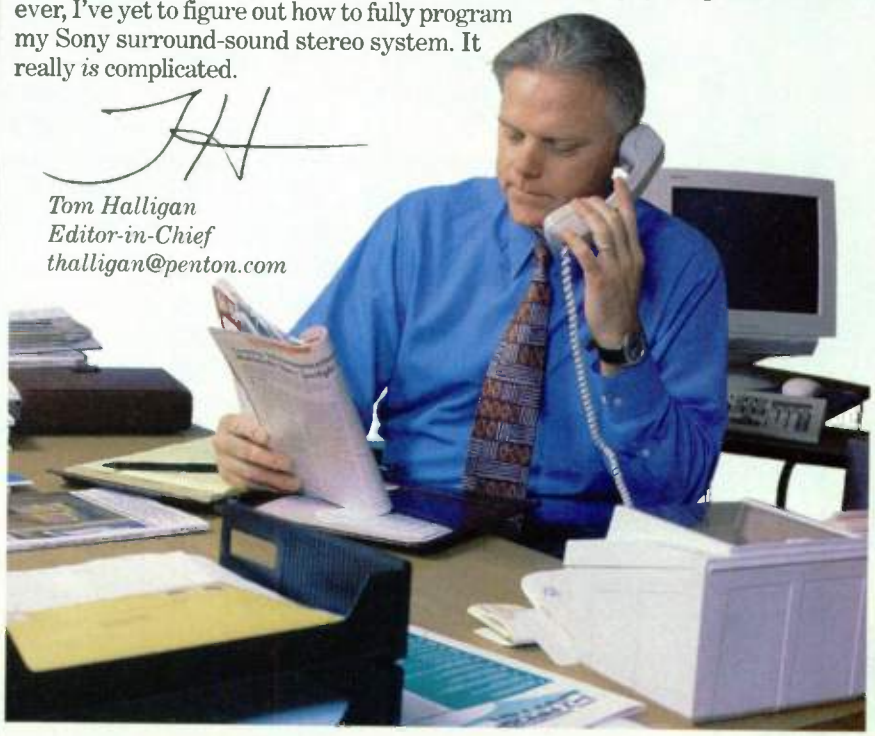
How many times have you heard someone jokingly say in some form or another that he/she would need an engineering degree to program their stereo, telephone, computer, or microwave oven? And the blinking "12 Midnight" on the VCR has become the running catch-phrase for late-night comedians and pundits who joke about the complexity of dealing with modern-day, chip-based products, gizmos, and gadgets.

I read a newspaper article recently which said that 85% of "us" are, to a degree, uncomfortable with technology. Quoted in the article was Donald Norman, vice president of the advanced technology group at Apple Computer Corp., who asserts, "Technophobia is not the people's fault, it's the designers' fault." Norman said that the "best way to cure technophobia is to cure the reasons that cause it; that is, to design things that people can use and design things that won't break."

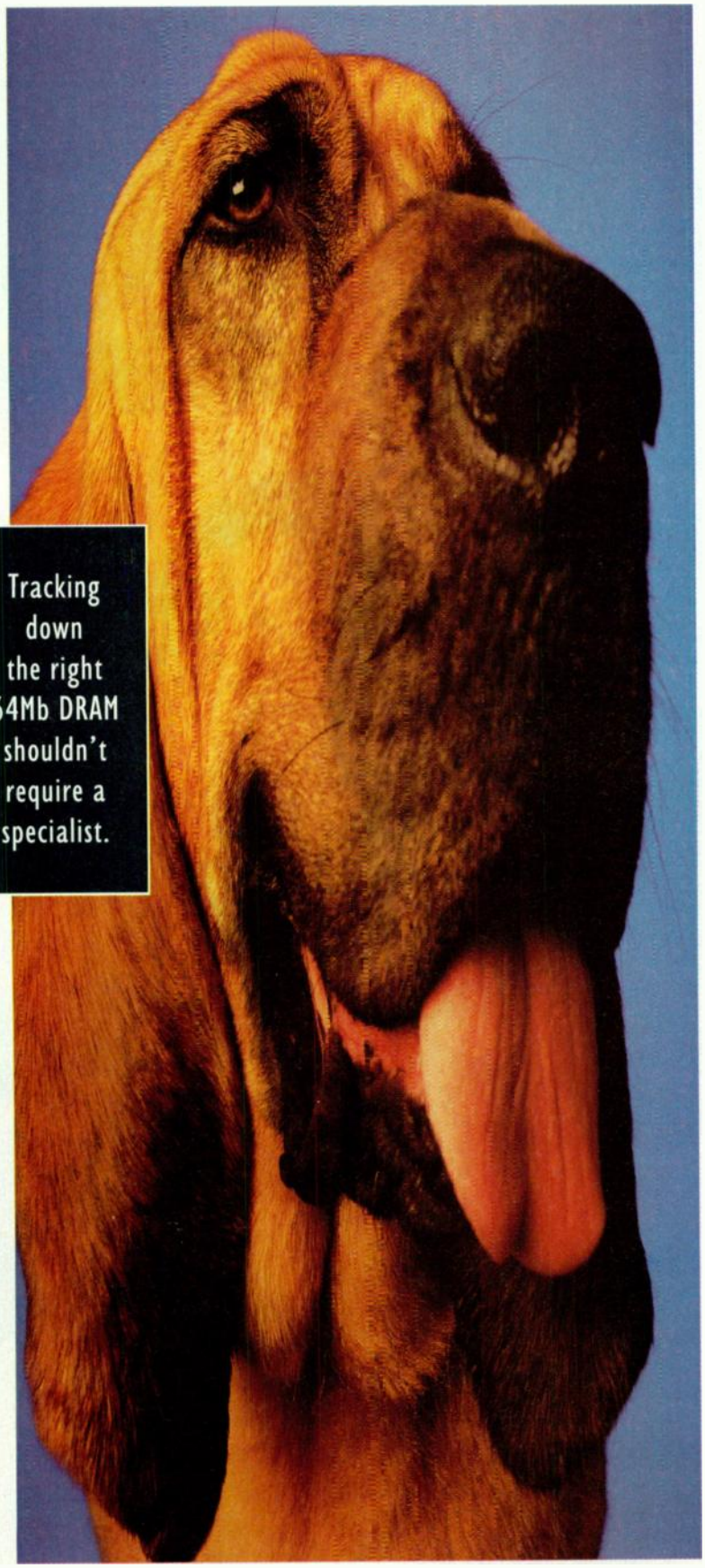
I agree with Norman that there are many examples of poorly designed and overly complicated products that cause angst among the masses. However, I don't think the blame should be placed solely on designers. "Technophobia," I believe, is a combination of three factors: overly complicated and confusing front-ends; poorly written and edited user manuals and documentation; and the end-user/consumer who refuses to set aside the large chunk of time it takes to fully understand and program his/her computer, phone, VCR, or stereo.

Obviously, there have been great strides in product design (especially computers) that are more "user friendly" and that take very little time to set up and use. It took me less than 45 minutes to get my new computer going. But, I haven't plowed through the thick manuals because I don't have the time and I'm only interested in a couple of applications, anyway. There lies another problem. I'll take an educated guess and say that 90% of electronic-based product functions and features are either not used or underutilized because of the above factors. I haven't seen any hard statistics to back it up, but I'll bet my percentage is on target.

I like the above quote from Akio Morita, and his biography is a good read. However, I've yet to figure out how to fully program my Sony surround-sound stereo system. It really *is* complicated.



Tom Halligan
Editor-in-Chief
thalligan@penton.com



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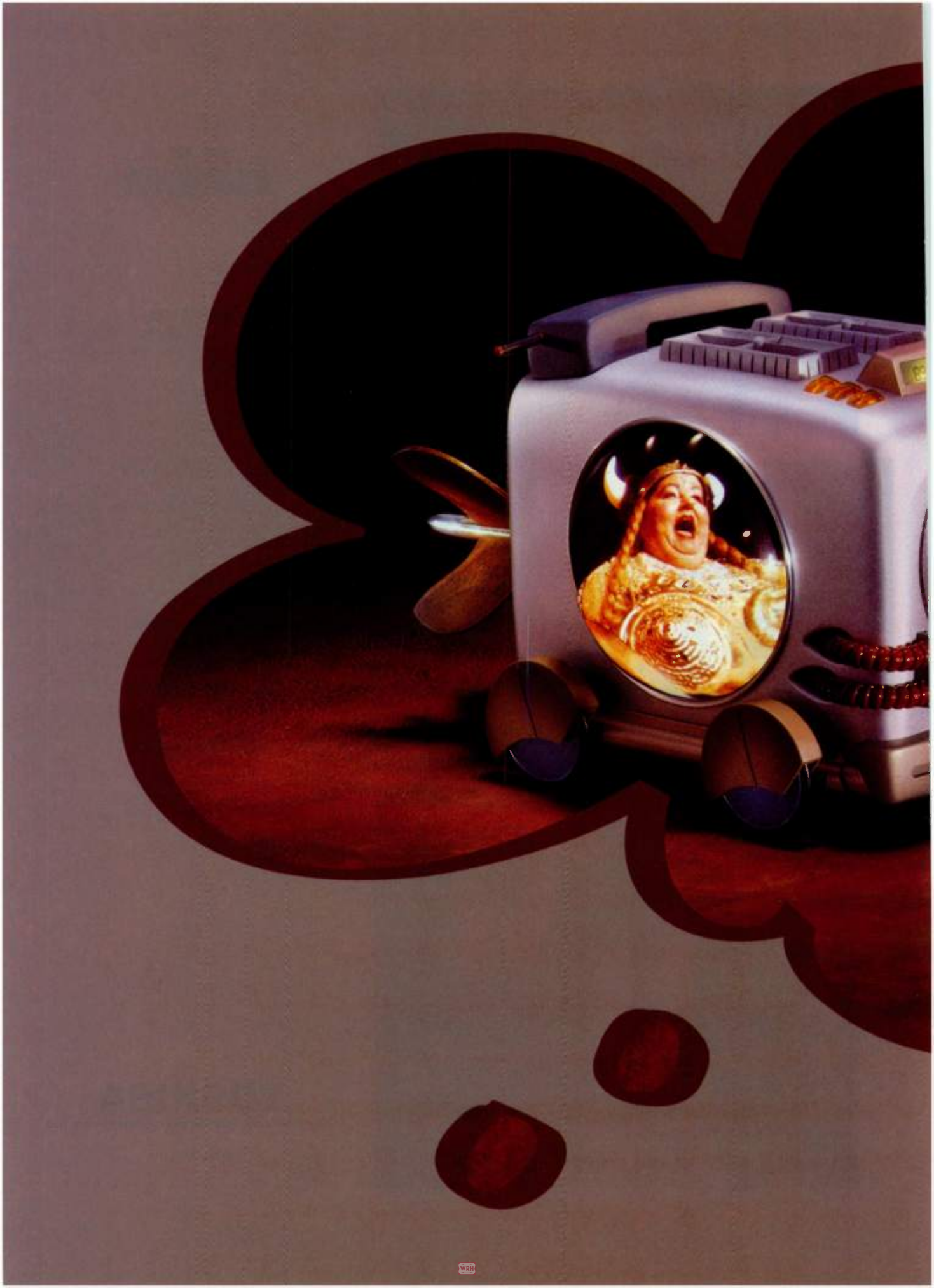

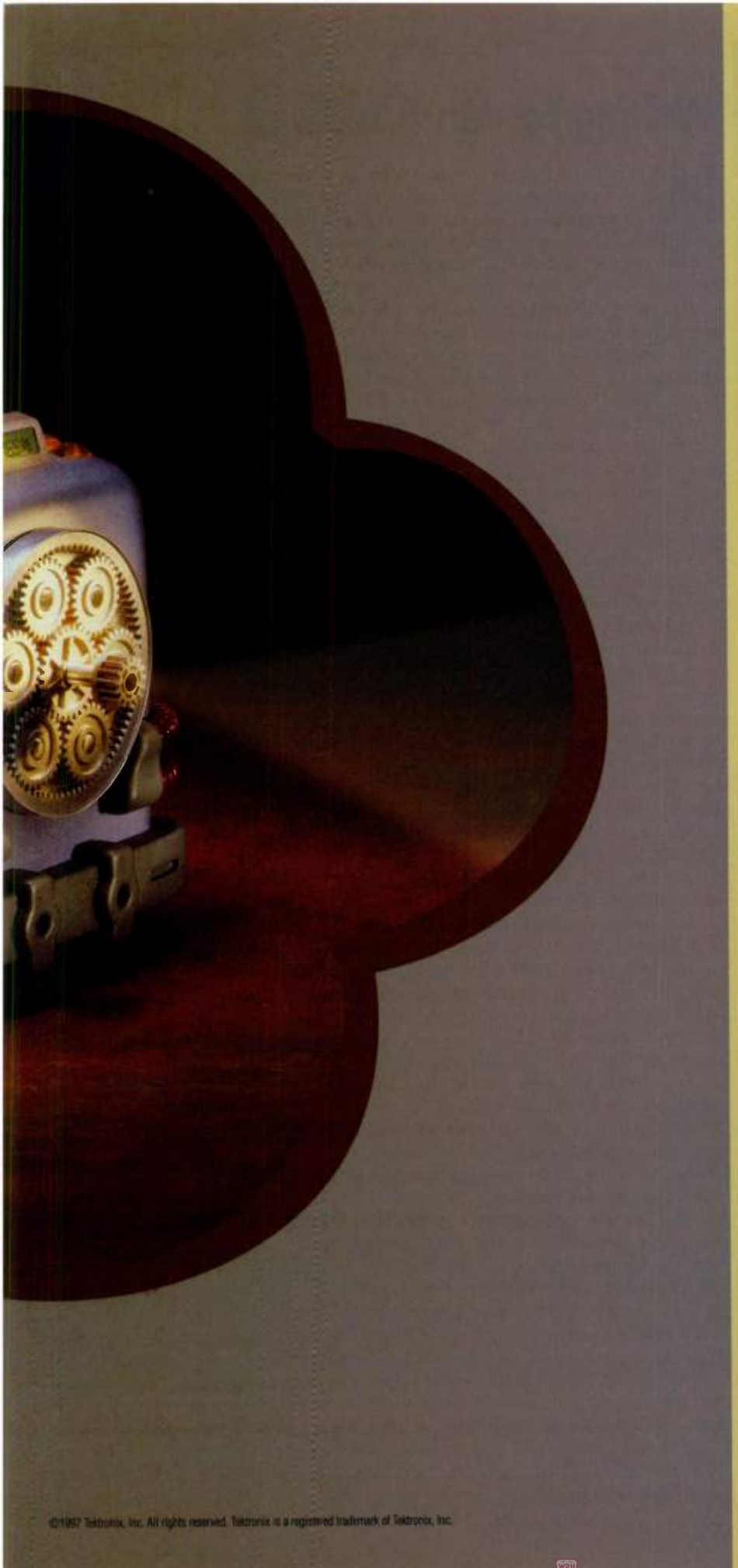

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Waiting For Mr. Goodbaud

My family and I finally moved into our new house. I also am quite thrilled to have a real home office in my new home. My old home office, which my wife and I shared, was basically a desk that was crammed next to our bed. To celebrate, I recently arranged to have a second phone line installed for my modem and fax machine. Unfortunately, our local telephone company has turned my bid to join the growing ranks of telecommuters into a comedy of errors.

Soon after moving in, I discovered that the installer had diligently hooked up my office line, but somehow managed to leave the two wires carrying our home phone line dangling somewhere up on the pole! Meanwhile, a recording on our old number was cheerfully forwarding friends, relatives, and telemarketers to that very same set of open wires.

After a week of chatting up various telco representatives and surviving two bungled installation attempts, our house now has a state-of-the-art communications system—circa 1962. If this is any indicator of the telco's ability to deploy technology, it's not surprising that their attempts to introduce ISDN have been a disaster. It also explains why their ADSL broadband data services are still shimmering on the event horizon, taunting us like a watery mirage in the desert. Too bad; residential broadband services will probably be one of the biggest growth industries in the early part of the next century.

LEE GOLDBERG
COMMUNICATIONS

There are many ways to deliver high-speed data to homes, including cable modems, wireless local loops (WLLs), and satellites, but there are many reasons why the telephone system's architecture is one of the few that stands a chance of being useful for anything more than home shopping. First, the telephone network is built on a switched model, not broadcast like cable, WLL, or satellite. Besides a broadcast system's obvious potential for security problems (would you like the entire neighborhood watching you download XXX .GIFs?), it forces you to take smaller and smaller slices of the network's bandwidth as subscribership increases.

Another nice thing about switched networks is that they tend to be bandwidth-symmetrical, or at least reasonably so. Even ADSL (in which the "A" stands for asymmetric) will give the average user between one-half and 4 megabits of dedicated upstream capacity. Contrast that with the skinny 100-kbit/s channel that the cable folks intend to let you share with a couple hundred of your neighbors and you begin to see what I mean. That's why I'm rooting for the phone system, and am offering them this bit of unsolicited advice.

Hey folks in the telephone industry! I don't mean to frighten you, but there is a growing horde of powerful, well-financed entrepreneurs (Gates, Malone, and Murdoch, to name a few) who are planning take away your business if you don't get your act together and roll-out broadband service in a big hurry. As unreliable as it may be, cable-modem service has arrived in many areas of the country while you guys are messing with another round of trials.

Broadband fever has even hit our local cable company—the same people who have given us such fare as the "all-Matlock channel," "the bass fishing network," and "the monster truck wrestling channel." To my surprise, they recently asked me if I wanted to have a cable modem installed. I'm thinking about asking them if I can get a cable modem without having to subscribe to their television service!

I'd hate to go over to the "dark side" and let one of those coax cables into my house again, but the chance to feed my hungry browser with multimegabits/s is very tempting. Sure, I still feel that cable-modem technology is at best, an inferior imitation of what an ADSL line could be, but I'd rather not wait until the next Ice Age to access the Internet at something approaching a useful speed.

So here's the deal. I'll wait six more months to see if there's even a hint of ADSL, VDSL, HDSL, RADSL, or anything remotely like it coming to my neighborhood. If not, I may have to do something rash. *leeg@class.org*

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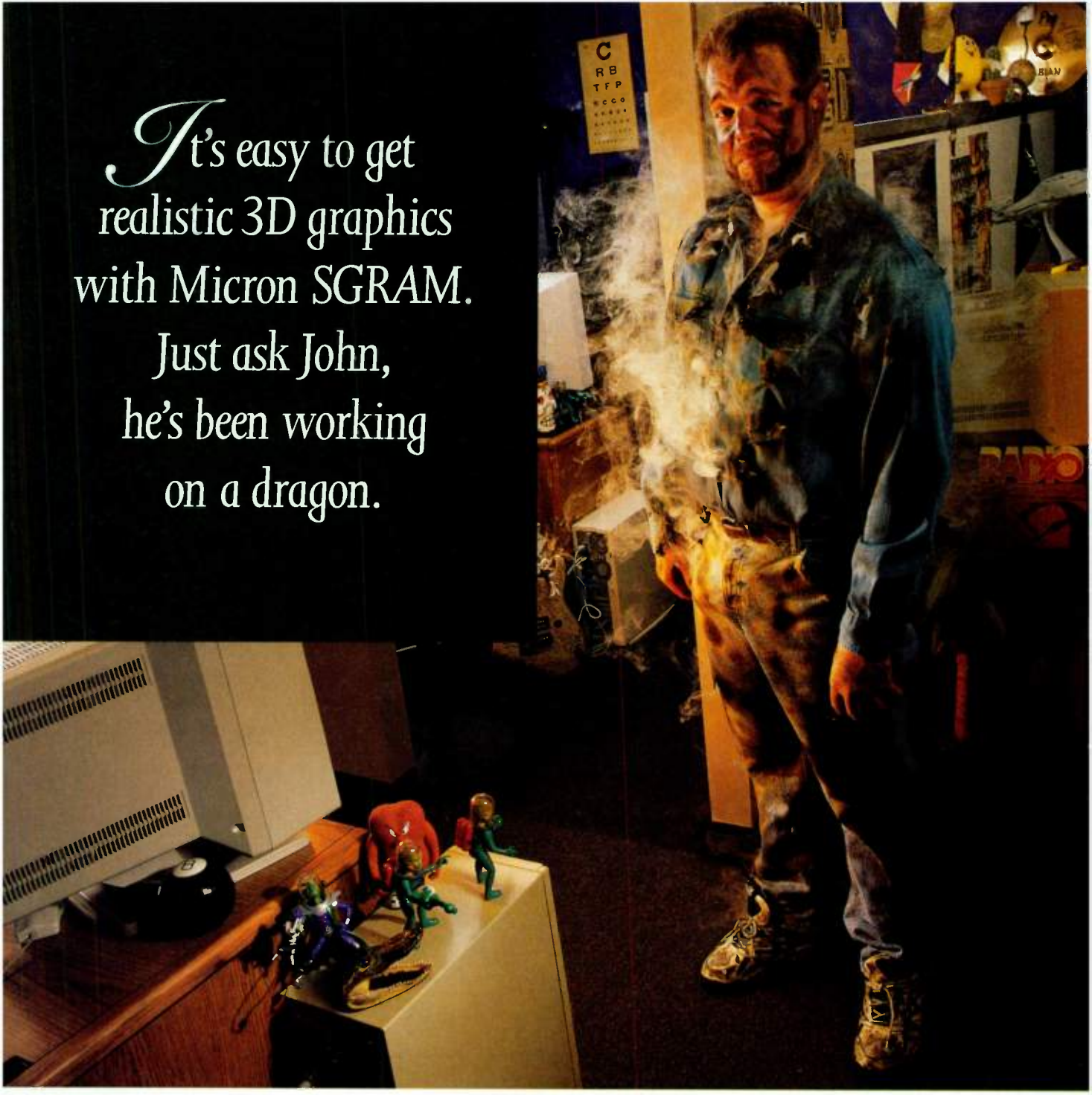

DENSITY	CONFIGURATION	VOLT	PACKAGE	CYCLE TIME
8Mb	256K x 32	3.3V	100-Pin TQFP	(125, 100, 83 MHz)
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As John can testify, our SGRAM breathes life into 3D graphics and advanced bandwidth applications. It boosts the performance of your system and does it in an industry-standard architecture that's easy to design in. But there's yet another reason John is a Micron graphics memory fan—it's our wizard of SGRAM, Gary Welch. Gary's one of those people who eats, sleeps and breathes graphics memory—and he loves to answer your questions. What's more, Gary is easy to reach. Just fire him an e-mail at gwelch@micron.com, or give him a call at 208-368-3900. For the whole story, or to see a data sheet, visit our Web site. www.micron.com/mti

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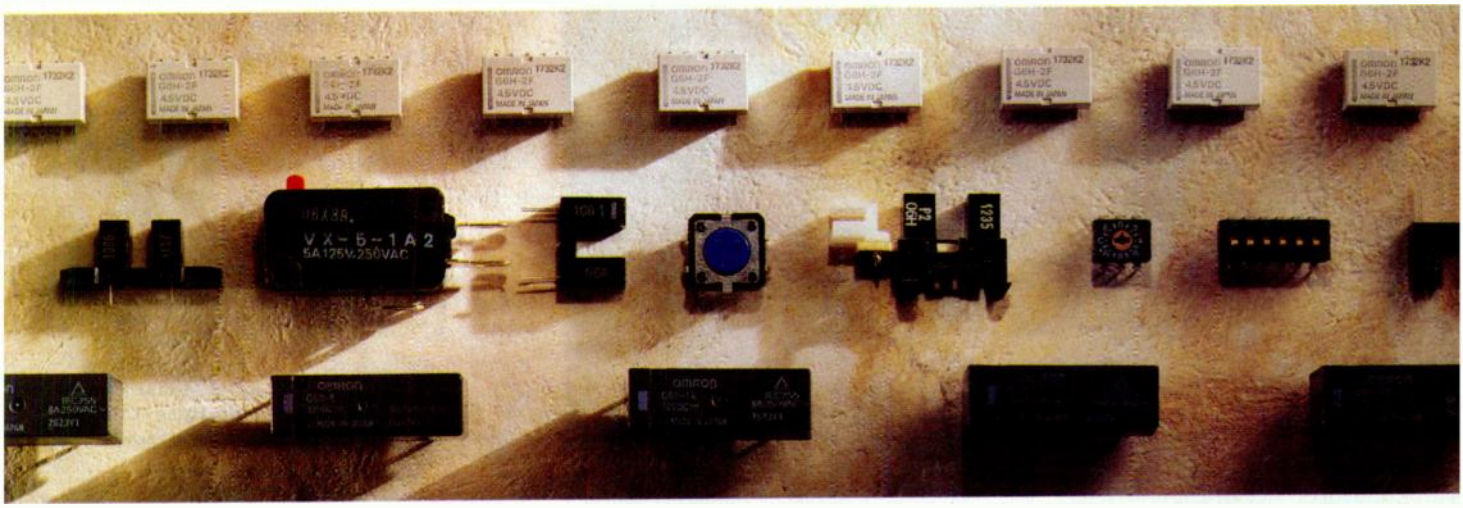
READER SERVICE 124

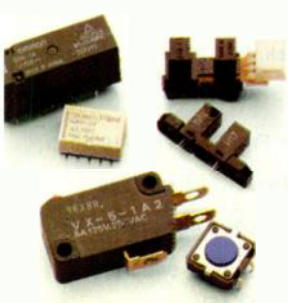
If You Think Omron Only Makes Relays, Read Between Our Lines.



It's true we're the world's number one relay supplier. So it's not surprising to learn that design engineers and specifiers know us for our relays.

But we also manufacture the world's most complete line of switches and photomicrosensors.

For years we've been building all types of switches, photomicrosensors, and relays for leading companies that manufacture telecommunications products, home and office electronics, computer peripherals, appliances, and HVAC equipment, just to name a few.



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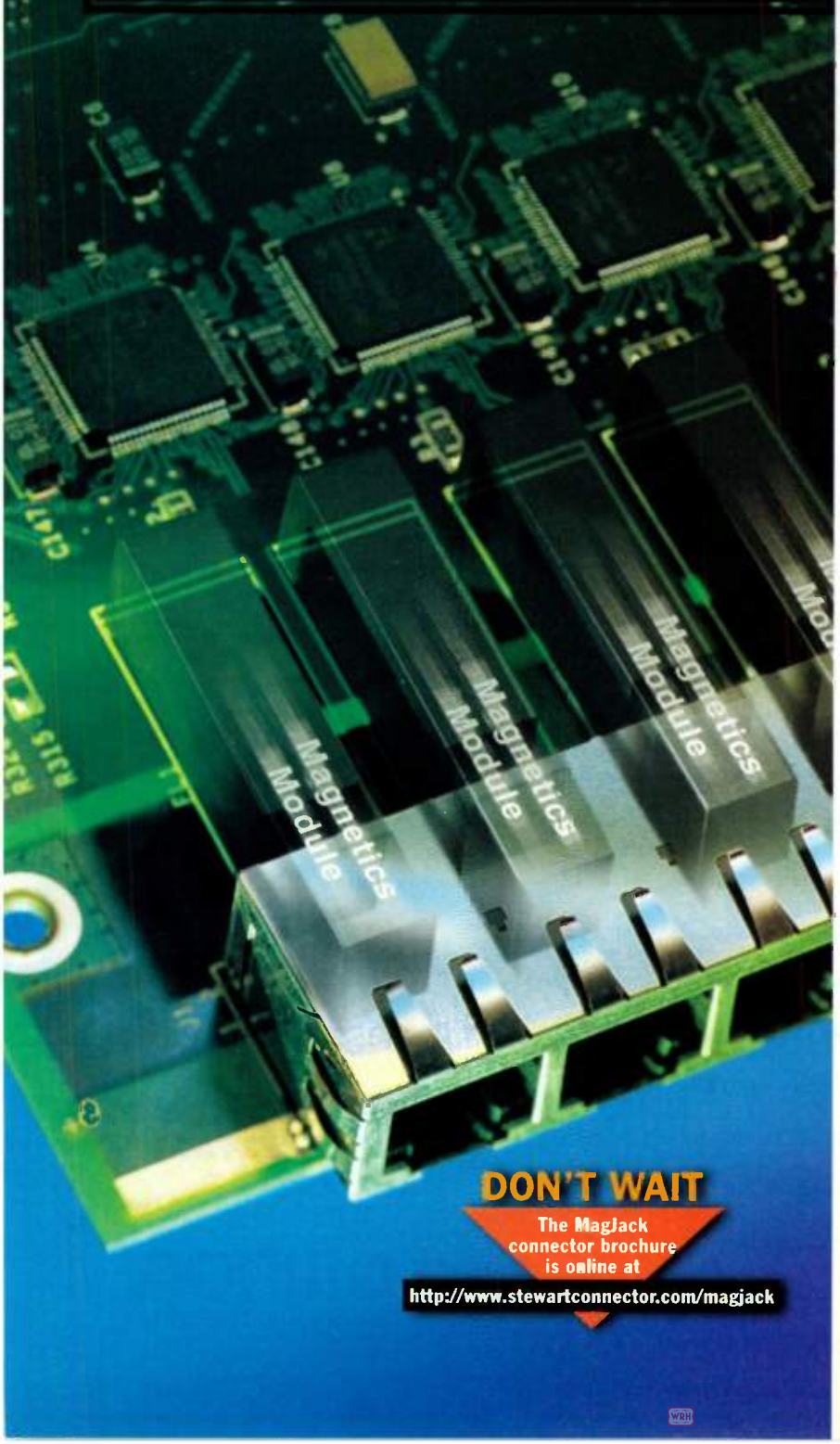

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MagJack integrates the isolation transformer and common mode filter into the shielded housing, minimizing signal degradation and conserving valuable board space.

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You need your space and MagJack delivers. By integrating the isolation transformer and common mode filtering in the housing, you eliminate the additional magnetics modules and gain valuable board space with every port. Whether you want to add components or shrink your design, MagJack offers flexibility unavailable in multiple-component solutions. The single-component design with industry-standard footprint lowers costs through fewer parts to buy, less inventory, and easier assembly to the board.

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READER SERVICE 151

Agreement Paves Way For New Wave Of Personal Telephony

A turning point in the deployment of new types of personal-communications satellite systems was achieved upon agreement among signatories of the Memorandum of Understanding on GMPCS (Global Mobile Personal Communications By Satellite). These new systems, known as Big, Little, and Mega LEO satellites, represent the immediate future of personal telephony. Such systems promise seamless global mobile fax, messaging, data, and even two-way voice and broadband multimedia connectivity via small, handheld phone sets, computer-mounted terminals, and laptops. Most are scheduled to come into operation within the next five years, and will be able to offer service to people worldwide.

The arrangements agreed upon cover four main areas: the mutual recognition of type approvals of GMPCS terminals; a simplified regime for the licensing of these terminals; a method of identifying (marking) the terminals; and access to traffic data by authorized national authorities. A recommendation on the principles for customs procedures to facilitate unrestricted transborder movement of GMPCS terminals also is included.

To ease regional, global, and transborder roaming, national authorities are invited to mutually recognize type approval and marking procedures for GMPCS terminals. They're also invited to continue to strive for a single procedure for type approval, as well as to exempt GMPCS terminals from the requirement of individual licenses when the essential criteria given in the arrangements are met. GMPCS terminals that are issued type approval pursuant to the arrangements will be marked with "GMPCS MoU." It will indicate the name of the GMPCS system for which the use of the given GMPCS terminals has been authorized.

Also agreed on was that GMPCS system operators or service providers will supply, upon request, to the national authorities implementing these arrangements, GMPCS traffic data originating in or routed to its national territory. This will exclude any confidential customer information.

Finally, the arrangements call upon countries to reduce duties on GMPCS terminals placed on the market, as well as exempt from customs-related restrictions and fees GMPCS terminals used when visiting or traveling through countries on a temporary basis. In this respect, work will be undertaken with national authorities and international custom bodies to ensure that GMPCS terminals are considered as a traveler's personal effects.

The final text of the arrangements is to be approved at the next meeting of signatories and potential signatories to be held October 6 and 7. As the depository of these arrangements, the International Telecommunication Union (ITU) will maintain a list of standards and specs. For more information, contact the ITU, Geneva, Switzerland; phone: +41 22 730 51 11; fax: +41 22 733 7256; *itumail@itu.ch*; *http://www.itu.int/newsroom*. RE

Display's Mini Neck Improves Resolution, Lowers Power

Improved resolution and a lower power consumption come as the result of a miniature neck employed on a color display tube unveiled by Samsung Display Devices, Seoul, Korea. The 15-in. tube reduces the thickness of electron beams by 10 to 30% to improve the sharpness of the characters displayed on the screen. One of the main differences in the new models is the use of an electron gun. While conventional displays use a non-dynamic gun, the mini-neck displays will take advantage of a single dynamic gun. The dynamic electron gun also improves the sharpness at the edges of the screen. In addition, while conventional displays consume about 75 to 80 W, the new mini-neck design consumes about 65 W. Samsung plans to start shipping the mini-neck displays later this year, eventually replacing its existing line of displays. For more information, contact Samsung at (822) 727-3597, or on the Internet at *http://www.sdd.samsung.co.kr*. RN

Protocol Lets E-CAD Users And Vendors Talk

Steps are being taken on an international scale to evaluate the feasibility, impact, and advantages of exchanging electrical information with STEP AP212. AP212, developed jointly by ProSTEP and Siemens, is an exchange format or data scheme that provides the means for E-CAD users to talk to E-CAD vendors systems. The project, referred to as E1, was launched at the beginning of the year and involves a number of users and vendors of E-CAD systems. Some of the companies involved include DASA, Debis, Delphi, Ford, Mentor Graphics, Harness Software, ProSTEP, and Siemens.

The main thrust of the project is to develop the first series of processors for physical file exchange that implement the AP212 protocol. Results of this work are expected to also include a definition of the functionality of the processors according to the most urgent user requirements, implementation of AP212 technology in industrial practice, demonstration of the productive data exchange using AP212 processors, verification that AP212 fits the user requirements, and recommendations for further improvement of AP212. It's anticipated that these results will be ready for presentation at the 1998 Cebit fair.

Running parallel to the E1 project is the Application Protocol "Electrotechnical Design and Installation" AP212 standardization effort. This protocol, which represents the properties of electrical and related equipment, is being standardized as 10303-212. Up to now, electrical-industry exchange formats typically only allowed the exchange of graphical information in the form

of drawings. AP212 supports the complete functional logic of electrical and related products, including all of the associated technical and non-technical data.

More specifically, AP212 represents the following type of information: general description of products and their structure; connections and nets; descriptions of functions; installation cables, wiring, and routing diagrams; identification of tools, connections, and signals; assignment of attributes, properties, and explanations; documentation and graphical representation; and version and configuration management. Thus., it's expected to provide both manufacturers and industry suppliers with important strategic advantages when used as the basis for information systems within a company

For further information on the AP212 standardization effort or the E1 project, contact either Dr. Martin Holland, ProSTEP, at phone: +49 6151 9287 17; e-mail: *holland@prostep.de*; or Mentor Graphics at 1 (800) 547-3000; Web: *http://www.mentorg.com/groups/cabling*. CA

Wheels Set In Motion For RTL Standard Infrastructure

One of the top ten projects on the EDA Industry Council's, San Jose, Calif., list of priorities involves synthesis interoperability. By realizing such interoperability, synthesis-based designers can produce well-defined designs with functional characteristics independent of a particular synthesis implementation. A project to address this need, known as the Synthesis Interoperability project, is currently underway. It's a joint effort on the part of VHDL International, Santa Clara, Calif., and Open Verilog International (OVI), Los Gatos, Calif.

To accomplish the goal of true interoperability, however, an infrastructure for a common semantic meaning for the RTL (Register Transfer Level) level of abstraction must first be in place. With the recent approval of the VHDL RTL Synthesis Standard Project Authorization Request (PAR) by the IEEE New Standards Committee (NESCOM), the path to that infrastructure is finally becoming clear.

The VHDL RTL Synthesis standard is based on the existing 1076, 1164, and 1076.3 IEEE standards. Its PAR will serve as a standard syntax and semantics for VHDL RTL synthesis. More specifically, it will define the subset of the IEEE 1076 standard that's suitable for RTL synthesis and semantics for the synthesis domain. The ultimate goal is to define a syntax and semantics used by all compliant RTL synthesis tools to achieve uniform results similar to simulation tools that use the 1076 standard.

In a related development, a strawman proposal for standardizing the VHDL RTL subset suitable for logic synthesis was developed under the guidance of VI (VHDL International), Open Verilog International (OVI) and the Industry Council Project Technical Advisory Board (IC PTAB) earlier this year. The proposed standard is now headed toward formal IEEE standardization under the sponsorship of the Design Automation Standards Committee (DASC). It is part of the Synthesis Interoperability project that also includes work in the areas of constraints, directives and libraries for logic synthesis. A formal standard based on this work is expected to be available by the end of 1998.

For additional information on this standard or related efforts, check out the VIUF Fall 1997 Conference, Washington D.C., October 19-23, 1997. Call (415) 329-0578, or contact Mahendra Jain of VHDL International, Santa Clara, Calif., at (408) 492-9806; e-mail: *jainm@vhdl.org*. The VHDL International's web site address is: *http://www.vhdl.org/vhdl_intl*. CA

Component Waveform Data Format Standard Sought

Simplifying the process of obtaining and analyzing component timing-diagram information has become of paramount concern for many engineers. To that end, CFI Inc., Austin, Texas, and members of its Electronic Component Information Exchange (ECIX) project have begun to develop a standard format for component waveform data representation. Members involved in the effort include Hewlett-Packard, Hitachi, IBM Microelectronics, Intel, National Semiconductor, Philips Semiconductors, and Texas Instruments.

At its core, the group hopes to provide a seamless flow of component information in both computer and human sensible formats from suppliers to customers by utilizing the latest media distribution technologies. Once in place, this standard data format would allow engineers to use any browser currently available with the guarantee that all of the data coming from the information suppliers would be in one format. The benefit is that because the engineer could download timing-diagram information with a standard web browser, which could then be viewed and analyzed inside a timing-diagram helper application, a component's timing could effectively be considered in the context of a custom design and/or translated to other waveform formats, such as Verilog, VHDL, or Spice as simulation test stimulus.

CFI is now soliciting existing representation formats for waveform data through its Request for Technology (RFT) process. Once in-house, CFI and an industry panel will review all of the submissions and decide on the most appropriate selection. A technical working group will then work on developing any necessary extensions. The final standard proposal will be submitted to a formal standards body when complete. For information regarding the submission process, contact John Teets, program manager CFI, at (512) 342 2244, ext. 57, or check out CFI's web page at *http://www.cfi.org*. CA

Edited by Roger Engelke

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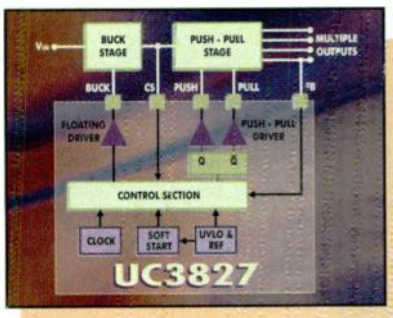

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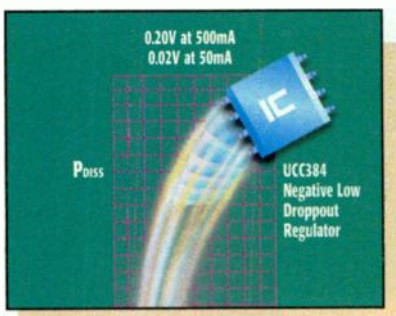
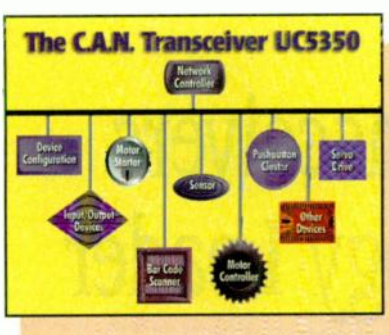
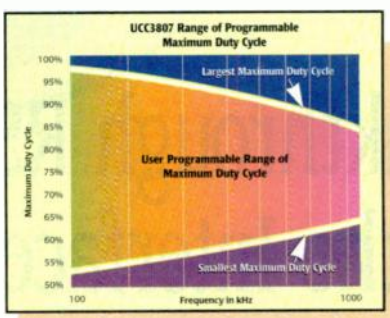
This flexible cascaded buck/push-pull PWM controller is ideal for multiple output and/or high voltage, and high power output applications. The need for additional components and complex circuitry is eliminated.



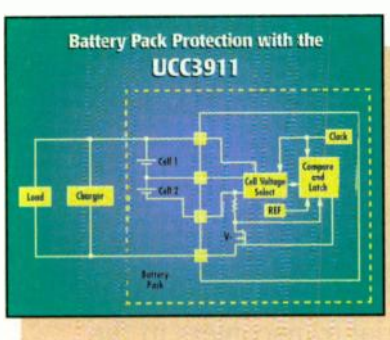
UCC384
This BiCMOS 0.5A negative voltage (to -15V) low dropout linear regulator with pulsed short circuit power limit provides less than 225µA quiescent current consumption allowing for high efficiency power conversion.



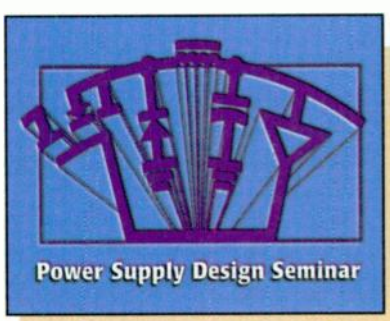
UC5350
Factory network automation is redefined with Unitrode's UC5350 Control Area Network (C.A.N.) transceiver. This plug-&-play network solution saves money, shortens design time, increases production reliability and reduces downtime.



UCC3807
This BiCMOS PWM controller allows the user to program the maximum duty cycle. The UCC3807 optimizes magnetics, reduces transformer primary and switch current, decreases power losses, increases efficiency and improves reliability.



UCC3911
This two-cell lithium-ion battery pack protector IC incorporates an on-chip series FET switch reducing manufacturing costs and increasing reliability. The UCC3911 safeguards battery cells against output short circuits and over/under voltage conditions.



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Receivers	1	1	1	1	0	0	4	4	1	1	4
Data Rate (Mbps)	5	0.25	5	5	10	10	10	10	5	5	10
Half/Full Duplex	Half	Half	Half	Half	N/A	N/A	N/A	N/A	Full	Full	Full
Features	Low Power Shutdown	Slew Rate Limited	Industry Standard Pin Out	Up to 256 Transceivers on Data Bus	Common Tri-State Enables	Separate Tri-State Enables	Common Tri-State Enables	Separate Tri-State Enables	Industry Standard Pin Out	Driver/ Receiver Enable	Pin Out for SCSI Interface

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READER SERVICE 149

Ultra-Wideband Optical Amplifier Technology May Increase Fiber Network Capacities Tenfold

Thanks to a recent development in optical amplifiers, fiber-optic networks may gain nearly an order of magnitude in data-carrying capacity. Researchers at Lucent Technologies, Holmdel, N.J., have demonstrated a record-breaking experimental ultra-wideband optical-fiber amplifier that can boost lightwave signals carried simultaneously over 100 or more channels, or wavelengths, of light.

With a bandwidth that spans 80 nm of light, the amplifier has almost seven times the optical capacity of amplifiers used in commercial wavelength-division multiplexed (WDM) communications systems. WDM allows the transmission of multiple channels of digital information channels on a single optical fiber, using several different discrete bands within the optical spectrum.

While it is revolutionary in its capabilities, the amplifier uses many of the basic principles now at work in commercial optical amplifiers. It consists of coils of optical fiber doped with erbium and other elements. The fiber coils are "pumped" with energy, using an external out-of-band light source (typically 980 nm), and incoming photons from the optical communications channels stimulate the fiber to emit photons at their respective channel wavelengths.

Thanks to their reliability, performance, and simplicity, erbium-doped optical amplifiers (EDFAs) are gaining acceptance for critical communications applications, such as repeaters in long-haul optical networks. One of the first applications was in submarine cables, which must run as long as twenty years without service.As their cost drops and performance improves, optical amplifiers are rapidly gaining acceptance in other sectors of the communications market. Of course, no emerging technology is without its share of growing pains, and optical amplifiers are proving to be no exception.

Perhaps EDFAs' most significant limitation is the physics of optical amplification. The principles used in today's amplifiers only permit them to have good efficiency and relatively uniform amplification characteristics across a relatively narrow bandwidth, typically 12 to 20 nm, and perhaps up to 40 nm, with extensive gain equalization. Erbium-doped tellurite fibers and other exotic materials are now being investigated to see if they can yield better wideband performance in amplifiers, but commercially useful products appear to be many years away.

To solve this problem, the Bell Labs team developed an amplifier that uses existing technologies and materials in a unique way. Their device has a split-band architecture, with two parallel amplification paths, each of which has characteristics optimized for a particular part in the erbium-gain spectrum. The demonstrated amplifier is a two-stage unit that has loops of commercially available silica fiber doped with erbium and aluminum.

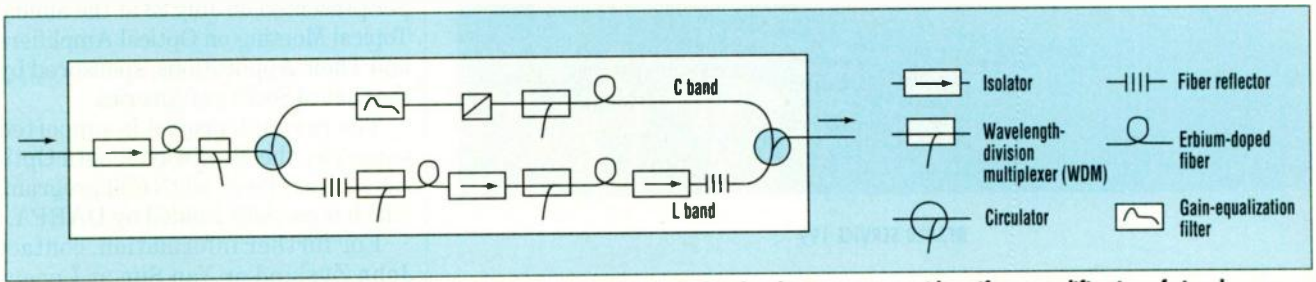
In the first stage, all wavelengths share a common amplifier *(see the figure)*. Upon exiting that stage the traffic is split into two bands using a broadband grating and an optical circulator. C-band (1526-to-1563 nm) and L-band (1569-to-1613 nm) traffic then undergo second-stage amplification in higher-gain stages whose characteristics are optimized for that particular frequency band. This allows each second stage amplifier to have different lengths of fiber, pump input levels, and input signal levels, all techniques used to equalize the fiber's amplification response at different wavelengths. A second grating and circulator is used to recombine the two bands into a single output fiber prior to exiting the amplifier.

The optical stimulus pump power for each stage is 20 dBm (25 dBm for the second loop of the L-band section). Bandwidth demonstrated by the experimental amplifier is three times that of erbium-doped fluoride amplifiers, twice that of recently described Bell Labs experimental erbium-doped silica fiber amplifiers, and 50% higher than has been reported for other experimental dual-band amplifiers.

Networks using the new amplifier could handle 100 or more optical channels, spaced at 100 GHz, instead of the eight or 16 in today's systems. By employing a technique known as wavelength division multiplexing, (WDM) these 100 channels could share the same fiber connection between network nodes, and then be directed towards the next point in their journey using all-optical switches.

Besides greatly increasing a network's capacity, the use of all-optical amplification and switching systems eliminates the need for electro-optic conversion, one of the greatest contributors to signal degradation. Until recently, optical signals had to be amplified and switched using conventional electronic circuitry, necessitating their conversion from photons to electrons and back again.

The nonlinearities in the detectors, emitters, and their associated circuitry used in this dual-conversion process in-



Bell Labs' experimental wideband optical amplifier employs a two-stage, split-band architecture to provide uniform amplification of signals across an 80-nm frequency range. After a first stage of amplification, the signal is split into two bands using a circulator. The C-band signal (1526-to-1563 nm) is equalized and sent through a single gain stage. The L-band portion of the transmission undergoes two additional stages of amplification before being recombined with the C-band signal at the amplifier output.

troduced phase and amplitude distortion, along with the inevitable quantum noise associated with electronic devices. With the advent of all-optical amplifiers and WDM optical switching techniques, fiber networks will enjoy longer distances between signal regeneration nodes. They will also probably find ways to use the lower noise floor to squeeze more data into a single channel.

This experiment is the first step towards creating commercially available devices that will enable Internet service providers, networked data services, and other communications industries to keep ahead of the public's demand for bandwidth that's growing at near-exponential rates. According to Lucent officials, this new amplifier technology will affect the architecture of optical networks by allowing the same piece of fiber to carry many more channels.

Another advantage of using ultrawideband networks is that it will permit carriers to use wider frequency gaps between channels. The greater separation helps reduce the effects of interactions that can spill into adjacent channels. Wider channel separation also allows network-termination equipment to employ simpler filtering to sort out multiple data channels, even with the distortions introduced into the signals during long-distance fiber runs.

The ultra-broadband optical amplifier was designed and demonstrated by Yan Sun, Atul K. Srivastava, James W. Sulhoff, Chuck Wolf and group leader John L. Zyskind, of Bell Labs, Crawford Hill, N.J. The team also worked with Jianhui Zhou, of Lucent's Optical Networking/SONET Business Unit, and Thomas A. Strasser, J. R. Pedrazzani, Justin B. Judkins, Rolando P. Espindola, and Ashish M. Vengsarka, of Bell Labs, Murray Hill, N.J. The Bell Labs research team reported its results in a paper presented on July 23 at the annual Topical Meeting on Optical Amplifiers and Their Applications, sponsored by the Optical Society of America.

The research project is supported in part by the Multiwavelength Optical NETworking (MONET) program, which is partially funded by DARPA.

For further information, contact John Zyskind or Yan Sun at Lucent Technologies Bell Laboratories, P.O. Box 400, 791 Holmdel-Keyport Rd., Holmdel, NJ 07735; (908) 588-7000.

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20V8	7	10,15,25	10,15,25			
22V10	5,7	10,15,25	15,20,25	12,15	10,15	25

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Personal Biotelemetry Will Assess Soldiers' Wounds In The Battlefield Of The Future

Sometime in the relatively near future, you may be able to don a lightweight undergarment which monitors your heartbeat, respiration, metabolism, body movements, and a variety of other critical bio-telemetry factors. Intended for use in battlefield and other hazardous conditions, it will automatically detect critical injuries and pass on data that will alert medics to the type of wound you have received, its severity, and parts of the body that have been damaged. While this may sound like science fiction, the technology for non-invasive biotelemetry is being developed under a joint project funded in part by the Defense Logistics Agency, DARPA, and NRAD, the U.S. Navy's R&D arm.

Known as the "Sensate Liners Project For Combat Casualty Care," the initial research is to quickly identify and locate downed soldiers and determine the severity of their wounds. The researchers hope that performing electronically-assisted "remote triage" will enable medics to locate and treat the most severely wounded casualties first. The program's goal is to significantly reduce the high percentage (around 65%) of soldiers who survive an initial bullet wound, but bleed to death before they receive medical attention.

The undergarment in development will detect when a soldier has received a penetrating wound on the battlefield, and relay enough information back to a central control point to allow a remote diagnosis and health assessment to be performed. As a by-product of this research, it has become apparent that many physiological factors can be monitored in the same way, making the technology potentially useful for many civilian applications. The most obvious potential beneficiaries of such a spin-off are those who work in hazardous occupations like fire fighters, deep divers, and police officers. Additionally, applications in everyday medicine will probably arise as the technology matures and manufacturing costs decline.

The original concept for the liner is to have a sensor array woven into and embroidered onto an inexpensive "smart fabric" that has an embedded matrix of conductive polymer fibers and fiber optic strands. In its primary use on the battlefield, the garment's small signal-processing unit is activated only when struck sharply or punctured.

Once activated, it will use the garments sensors to collect acoustic and electrical signals generated as the projectile penetrates the body. The signal-processing unit will collect data from the undergarment and determine if the impact was sufficient to cause serious injury. Then, it will pass the data on to a soldier's personal information device (PID), a small, body-mounted 486-class computer. From there, the PID will compress and transmit the data back to headquarters, where further analysis

can identify the projectile and its trajectory, as well as assess the wound and other tissue damage. The PID also will transmit the fallen-soldier's location, thanks to a built-in GPS system.

Three contracts are underway to develop different portions of the technology. The Georgia Institute of Technology, Atlanta, is to develop and weave conductive fibers that will act as a sensor matrix into the liner's fabric. ILC Dover, Dover, Del., the manufacturer of most U.S. spacesuits, will fabricate the undergarment and embroider a break-wire system onto it that will detect a puncture wound. The third contract, undertaken by Mission Research, Fountain Valley, Calif., commissions the firm to develop the sensors and signal-processing algorithms that will actually locate the impact area, assess the projectile's trajectory through it, and calculate the level of injury the soldier sustained.

Many sensors were evaluated by Mission Research, both active and passive, and two were selected for their ruggedness, low cost, and ease of integration. The first is an impact detector which will activate the system only when it determines that an impact or penetration significant enough to cause serious injury has occurred.

After triggering, the system will collect around 2 μs worth of data from an array of data-collection sensors spread across the suit. Each of the 10 data-collection patches is a small cluster of piezeo-electric sensors which can be used as a phased-array element. Signals from these sensors contain real-time signatures of the direction, speed, and size of the projectile, as well as the type of materials it impacts. When combined with information about its entry point, spectral analysis and acoustic ranging will allow the processor to determine the type of projectile, its velocity, and trajectory. This will allow expert system f software to make a detailed assessment of where the fragment has landed and how much damage has done .

Aside from the grisly aspects of this technology, many interesting by-products have arisen which may be useful in peacetime. For example, much of this technology can be integrated into bullet-proof vests and body armor for law-enforcement people. Also, initial research shows that the conductive threads and optical fibers may make excellent transducers, capable of monitoring large and microscopic displacements.

Between monitoring changes in bulk resistivity and other transmission characteristics, it is possible to extract signals that report precise changes in chest volume, limb displacement, and other movements. From this, respiration and even heartbeat can be extracted. Using the fiber's trebo-microphonic characteristics may enable engineers to actually monitor heart sounds and blood flow in various parts of a person's body. Future contracts may include research into even more sophisticated biotelemetry sensor techniques.

Contact Bob Eisler at Mission Research Corp., 17150 New Hope St., Suite 516, Fountain Valley, CA 92708-4253; (714) 754-1300. Or contact Dr. Eric Lind, NRAD's Program Manager, at NCCOSC RDTE, Code D364, San Diego CA 92152-6320; (619) 553-2671.

Lee Goldberg

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But the DS2152 then goes on to add features to increase flexibility with two goals in mind. First, it incorporates more functions in the hardware, eliminating the expense and time required for firmware or external hardware development. Second, the new chip reduces processor real-time servicing. One processor can now service multiple channels, reducing board space consumed and costs for additional chips.

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READER SERVICE 176

Sub-5-V Voltage Reference Mimics The Performance Of Buried Zeners

JFET-Based Precision IC Reference Operates At 2.7 To 15 V, Yet Offers Effective Temperature Stability And Low Noise.

Frank Goodenough

References of some kind are mandatory for all measurements, no matter how simple or accurate they must be. For instance, many types of weighing scales use calibrated springs. Today, voltage references remain the unsung heroes of the IC industry. However, as supply voltages continue to decrease, "good" ones get harder and harder to obtain—read more expensive—and they often provide limited performance in the form of significant noise on the output signal or a poor temperature coefficient. Basically, they make good temperature sensors and, with a few circuit modifications, are often marketed just for that purpose.

COVER FEATURE

As power-supply rails move closer to zero in voltage, system and IC designers need high-performance voltage references that can operate off power-supply rails below that of the buried Zener-diode's 6 V. Ideally, such a device must combine low-power operation with low-noise and low-drift performance. It must also offer a linear temperature coefficient.

On the other hand, the best IC references currently available on the market, buried Zener diodes, need a power supply rail of at least 6 V for operation. They also need a current of at least 1 mA to keep the noise down to a practical level.

Moreover, practical bandgap references that can run off voltages below 5 V are not noted for low-noise performance. They exhibit considerable temperature hysteresis, and their long-term stability is dependent (among other things) on the absolute value of at least one on-chip resistor.

Meeting The Need

Therefore, to meet industry and designer needs, designers at Analog Devices, Santa Clara, Calif., set out to create this much-desired IC reference. They came up with a new reference architecture for which they have applied for a patent.

The reference voltage in the new architecture is based on the difference in the pinch-off voltage between two junction FETs (JFETs), Q1 and Q2 *(see the figure)*. JFETs Q1 and Q2 are not just two plain-vanilla devices—JFET Q2 receives an additional channel implant step during its fabrication process.

The reference's designers dubbed the new device the XFET (eXtra implanted FET). The ADR229x series are the first of a large family of references based on the new architecture. They operate off supply rails between 2.7 and 15 V from which they draw just 12 µA. The ADR290 puts out 2.048 V; the ADR291 puts out 2.500 V; and the ADR292 puts out 4.096 V.

To be sure, the bandgap-type reference has been around for over 30 years. During that time, it has become a high-performance device. Many organizations (both corporate and academic) have dedicated a great deal of design effort in optimizing the circuit, particularly for devices that will work off 5 V or lower. However, these references still lack the preci-

sion demanded by many of today's electronic systems.

No Axe To Grind

Analog Devices designs and markets IC voltage references, both bandgap and buried Zener types, so the XFET can be compared with several available bandgap references without treading on the toes of the competition, while attempting to demonstrate their claim of its superiority over a bandgap-type reference *(see the table)*.

The XFET circuit displays three major advantages over most bandgap and Zener references. Peak-to-peak noise voltage from a bandgap reference, in the frequency band between 0.1 and 10 Hz, typically runs more than 5x that for the XFET when operating at the same current. Alternatively, a bandgap reference must run at more than 100x the supply current required by the XFET to provide an equivalent peak-to-peak noise. In addition, the XFET sports a very flat and linear temperature coefficient over the military temperature range.

On the other hand, the best bandgap and Zener references typically have nonlinear temperature coefficients at the temperature extremes. These nonlinearities are different from one IC to another, so a simple ROM/software lookup table cannot be used to perform temperature-coefficient correction. A linear temperature coefficient is vital for DVM applications. Long-term stability represents the third major advantage of the XFET. It runs about 50 times better than that of either a bandgap or a Zener reference.

The XFET offers a system designer the following advantages:

- Lower noise than either a bandgap or a Zener reference running at the same current.
- Lower operating current than a bandgap or a Zener reference at a specified level of noise riding on the dc output.
- A flat temperature coefficient over the military temperature range.
- Long-term stability that's 50 times better than that of a bandgap or Zener reference.
- Thermal hysteresis one-fifth that of a comparable bandgap reference.
- An output capacitor is not required for stability.

Despite their low quiescent current (12 µA), these XFETs can deliver 5 mA to a load from a low-dropout pnp output stage.

Despite their low quiescent current (12 µA), these XFETs can deliver 5 mA to a load from a low-dropout pnp-transistor output stage. Broadband noise runs 460 nV/$\sqrt{\text{Hz}}$. Preproduction devices exhibit a thermal hysteresis ranging from 100 to 200 µV recoverable and noncumulative drift when subjected to a thermal shock of 100 Kelvins. A similar bandgap reference would show a shift of over 500 µV.

How It Works

As noted earlier, the core of the XFET consists of two JFETs, Q1 and Q2 *(see the figure, again)*. JFET Q2 was given an extra channel implant. By running both JFETs at the same drain current, the difference in pinch-off voltage (V_p) is amplified to form a highly stable voltage reference. This difference is about 500 mV and its negative temperature coefficient runs 120 ppm/K. Its slope is essentially locked to the dielectric constant of silicon and is accurately compensated for by adding a correction term generated in the same fashion as that of the proportional-to-temperature (PTAT) term used to compensate bandgap references. However, the intrinsic temperature coefficient is one-thirtieth that of a bandgap. As a result, much less cor-

A COMPARISON OF VARIOUS ANALOG DEVICES IC REFERENCES

Parameter	ADR291[A]	REF192	AD1582	AD586[B]
Reference topology	Series XFET	Series bandgap	Series bandgap	Buried Zener
Precision voltage options, V	2500	2500	2500	5000
Initial accuracy @25°C, mV maximum	±2/±3/±6	±2/±5/±10	±2/NA/±20	±2/±5/±20
Temperature coefficient, ppm/°C maximum	8/15/25 (-25 to +85°C)	5/10/25	50/NA/100	2/15/25
Line regulation @25°C, ppm/V maximum	100/100/125	4/8/8	25/NA/25	100/100/100
Load regulation @25°C, ppm/A maximum	100/100/150	4/8/8	200/NA/200	100/100/100
Load current @25°C, mA maximum	5	30	±5	±10
Noise voltage over 0.1-10 Hz, µV p-p typical	8	25	70	4
Wideband noise @1 kHz, nV/$\sqrt{\text{Hz}}$, typical	480	---	500	100
Maximum input voltage @I = 0 mA, V	15	18	12	36
Maximum supply current @I = 0 mA, µA	12	45	65	3000
Mamximum shutdown current, µA	NA	15	NA	NA
Long-term drift, ppm/1000 hours typical	0.2	20	100	15
Temperature range, °C	-40 to +125	-40 to +85	-40 to +85	-40 to +85
Package	TO-92, SO, TSSOP	DIP, SO, TSSOP	SOT-23	SO-8
Price, top/2nd/3rd grades	$7.50/$3.50/$2.25 (100-piece lots) $6.06/$2.95/$1.95 (1000-piece lots)	$7.50/$3.60/$2.20 (100-piece lots) $6.60/$3.17/$1.91 (1000-piece lots)	$1.25/NA/$0.85 (100-piece lots) $0.75/NA/$1.05 (1000-piece lots)	$6.83/$4.90/$2.95 (100-piece lots) $5.78/$4.20/$2.50 (1000-piece lots)

Notes: NA = not available; A = 3-pin package; B = has V_{out} adjust pin; 2nd and third grades are available in plastic packages.

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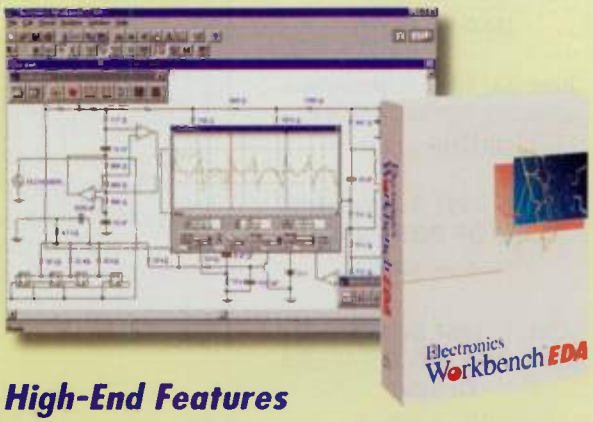

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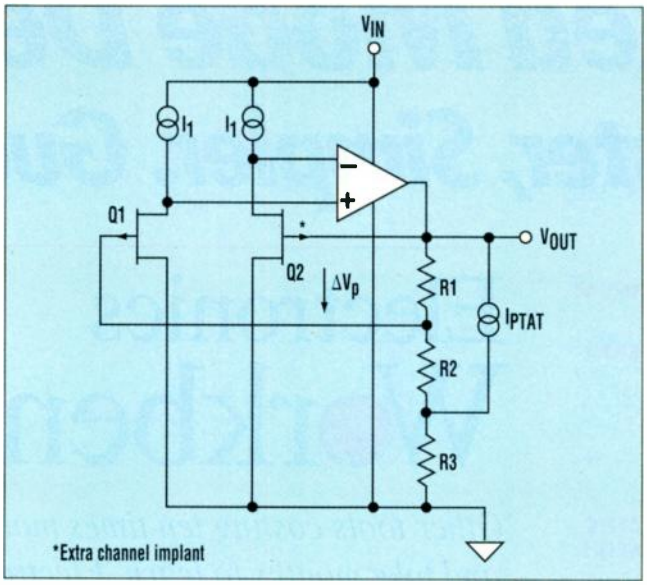
READER SERVICE 166



This new precision voltage-reference architecture is based on the difference in pinch-off voltage between JFETs Q1 and Q2. This design allows the reference to operate at 2.7 to 5 V yet it offers ultra-stable temperature and low-noise performance.

rection is needed, which further results in much lower noise. That's because most of a bandgap's noise is inserted in the temperature-compensation circuitry.

The temperature-correction term is provided by a current source, I_{PTAT}, which is positive and proportional to absolute temperature. Compensation of the circuit is governed by the equation:

$$V_{OUT} = (R1+R2+R3)/R1\ \Delta V_p + I_{PTAT}\ R3$$

On-chip trimming of resistors R1 and R3 set the output voltage.

Details, Details

The basic XFET design relies on equations similar to those found in proposed punch-through bipolar references and enhancement-mode/depletion-mode MOSFET references. Control of the basic process has limited such advanced devices to noncritical applications or conference papers. However, the JFET has proved to be a controllable device in its role as a reference due to process enhancements, such as the implanted JFET, given Analog Devices' complementary bipolar process.

Practical considerations have led to a low V_P of about 1 V and a high V_P of 1.5 V, yielding an intrinsic reference voltage of 500 mV. However, JFETs sport significant V_P control problems that generally limit the tolerance on the intrinsic reference voltage to within ±15%. The tolerance limitation in turn mandates the need to use laser trimming for any high-volume IC device manufacturer.

The temperature coefficient is largely that of the dielectric constant, about 110 ppm/K, plus an additional term due to the difference in built-in voltage caused by the extra implant. Thus, the reference voltage changes at about -117 ppm/K (±8 ppm/K) with about 3 ppm/K of curvature. Compensation methods used to trim the temperature coefficient have resulted in a final temperature coefficient of about 3 ppm/K typical, and 8 ppm/K maximum, over the full military operating temperature range. A second-generation XFET reference is on the way with an expected typical temperature coefficient of just 1 ppm/K. The improved temperature coefficient has been achieved by understanding and trimming second-order effects, and by using data learned from the laser-trimming process.

Price And Availability

The ADR290, the ADR291, and the ADR292 are available now. An XFET reference putting out 5 V, the ADR293, will arrive by year's end. All four references are available in TO-92,SO-8, and TSSOP-8 packages. Three electrical grades also are available for each reference. In quantities of 1000, pricing starts at $1.95 each.

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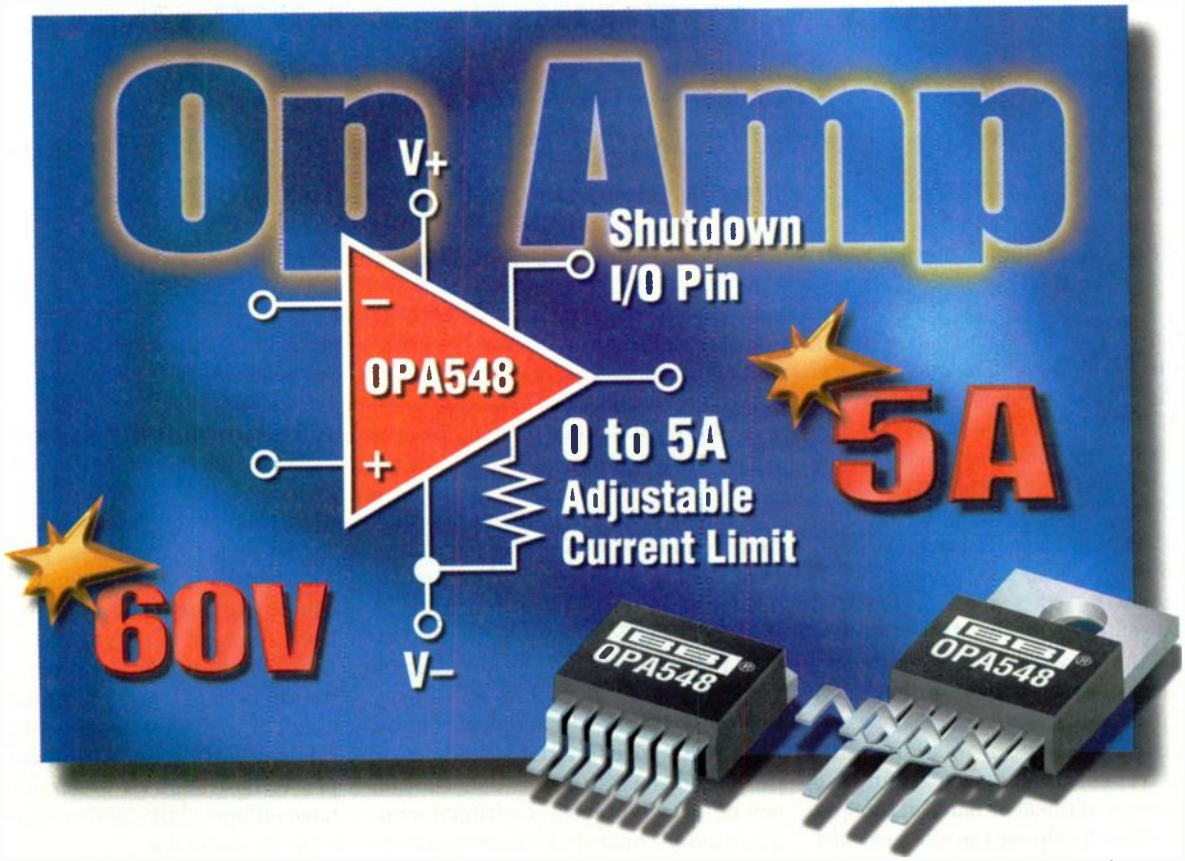

OPA548—easy to use and it packs a peak output of 5A (3A continuous). It operates on up to ±30V dual supplies or a +60V single supply. Input common-mode range extends below V– to simplify single supply circuits. It's ready made for driving heavy loads such as motors, valves, speakers, or as a programmable V/I source.

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OPA548 is available in two power packages: 7-lead DDPAK and 7-lead TO-220. It is priced from **$5.45** in 1000s.

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OPA544	FET-Input	70	2	8	TO-220, DDPAK	X	11250	82
OPA541	High Current, FET-Input	80	9	10	Power Plastic,TO-3	X	10737	83
OPA512	Very High Current	100	15	4	TO-3		10600	84

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Exploit Software Flexibility To Add PC Multimedia Functions

Don't Rely On Chips Or Boards To Add New PC Hardware Functions. Instead, Program Adaptable Multimedia Engines To Perform An Array Of Processing Tasks.

MARK NOGAKI, Toshiba America Electronic Components Inc., 1060 Rincon Circle, San Jose, CA 95131; (408) 456-8900.

There's good news and bad news for the PC industry. The good news is that PCs are booming. Tomorrow's PCs will take on a number of roles: 3D game machines, home-entertainment systems, computer telephony stations, network nodes, data-visualization workstations, 3D-modeling stations, and Internet stations. The bad news is that a new board is usually added for each new function. It's time to try a new tactic: software expandability.

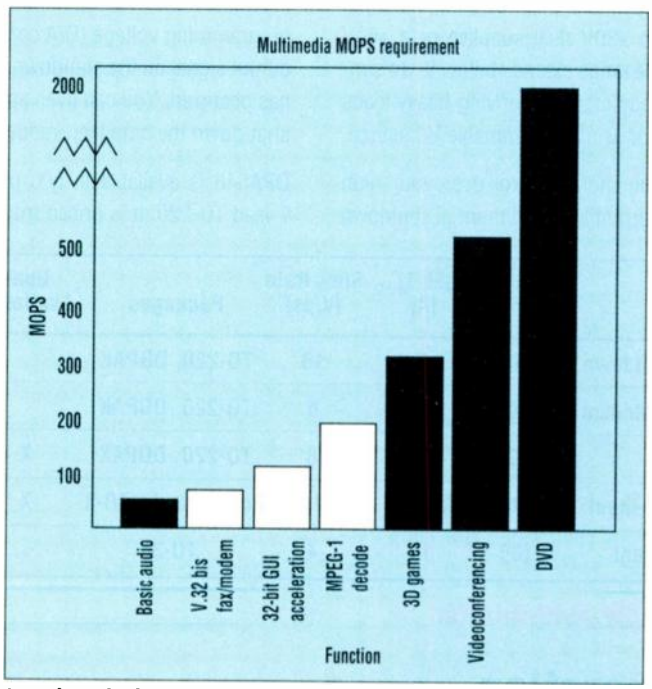
These new applications demand a great deal of additional processing capabilities. While some of this capability comes from faster, more powerful host CPUs, most of it will be handled by special processing chips on the motherboard or adjunct function-processing cards. New functions typically require new peripheral cards, such as Sound Blaster, modem, or graphics-accelerator cards. Over time, this adds up to a lot of pc boards.

Even worse, adding cards is out of sync with the trend toward PCs as closed boxes, or managed PCs. These types of systems are configured at build time and expanded via serial buses such as USB and FireWire.

Most new functions require that multimedia software/hardware be added to PCs. These multimedia functions include:

- 3D graphics
- Computer telephony
- High-quality audio/stereo
- Video capture, editing, and export
- Video conferencing
- DVD
- 3D data visualization
- Real-time 3D games
- Fax, modems, and networks

Collectively, the multimedia functions require a lot of processing power *(Fig. 1)*. Today, there's a separate chip or engine for each of the functions. A digital signal processor handles the modem function, a 2D/3D graphics accelerator handles the graphics, and a separate audio processor handles the audio. However, those functions need not be processed separately. Instead, they all can be handled by one multimedia engine under control of a host resource manager that ensures that the processing resources are available as needed.



1. Multimedia functions require a lot of processing power. This graph shows the estimated MOPS needed for some common functions.

A Programmable Approach

When you run a new software program, you don't buy a new PC. You simply load a new software package and the hardware platform stays the same. That kind of expansion and flexibility can be extended to PC hardware functions. Instead of adding a new chip or board for each new hardware function, we can use software to program adaptable engines—media processors—to take on the functions. And we can improve those engines, much the way we have enhanced the X86 architecture to take on new tasks.

Software programming is typically the way to go for complex functions that are just emerging. Programming provides a flexible base that can accommodate early changes and standardization tweaks. However, when the function becomes standardized, then a hardwired solution is usually cost effective. Graphics functions such as VGA and MPEG1 have become hardware standards, and have transmuted into hardwired chips or cores for ASIC development.

There are two major problems with relying on hardwired solutions. The first is that the functions eventually become outmoded. VGA, for example, is the standard display technology for PCs. It relies on a register-based interface that is increasingly emulated by

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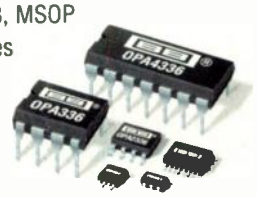

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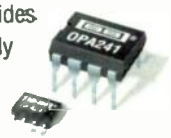

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higher-level graphics accelerators. The second problem with hardwiring is that multimedia PC standards continue to evolve. Hardwiring each standard, and then carrying it along to new designs adds size and cost. It also complicates newer, more sophisticated application programming interfaces (APIs).

Programmability, on the other hand, offers a flexible way to accommodate new or old functions and standards. The required standard or function can be dynamically loaded into the media processor as needed. Most systems don't require all possible interfaces to run. Unfortunately, in a hardwired system, the only way to accommodate all standards is to build them in.

Programmable systems can easily adopt new standards or incorporate existing standards' changes and fixes. The software approach enables the multimedia system to load the proper application mix as needed. For example, game applications require 3D graphics and positional sound placement, but DVD movie players need MPEG2 and Dolby AC-3.

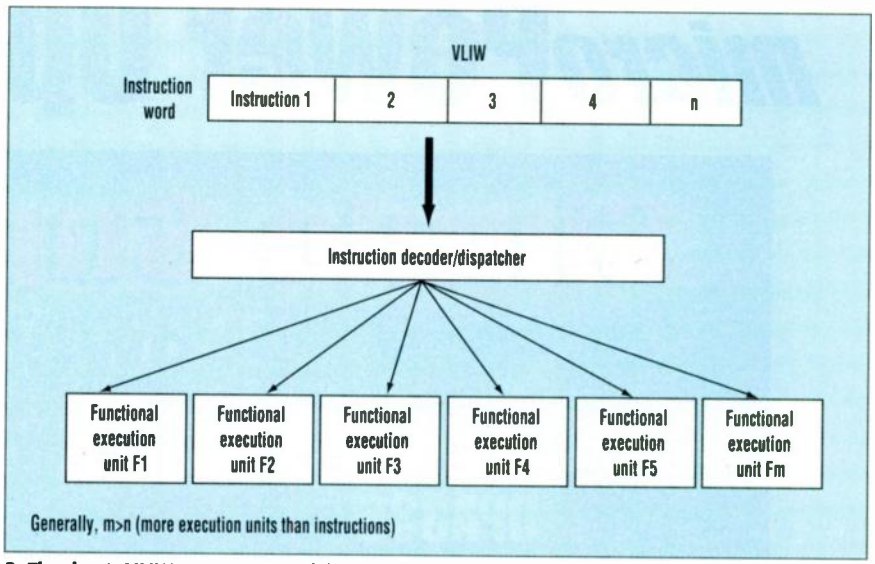
A programmable multimedia engine needs its own real-time kernel. This kernel schedules the function tasks, interfaces to the host, and monitors subsystem operation. The engine also requires a level of host-side software to manage its resources and interface with the host software (receive multimedia API calls).

Finally, programmability and hardwiring are not necessarily mutually exclusive. Key hardwired functions can supplement the main engine on the same chip. For example, the Mpact media processor has both a hardwired motion-estimation unit and a 3D graphics engine. These functional units set instructions on a cycle-by-cycle basis.

Why Not RISC?

Why not use a high-performance RISC chip as a multimedia processor? Because von Neumann architectures have evolved to large-scale desktop and server processing. They are more appropriate than RISC processors for this application *(see "RISC Limitations For Multimedia Applications," this page)*.

Current RISC processors use high clock rates, deep pipelines, multilevel caches, and superscalar execution to raise processing power. Fourth-generation RISC chips such as Sun's UltraSPARC issue up to four instructions per cycle. They, along with Intel's Pentium II, use of branch prediction and prefetching extensively to minimize bubbles or disruptions of the pipeline processing.



2. The classic VLIW processing model issues multiple instructions per clock cycle. The instructions are performed concurrently by multiple execution units.

But to date, RISC architectures have not been able to deliver a high percentage of their superscalar processing capability. A superscalar RISC such as the 604e PowerPC can issue up to four instructions per pipeline cycle, but is lucky to sustain an execution/completion of two instructions per pipeline cycle. Branches are the main culprit: they are one-fifth or one-sixth of the code and can't always be predicted. Bad guesses can create pipeline stalls or bubbles. Similarly, RISC processors tend to use cache as an input buffer, and when the necessary data or instructions aren't in the cache, pipeline delays can result. Some of these delays, such as page faults, can be expensive.

RISC processors are sophisticated compute engines able to handle a wide range of applications. In contrast, multimedia applications are much more well-defined. Processing is characterized by the inputting and massaging/converting of a stream of display or audio data. The multimedia programs can't switch around in the middle of processing a flow, and still have enough time to handle the process flow. Rather, multimedia processing is similar to the inner-

RISC Limitations For Multimedia Apps

- Limited Superscalar Operation: two or fewer instructions executed per clock cycle.
- Complex Logic: to reduce data conflicts and hardware resource conflicts.
- Design for General Applications: not tuned for regular, iterative multimedia coding.
- MMX Not Enough: provides multiple field operations on 64-bit registers. Doesn't help with addressing, integration, and loop control.
- Single-Thread Execution Model: can only operate on one thread at a time. Must context switch for each new thread. Can't process 3D rending and another application concurrently.

loop processing at the core of most large programs.

Using a RISC processor to run multimedia functions is like having a race horse pull a beer wagon. RISC is designed to quickly adapt to and run a wide range of applications. It's better to use a multimedia Clydesdale: an engine that is bred specifically for multimedia processes, that's tuned to process the fixed multimedia data streams, and that can process different functions in parallel.

The visual/multimedia ISA extensions like MMX don't transmute RISC chips into media processors. The MMX instruction extensions give Pentiums the ability to perform multiple-field operations in a single instruction using equivalent 64-bit floating-point registers. These do the same operation on all fields as part of the Pentium execution stream. MMX helps in some pixel and other field manipulations. It delivers an 8x or 4x speed-up by manipulating gangs of 8-bit or 16-bit field values. But the CPU must still do its own looping and control. And it can still only process one multimedia data stream at a time. MMX is not strong enough to turn a RISC processor into a media processor.

That's also true of the PC host CPU, Pentium or Pentium Pro. These don't have the horsepower to handle all the multimedia processing. The combination can bring mainstream processing to a walk, or even a halt. DVD alone can overload the CPU because it requires about 2000 millions of operations per second (MOPS). A 233-MHz Pentium Pro can do 233 to 466 MOPS for media processing—not enough.

A VLIW Processing Approach

Like a superscalar RISC processor, a very-long instruction word (VLIW) architecture issues multiple instructions per clock cycle *(Fig. 2)*. It differs from a RISC architecture in that the instruction executions are fixed by the compiler, and are not scheduled by local hardware when the data they need is available. Instead, VLIW processors hit each clock cycle with parallel instructions, all to be issued and executed concurrently. For VLIW, branch conflicts or predictions are primarily handled at compile time by the development software.

VLIW processors have had a checkered past. A number of companies (including Cydrome, Culler, and Multiflow) have tried to build on VLIW technology. None have succeeded. Part of the reason was that VLIW architectures were a new technology that represented a new incompatible direction for ISAs and software. The other reason was that the hardware technology, in particular, silicon densities, were not available to build cost-effective VLIW processors.

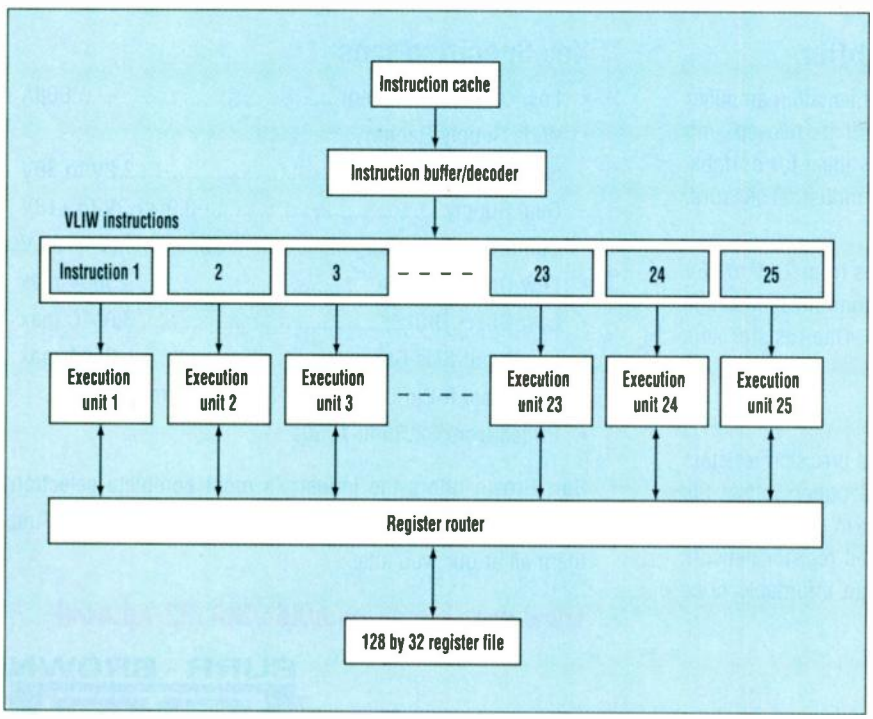
Today it's believed that the densities exist, and that VLIW processing is the next-generation computer architecture. Supposedly, Intel and Hewlett-Packard are jointly developing a new VLIW architecture, one that will be the next step in the X86 ISA evolution. This design, code-named Merced, is due out within a year or so. Additionally, Texas Instruments recently released its TMS320C6xx VLIW DSP, a 200-MHz VLIW processor with eight 32-bit instructions packed into each VLIW word.

A VLIW processor with four instructions per word looks very much like a four-issue superscalar RISC processor. Both take in a number of instructions in parallel for the next cycle. The VLIW processor takes in four instructions in a VLIW word; the superscalar RISC processor takes in four or more instructions in a cache line or partial cache line.

The difference is that the VLIW processor issues the instruction for direct execution on the next cycle (unless execution is blocked for all instructions), while the RISC processor must determine which instructions are executable, and issue those. RISC instructions may not be executable due to data dependencies (the data they need is being used by some other instruction or is not ready), or resource conflicts (the register, ALU, or other functional unit isn't available).

Superscalar RISC instruction execution is very much like a data flow processor. Instructions are held, pending the availability of the necessary data or resources, and then executed. Most of these CPUs have reservation stations that hold instructions in front of the resources (execution units) until the data and the unit is available to execute the instruction. Many superscalar RISC processors allow out-of-order execution (instructions executed out of compiled order) and use a number of techniques, such as register renaming, to minimize resource conflicts.

Needless to say, superscalar execution needs sophisticated, complex logic to support it. VLIW architectures, on the other hand, leave that kind of work



3. Processing is almost hierarchical in Philips' TriMedia chip architecture. The VLIW instruction word moves down from the cache to the decoder/dispatcher, which expands the VLIW word into five instructions.

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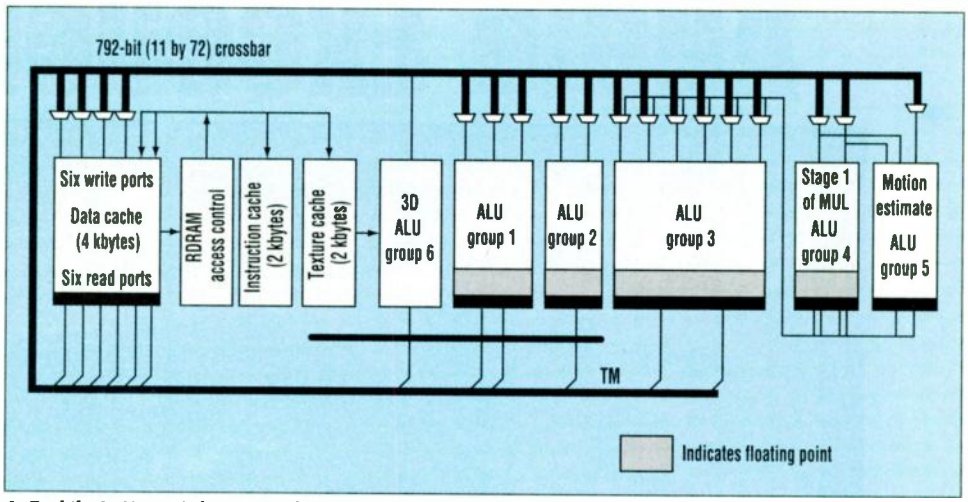
to the compiler. The VLIW compiler must come up with executable code, a set of instructions that can be executed in parallel with no data or resource conflicts. Instruction conflict must be resolved at the compiler level for a VLIW architecture to work effectively.

One problem that has held up the adoption of VLIW machines is having to resolve branches that are dependent on dynamic data (the value of the data is computed on the spot). Complex programs are hard to compile for efficient VLIW execution.

Interestingly, multimedia is an ideal application arena for VLIWs. The processing is regular because it works on flows of input data, and the processing is very iterative. It's also predictable. Thus, the multimedia VLIW processor works on regular blocks of code on fixed problem sets with iterative code.

The regularity and VLIW parallelism combine well for high throughput and execution rates. For example, Philips' TriMedia and Toshiba's Mpact/3600 and Mpact2/6000 claim peak instruction execution rates on the order of 2, 3.8, and 4 billions of operations per second (BOPS) respectively. Those execution rates are done with relatively modest clock rates of 100 MHz for the TriMedia and 62.5 or 125 MHz for the Mpact/3600 or Mpact2/6000 media processors.



4. Toshiba's Mpact2/6000 media processor employs an enhanced VLIW architecture. The Mpact CPU issues one instruction word per clock cycle. The word contains two instructions, each of which can drive one or more of Mpact's six ALU groups or functional execution units.

Multimedia VLIWs

The Achilles' heel of RISC superscalar and VLIW processing is instruction bandwidth. If a CPU issues and executes four instructions each cycle, then it needs four instructions per cycle. Using 32-bit instructions requires 16 bytes every cycle, or a 4800-Mbyte/sec bandwidth with a 300-MHz clock. The good news is that many of the instructions are available in cache, but that's still a pretty hefty bandwidth to maintain.

The problem only gets worse for wide-word VLIW architectures. A 200-MHz, 8-instruction-wide VLIW processor with 32-bit instruction words needs a 6400-Mbyte/sec (8 bytes by 4 bytes by 200 MHz) bandwidth just to move instructions for the next cycle. If those instructions aren't in cache, or the program does a lot of dynamic branching, the VLIW processor's efficiencies could drop off dramatically.

There are ways to increase the number of operations other than just increasing the VLIW instruction word size. Enhanced VLIW processors increase their operations with some secondary expansion on the instructions themselves. Therefore, a VLIW processor with four instructions can execute some multiple of four operations depending on what the addressed functional execution units do. This approach minimizes the VLIW instruction bandwidth while increasing operation throughput.

Philips' TriMedia VLIW processor uses an enhanced VLIW architecture *(Fig. 3)*. This CPU has 27 execution units and takes in a VLIW word with five instructions per word. These instructions are decoded and shipped to the individual execution units for parallel execution. The TriMedia compiler uses advanced techniques to compress the instruction word, especially no operations (NOPs).

The TriMedia architecture gets some extra performance boost with complex execution units. One instruction may launch multiple operations in its addressed execution unit, and these operations can be pipelined, taking more than one cycle to execute. As a result, while in a given cycle only five instructions are issued, those instruction can generate more than five operations. Moreover, operations specified by previous instructions, such as iterative adds, can still be running, contributing to a much higher throughput than just five operations per cycle.

Figure 3 shows the Phillips TriMedia architecture. Processing is almost hierarchical with the VLIW instruction word moving down from the cache to the instruction decoder/dispatcher that expands the VLIW word into five instructions. These instructions are shipped to their addressed execution unit. The execution units also take in register values from the CPU's large 128-register register file. Results are passed back to the register file.

The CPU minimizes branches by using "guarded" instructions: the instructions execute if a given condition is true. If the condition isn't true then the instruction doesn't execute, but there are no branches involved. The test is embedded in the instruction itself.

Like the TriMedia chip, the Mpact media processors are enhanced VLIW processors *(Fig. 4)*. The Mpact CPU issues an instruction word per clock cycle (at 120 MHz for the Mpact2/6000). This instruction word has two instructions in it, each of which can drive one or more of Mpact's six ALU groups or functional execution units.

Typically, Mpact's function units consist of multiple ALUs and functions. An instruction to one can result in the same instruction, such as an ADD function, being executed by all the ALUs in the group. These are single-instruction, multiple-data-paths (SIMD) instructions. Moreover, Mpact instructions can

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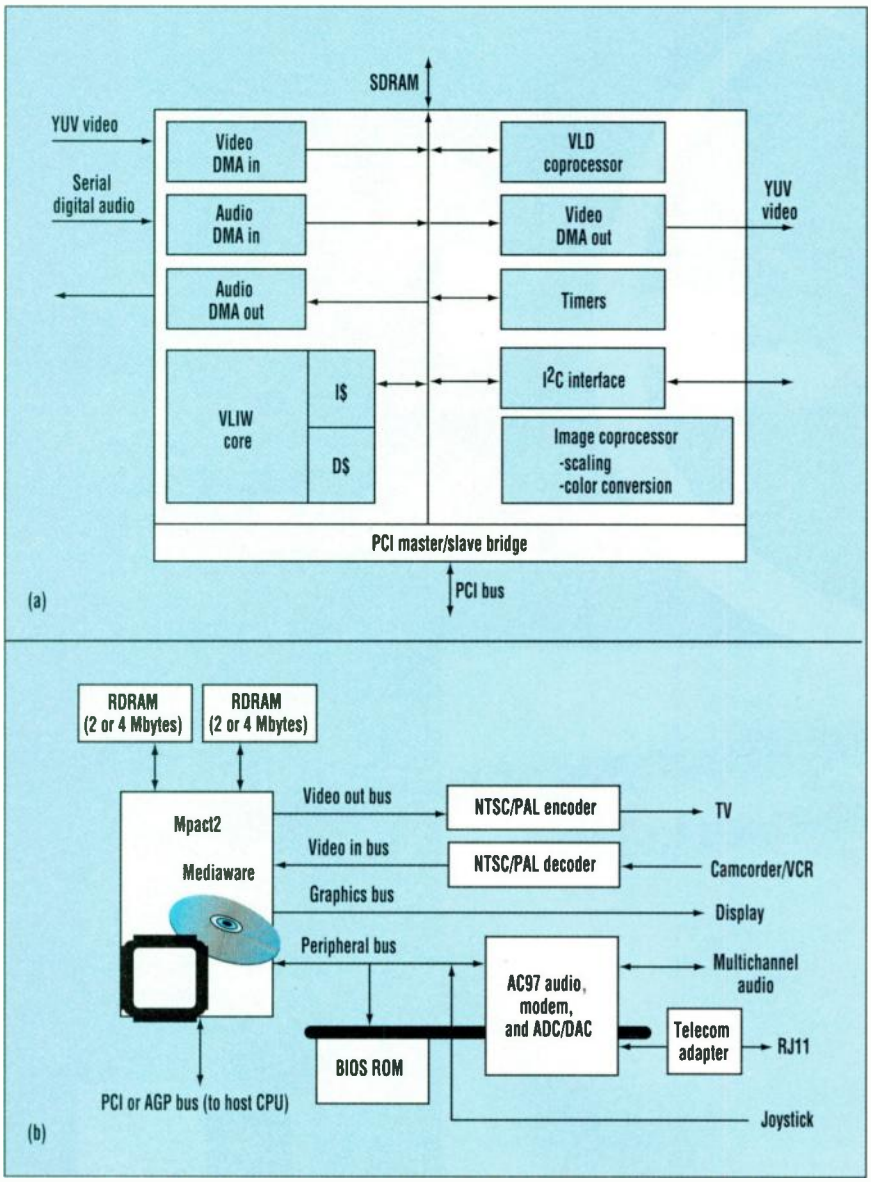
set loop processing in motion, in which a SUB function is continuously executed until a vector register counts to zero. Thus, the latency of that instruction is n cycles, which is a count in a vector register. Therefore, multiple instructions can be running in parallel with the new instructions issued by the CPU.

While the Mpact CPU only issues two instructions per cycle, up to 48 operations can be running in parallel. In effect, Mpact is a VLIW/SIMD architecture. Each instruction can cause 2-to-24 integer/3D operations, including matrix instructions such as Matrix ADD. Each instruction generates up to 48 results per cycle. By employing nonblocking looping instructions (the CPU continues to issue instructions to other groups while the loop runs) multiple operations can build up and execute in parallel.

Mpact's design builds around a 792-bit crossbar that connects the CPU cache memory to six functional units (ALU groups). The crossbar supports 11 72-bit word point-to-point transfers per clock. Each 72-bit instruction word contains two instructions. The 4-kbyte data cache is supplemented by a separate 2-kbyte instruction cache and 2-kbyte texture cache.

The ALU groups have multiple execution units or SIMDs (single-instruction multiple data). They can execute an instruction in multiple units or cascade operations. Two ALU groups are hardwired engines. Group 5 is a multilevel, hardware-motion-estimation engine and Group 6 is a 35-stage 3D rendering engine.



5. A block diagram of the Philips TriMedia processor shows the VLIW core and the chip's other functional blocks. It links to the host through the PCI bus (a). Toshiba's Mpact2 media processor links to the host CPU chip set via a 66-MHz, 32-bit PCI bus, or through an AGP point-to-point connection (b).

Multimedia Crossroads

A multimedia engine is where all the multimedia inputs and outputs come together. Elements include a graphics bus, video out (TV), video in (camera or VCR), multichannel audio out (AC 97 signals), peripheral bus audio, telephone line, joystick, and PCI link to the host chip set. Instead of separate chips for graphics, audio, and modems, all the work is all handled by a single media processor chip.

VLIW processors, like Toshiba's Mpact or Philip's TriMedia, provide a high-performance processing platform for a multimedia engine *(Figs. 5a and 5b)*. VLIW processors have the bandwidth to handle multiple application streams, much as a desktop system can run multiple tasks. In the VLIW world, the processor bandwidth can be multiplexed to serve multiple multimedia applications, giving the appearance of parallel execution. Instead of three or four boards, each with its own special application hardware and processor, one multimedia engine can do the job.

Mpact2/6000 deploys two 600-Mbytes/s RAMBUS channels, each with 2- to 4-Mbyte RDRAM memory. It links to the host CPU chip set via a 66-MHz, 32-bit wide PCI bus. This bus can be used for an AGP point-to-point connection, but lacks the sideband and split transaction features. AGP is Intel's newly defined graphics bus that builds on PCI, but adds some special high-throughput features and works as a point-to-point connection. AGP defines a 2x (dual-edge clocked version) that delivers a 533-Mbyte peak bandwidth. Intel is now working on a 4x version. Future versions of Mpact will support all the AGP features.

Multimedia Software

Media processors are software driven. Both TriMedia and Mpact include software. Both solutions include developed runtime and host-level software to support the chips. TriMedia supports user additions, whereby designers can

code for their TriMedia engines. Philips supplies a software kit.

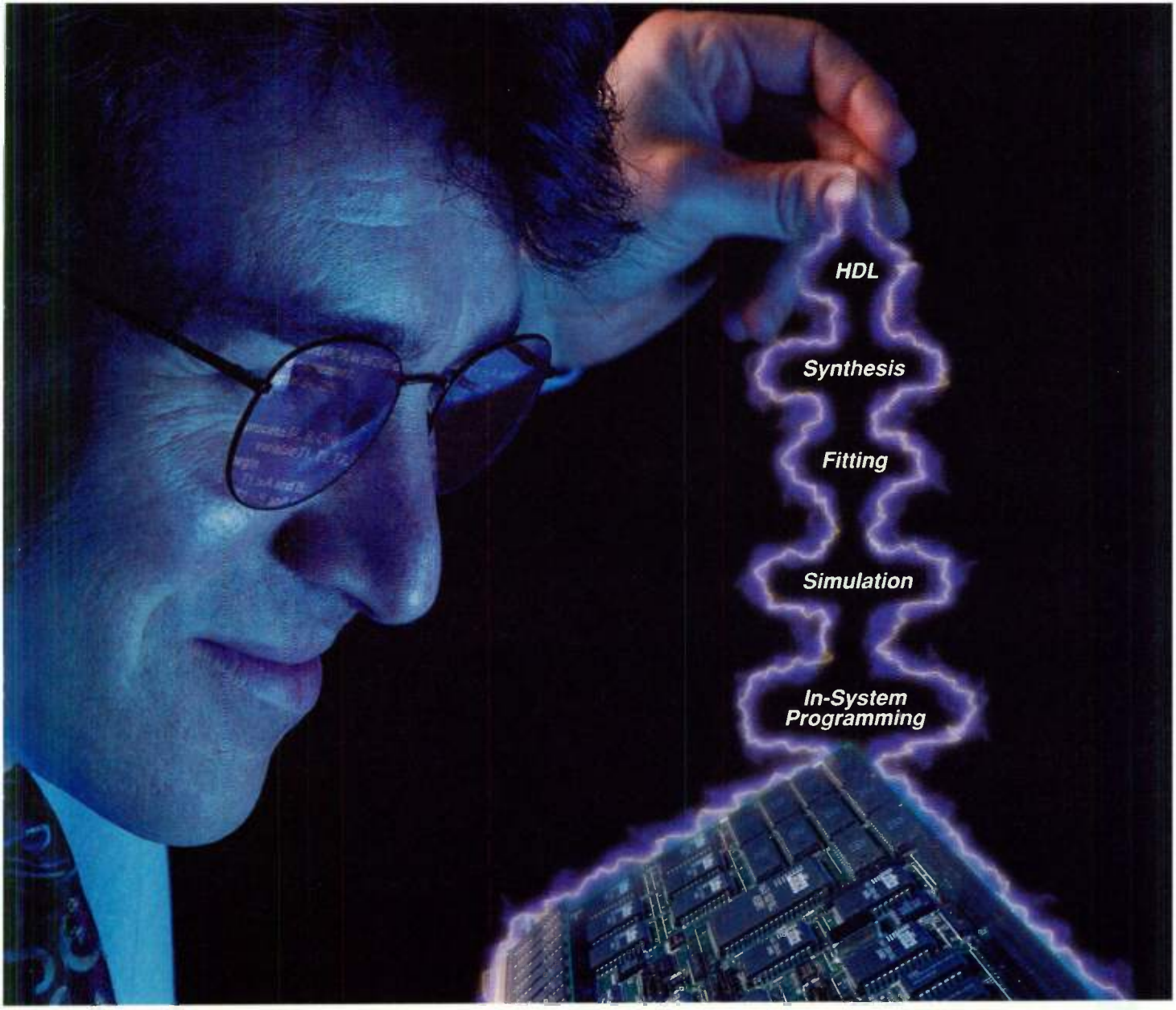
Mpact's software approach is different than most chip vendors. It provides a turnkey software package, Mediaware (developed by Chromatic Research), for both the host and multimedia engines. Mediaware has an interesting view of how a multimedia engine really works. To the host, Mediaware is essentially a shell that accepts MS Direct3D API calls. Those calls are either handled by the Mediaware Resource Manager on the host, or converted to calls and code downloads to the media processor. Some processing is done on the host with Mediaware application code.

In addition, the Mediaware Resource Manager on the host controls the media processor across the PCI/AGP bus. It downloads code for execution and tracks resource usage. The downstream multimedia engine runs with its own real-time kernel, MRK. This kernel brings the Mediaware modules up, schedules them, and monitors system operations. The modules include 2D graphics, 3D graphics, video, fax/modem, telephone, and videophone.

Programming a media processor like Mpact is not child's play. It's very much like programming the early digital signal processors, using a very cryptic instruction set in which each instruction can specify multiple operations. But designers needn't worry. Chromatic provides all the programming for the Mpact chip and for the Resource Manager on the host side that drives the Mpact chip over the PCI (or AGP) bus. Programming is at the application level with API calls to Microsoft Direct3D. These calls translate into function calls to the Resource Manager, which either handles the request locally or transforms it into one or more requests that are passed down to the Mpact media processor.

Mark Nogaki is the director of marketing for Toshiba America Electronic Components. He received a BSEE and an MBA from the University of Southern California, Los Angeles.

How Valuable	Circle
Highly	541
Moderately	542
Slightly	543



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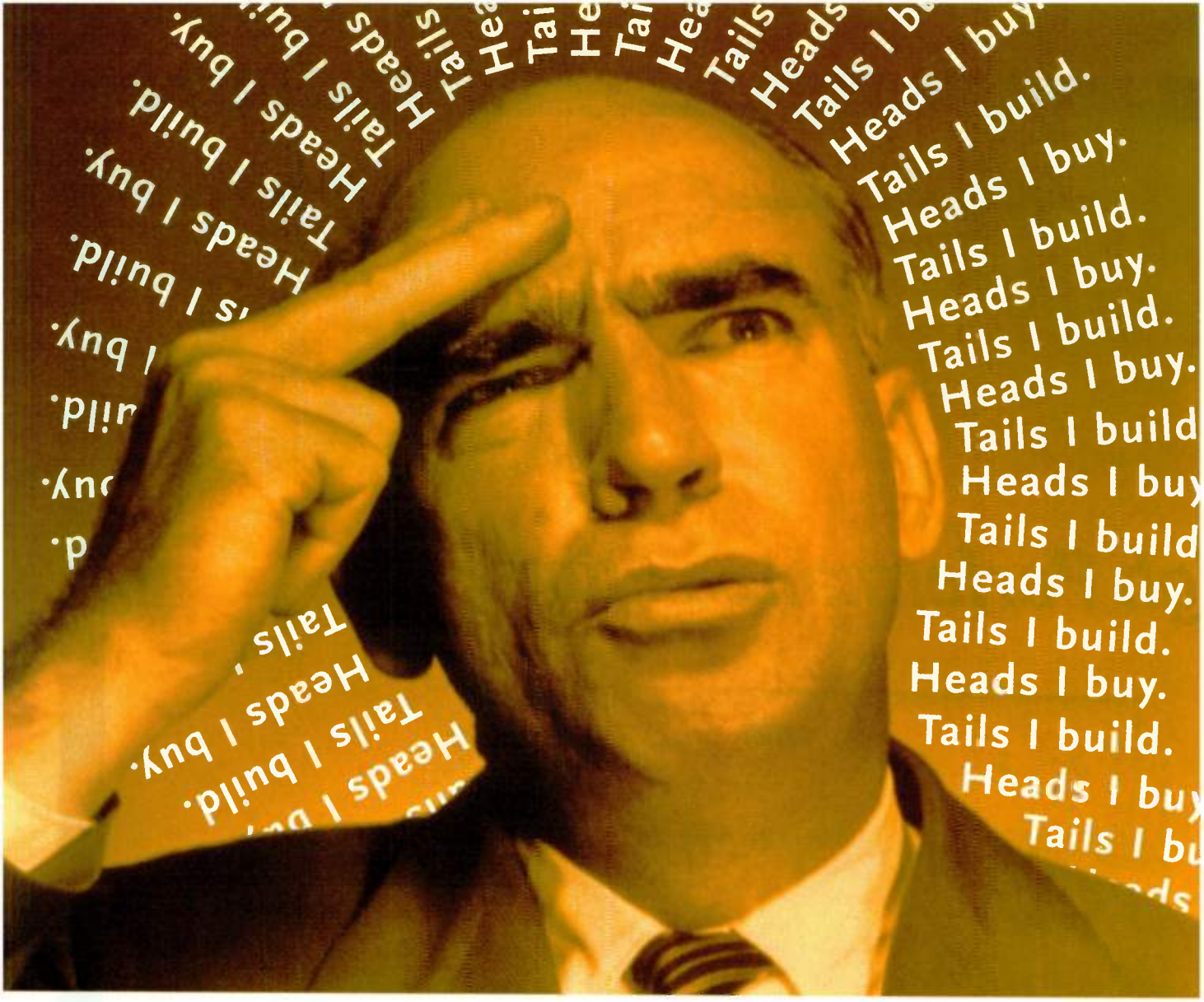

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Validate Image-Processing Device Models With A VHDL Test Environment

Growing Design Complexity Necessitates Accurate Device Models And Test Methodologies For Design Verification.

STEFFEN MUELLER, Robert Bosch GmbH*, Corporate R&D, Advanced Development Multimedia, P.O. Box 77 77 77, D-31132, Hildeshheim, Germany;+49 5121/49 4744; fax +49 5121/49 3190; e-mail: steffen.Mueller@fr.bosch.de.

Complex systems such as image processors are increasingly being designed in VHDL. The first step in a top-down design is the creation of a behavioral model that represents a detailed specification of the system. Validation of this model proves that it provides the required functionality. Necessary to the validation of the VHDL behavioral models such as those used in the design of image processors is a proper test environment. The test environment and the device under test (DUT) constitute the complete simulation system, the connecting interfaces of which must be carefully described.

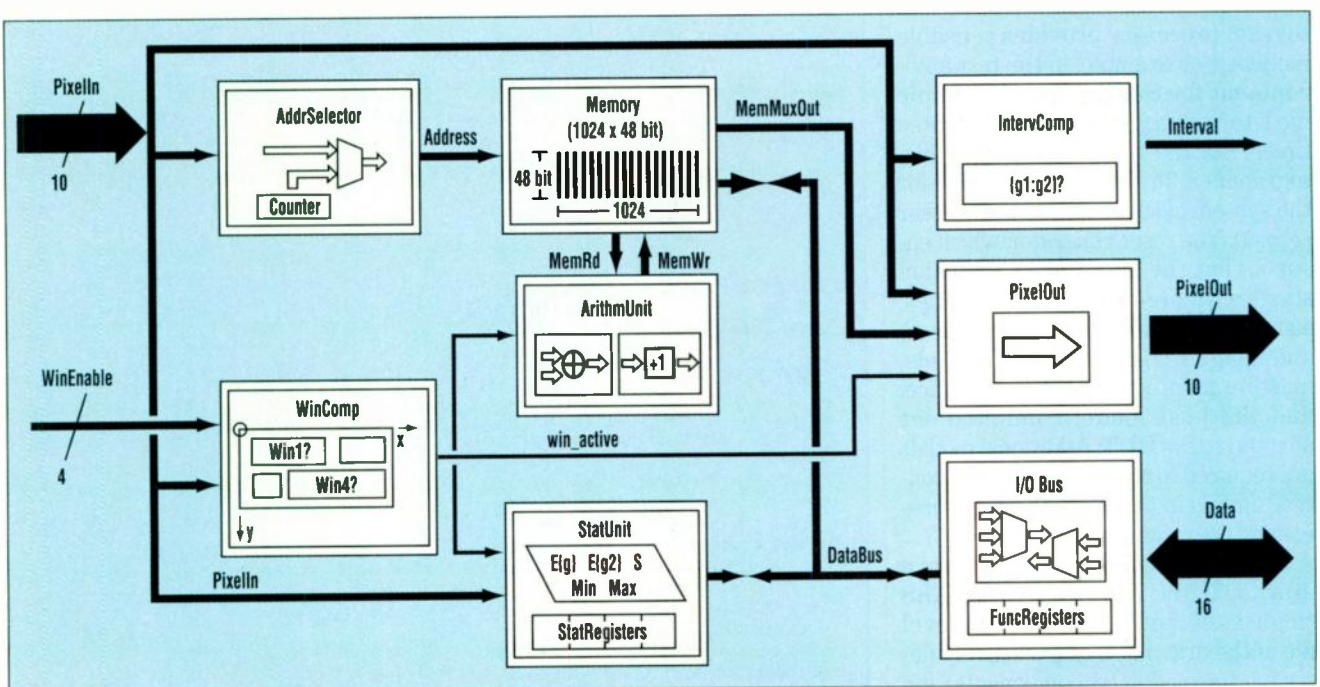
**(Note: the work described in this article was performed while the author was at MAZ Hamburg GmbH).*

The simulation of a special processor model for image-processing applications is characterized by an enormous amount of image data. For example, image processors in the image pre-processing area are switched directly into the pixel stream, and the original image is visually compared to the processed image resulting from the simulation. Both images are required in commonly used image formats, which means that data-handling requirements are tremendous. A host processor uses a data interface employing a special data-transfer protocol to program the DUT, and the results are obtainable via the data interface. A design suitable for test environments must explain the modeling of the different data sources.

The design should meet the following criteria:

- A carefully separated test environment and DUT (proper interfaces).
- A host-processor model calling the commands (program) from a text file.
- Documentation of the performance by a journal file, on-screen notes, and messages.
- Modeling the image input/output as image and camera interfaces.
- Automatically and reasonably checking system signals as much as possible.
- One configuration file containing all important system parameters (clocks, resets, etc.).

There are ways to make it easier to handle the test environment. For example, this is possible by preparing a



1. This block diagram accurately depicts architecture of the histogram processor in real time. The processor also providesin statistical characteristics in these windows, which can be controlled by external signals.

"box of models" that can be reused for different test environments, and by creating a simple way to generate the VHDL top level of the test system containing the DUT and test environment. Also, by providing models and the connection of all these components (structural model), dealing with the test environment can be substantially easier.

The practical application of the above requirements can be demonstrated by designing a test environment for a histogram processor used in image processing. The test environment would include models for data I/O (host processor), image I/O (camera, memory), several clock generators, and a reset generator, as well as some models for control-signal generation and checking.

The processor is able to compute histograms in up to four variable windows in real time *(Fig. 1)*. It also provides statistical characteristics in these windows, which can be controlled by external signals. The Interval signal proves that the gray level of the pixel of interest is in a pre-loaded gray-level interval. The histogram data is usually employed to generate a binary image and to perform image enhancement. A 16-bit data interface allows the histogram processor to be programmed and the computed values transmitted.

The Test Environment

The test environment for the histogram processor provides reusable models. For example, in the test environment for this design, the simple model of a clock generator is used three times: For the system clock of the histogrammer, for the pixel clock, and for the system clock of the host processor *(Fig. 2)*. The reset generator, which ensures that the hardware simulation starts with pre-defined signal values, also is reusable. The data I/O, or 'host', and image I/O, or 'image_io' models, must be adapted to the data interface, and the host model command set adapted to the DUT. Additional models are required to check and generate control signals in the current image-processing operation.

The top-level design exists as a drawing in the EDA-Tool COMPASS "logic assistant." A VHDL top-level file of the drawing that exclusively describes the models (as components) and interface connections can be derived. The time parameters of the clock and the reset generator, identified by name, can be found in a configuration file. The models read the parameters of interest from the configuration file during the initialization process by using the VHDL 'textio' package.

Host Processor Model

Table 1 explains the principle structure of the VHDL host-processor model. There is a procedure for every command for describing its function. Commands for adapting the model to another device are easily added or deleted. This method of operation is characterized by extreme flexibility, and allows the host processor model to be used for another DUT. In addition, the host processor checks the data-transfer protocols for faults and time violations. The time parameters are defined as constants in the generics section of the commands.

The command text file, to which the host interface has access via the data interface, holds the commands required to program the histogrammer. The host processor model reads the commands in the command text file, sending and receiving data according to a selected protocol. The host model provides on-screen comments on test performance, which are then captured in a journal file for documentation.

TABLE 1

```
ENTITY host IS
  GENERIC (  tRHRL:TIME:=  25ns; tCLRL:TIME:= 15ns;...tDHCH: TIME:=  15ns);
  PORT (...):
END host;
ARCHITECTURE behavioral OF host IS (...)
  BEGIN (...)
  main: PROCESS
     BEGIN
       reset_loop: LOOP (...)
          processing_loop: LOOP
          WAIT UNTIL ((HostClk'EVENT AND HostClk='1') OR Reset='1');
          NEXT reset_loop WHEN (Reset='1');
--RESET 'high active'
          first_letter  :=' ';
          second_letter  :=' ';
             CASE first_letter IS
               WHEN 'S' =>
                 CASE second_letter IS
                   WHEN 'T' =>
ST_procedure(...);
                   WHEN OTHERS =>
COMMENT_procedure(...);
                 END CASE;
               WHEN 'R' =>
                 CASE second_letter IS
                   WHEN 'E' =>
RE_procedure(...);
                   WHEN 'D'|'B'|'H'=>
RDBH_procedure(...);
                   WHEN OTHERS =>
COMMENT_procedure(...);
                 END CASE;
               WHEN 'W' =>
                 CASE second_letter IS
                   WHEN 'T' =>
T_procedure(...);
                   WHEN 'R'|'B'|'H' =>
WDBH_procedure(...);
                   WHEN OTHERS =>
COMMENT_procedure(...);
                 END CASE;
               WHEN '-' =>
                 IF (second_letter='-')
THEN
COMMENT_2_procedure(...);
                 END IF;
               WHEN OTHERS =>
COMMENT_Procedure(...);
           END CASE;
         END LOOP;
       END LOOP;
     END PROCESS main;
   END behavioral;
CONFIGURATION host_CON OF host IS
  FOR behavioral
  END FOR;
END host_CON;
```

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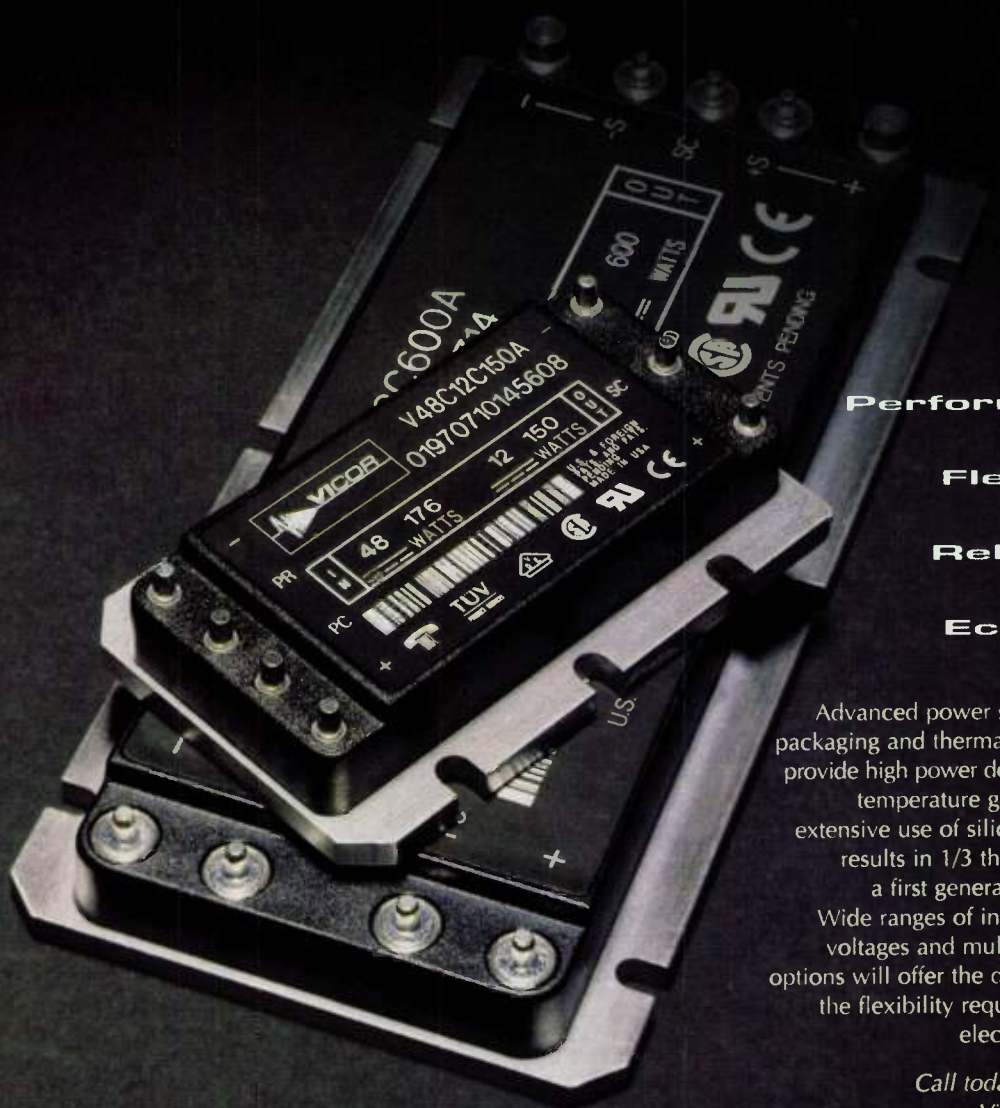

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The command text file must be prepared before starting the simulation. The structure of the host model allows an adaptation to another DUT, so the host processor model is reusable.

The flexibility of the host processor model structure can be illustrated by looking at the command set of the histogrammer *(Table 2)*. The commands allow access to the histogrammer memory and registers, start and stop operations, and wait-on-ready, or for an absolute time ('start' and 'ready' are histogrammer control input and output signals).

If the host processor model uses "RD <mode>" commands, the data will be transferred to an output file. The data in the file (histogramming data) need verification after simulation. When transferring data from the host-processor model to the histogrammer data interface, the value(s) for this "WR <mode>" operation appear(s) in the line following the command.

Table 3 shows a sample host command script. The host processor reads line-by-line and interprets/executes the commands. The first two letters in a line define a command; '—' indicates that a comment is to be ignored. The line in which the first two characters do not match any command appears on the screen as a comment. Executed commands will be shown on the screen, as well as warnings and error messages. Simultaneously, screen output is stored in the journal file for documentation.

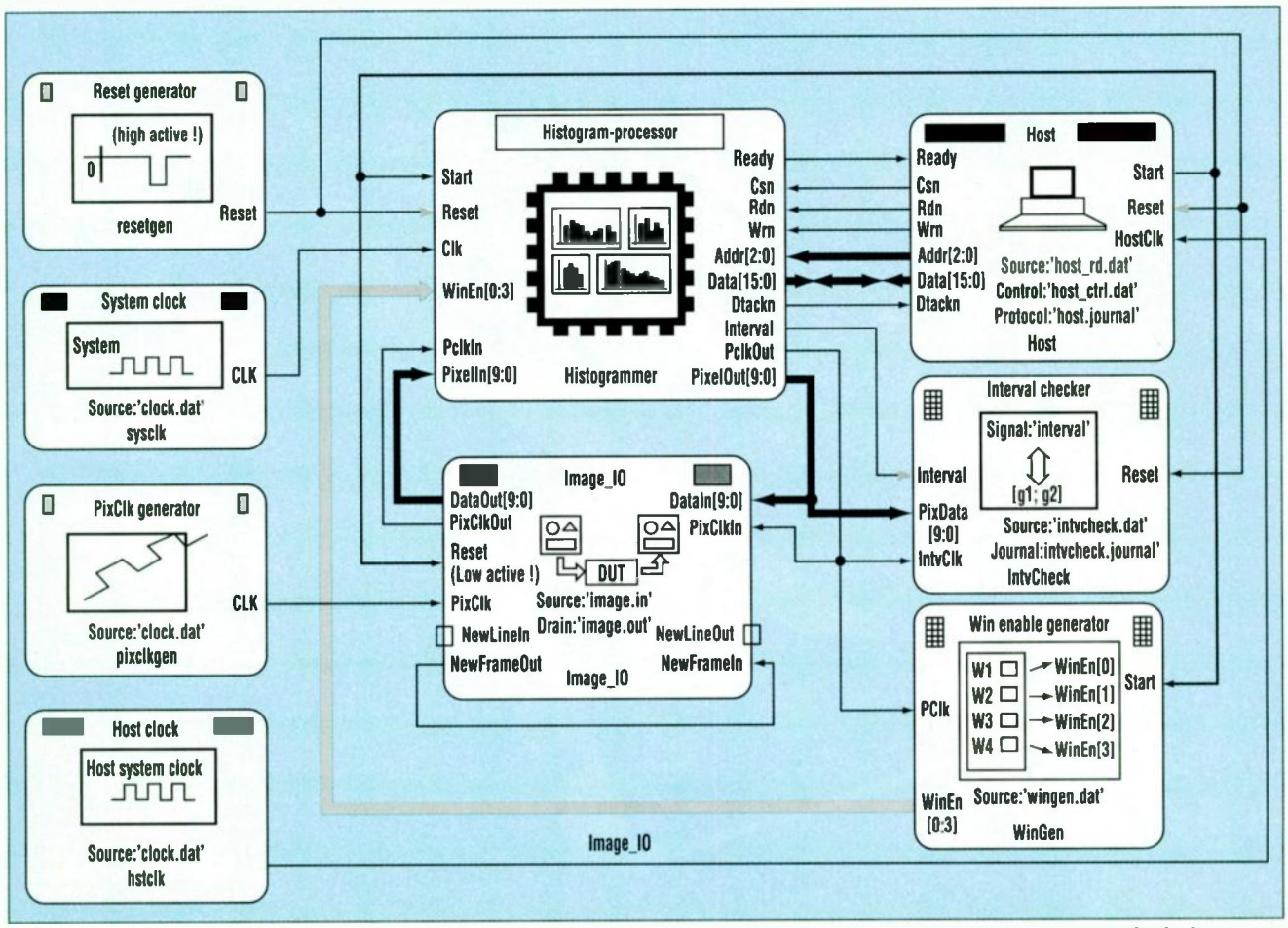
Three different bus protocols, single-data mode, burst-data mode and handshake mode, are available for transferring data. The memory and registers are addressed and accessed by the address and data registers. The address registers are incremented automatically after each read/write operation. This allows data transfer in the burst-data mode.

TABLE 2

```
ST n  Set START to n (n is '0' or '1')
RE n  WAIT FOR READY=n (n is '0' or '1')
RD    READ single data (data interface)
RB n  READ n data in BURST mode (data interface)
RH n  READ n data in HANDSHAKE mode (data interface)
WR    WRITE single data (to data interface)
WB n  WRITE n data in BURST mode (to data interface)
WH n  WRITE n data in HANDSHAKE mode (to interface)
WT t  WAIT FOR t (t is time value)
—     ignore comment
```

Image Data Interface

The image data interface (image_io) is the most important component in a test environment for image-processing applications. It reads the image data file and prepares the data for processing by the DUT. The DUT output provides images that can be shown on-

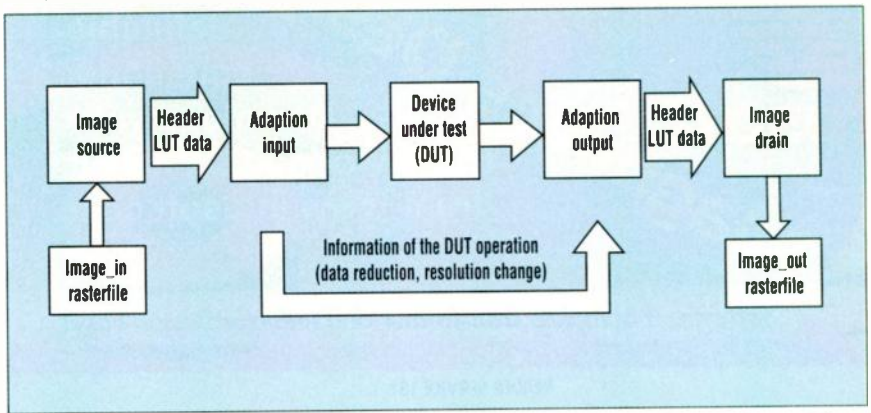


2. This top-level design view of the test environment was created using Compass Design Automation tools. The environment fo the histogram processor provides for the use of reusable models. For example, in this design, the simple clock generator is used three times.

screen after the simulation.

The image_io reads the image data from a rasterfile. This data is then converted to an ASCII file by a routine because the file-I/O in the VHDL standard is only applicable to ASCII files. Some simulators read directly from a binary file; however, there is no standard for this, and there is no guarantee of compatibility with other simulators. After the simulation, the DUT image output is converted from ASCII back to a binary format. In this format, the resulting image can be shown on a screen.

The histogrammer implements a simple pixel data interface. An outline for modeling image and camera interfaces is presented *(Fig. 3)*. Adapting this model to a special image interface is possible with minimal effort. Only two components, source and drain, are responsible for reading the image data from one rasterfile and writing the processed data back to another rasterfile. These components consist of special interfaces that provide all of the important information about an image and allow the creation of a new image. Two additional components can be used to adapt this general interface to the interface of the DUT to create a new test environment. This model is completely reusable.



3. The scheme of the image data interface model is illustrated above. Adapting this model to a special image interface is possible with minimal effort.

Clock Generator Model

The clock generator (for the system clock, 'sys_clk') reads the configuration file and the three values appended to its keyword and interprets these values as clock high- and low-time. The third value shows the variety of the clock period. The model uses a pseudo-random function (m-sequence) to generate a jitter.

The name of the clock can be easily changed by a string definition in the "generics" declarations. In the test environment, three clocks are implemented: System clock ('sys_clk'), pixel clock ('pix_clk'), and host clock ('hst_clk'). These models differ only in the generic part, for example, and adaptation means changing this string.

Reset Generator Model

The configuration file consists of lines beginning with the keyword 'reset.' The model for the reset generator looks for these lines and reads the following time value. After that time, the model changes the reset value and looks for the next line until the end-of-file is reached. The initial reset value depends on the active level of the reset signal. The reset generator can be re-used.

Special devices generate and need special control signals. These signals always require an absolutely new VHDL model. The histogrammer delivers the control signal 'Interval' and needs the external window control 'WinEn' for a special function. Usually, there is no way to reuse these kinds of models, because they are too specialized.

If the test environment components and their interfaces have been carefully modeled, the test environment will imitate reality in great detail. The test environment should contain components that verify all outputs by comparing them to the expected values. Components connected to asynchronous parts of the DUT should check for setup-and-hold-time violations of signals.

Two possible test strategies that might be implemented include:

1. Consider all possible faults of function and search the simulation results for them. Do not expect to cover all possible faults. Use this approach if you are convinced of the correctness of your test environment.

2. Check whether the device behaves as expected; for example, insert assert-constructions into the VHDL code to verify the correct function. An assertion occurs in case of either an undefined sta-

TABLE 3

```
* preparing the histogram operation *                    sm17.01.95

WR RegAddr
0
WB RegData 18              - window sizes
0 0 63 63 0 0 0 0 0 0 0 31 31 32 32 63 63 63 63
WR RegData                 -(Reg 18) 10.1111.0000 set stopbits 752
WR RegData                 -(Reg 19) histmode 0
WR RegData                 - (Reg 20)0
WR RegData                 - (Reg 21)
62
WB RegData 6                   -(Reg 22-27) interval, thresholds
100 150 150 0 150 150

     * start and wait for ready *

ST 1                  -start histogram operation
RE 0
RE 1                  - wait for operation end
ST 0

     * read histogram data window 1 *

WR RegAddr
19
WR RegData
123                     - read data of window1, clear memory
after read
WR MemAddr
0                     - start address
RB MemData 2048
```

tus or a deviation of functionality. Determine whether the problem is due to the test environment or the DUT. After eliminating the fault, start the iterative process anew. This approach, focusing on behavior, is a more promising method than looking for faults.

The test environment previously described checks for the expected behavior; that is, it looks for unexpected values. A generous insertion of checks will help to locate the fault.

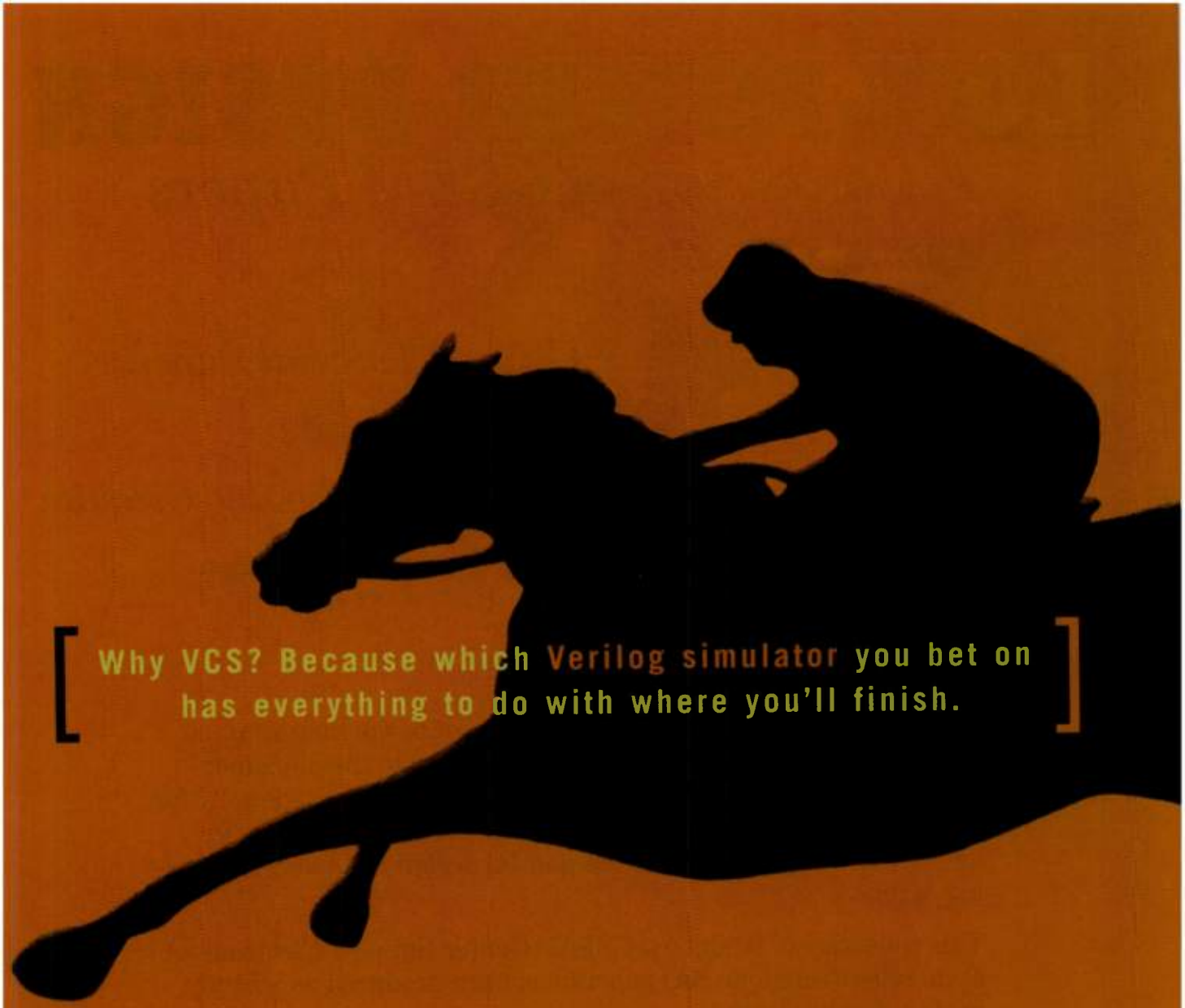
Pulling It All Together

Composing a test environment is an important process. The designer must describe the kind of environment in which the device can be used, and has to consider the problems that can occur. Obviously, no tool can automatically produce the results of basic considerations—that is the designer's work! But there are opportunities—and a requirement—to efficiently document the test-environment interfaces and connections. Furthermore, the results of a simulation should be stored.

In the VHDL test environment presented here, component parameters are listed in a configuration file, performance is documented in a journal file (including all warnings and errors), and the resulting image is available as a rasterfile. In this environment description, templates have been given for host processor and 'image_io' components, both of which allow easy adaptation to accommodate different DUTs. Clock and reset generators described are modeled only once. Special signal generators and observers must be designed for each DUT. The test strategy is to check for the expected values and in case of failure, determine whether the problem is located in the test environment or in the DUT's functionality.

Steffen Mueller received his degree from Kaiserslautern University, Germany and continued his studies at Michigan State University as a scholar in 1992. From 1993 to 1997, he worked at MAZ Hamburg GmbH where he was involved in the development of dedicated hardware for image processing.

How Valuable	Circle
Highly	538
Moderately	539
Slightly	540



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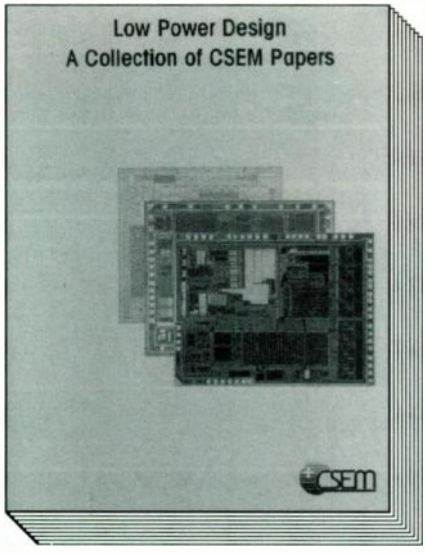

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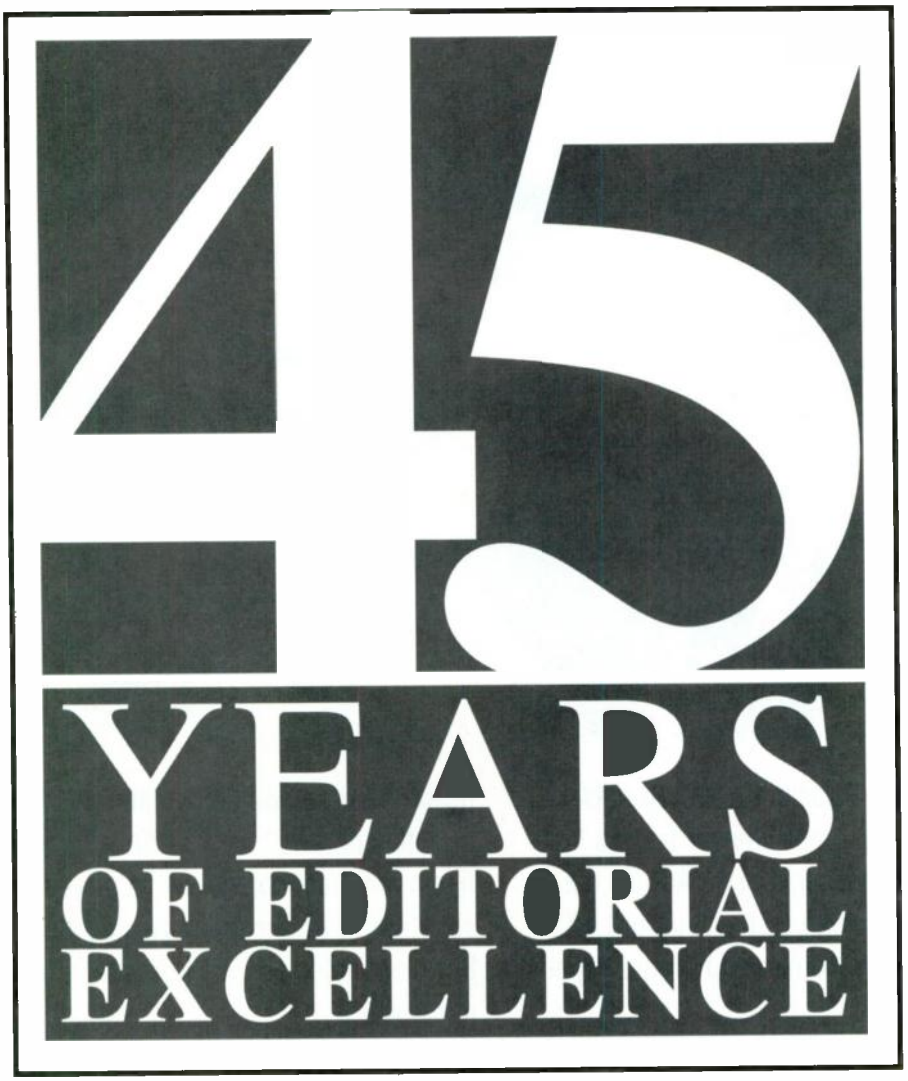

Electronic Design's on-going objective is to observe and report the latest breakthroughs in EOEM technology. By providing this information, *Electronic Design* has been the strategic partner of system designers and suppliers for the past 45 years, helping to bring them together so they can deliver more competitive products to market faster.

A PENTON PUBLICATION

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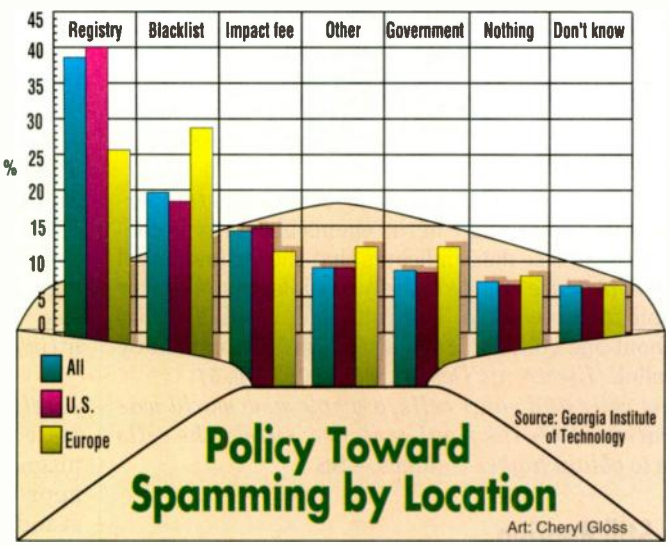
ELECTRONIC DESIGN QUICK LOOK

Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Spicy Messages

Who knew back in the '20s, that spam would become a code word for a ridiculously high number of times an article is posted to one or more newsgroups. And, if you ask a hacker what spam is and where it came from, he or she will probably reply that it's a method of crashing programs by overfilling a fixed-size buffer with a huge amount of input data. And, no doubt, you'll definitely run into some Monty Python fans who will sing the Spam Song. It's such a loud noise out there in Web Land that doing a search for "spam" yields more links than "sensors." The Graphics, Visualization, and Usability Center at the Georgia Institute of Technology decided that the topic merited an on-line survey. Over 19,970 Internet users responded to the study. According to the survey, 38% of the respondents supported an "opt-out" list for people who choose not to receive mailings. This type of registry was more favored by Americans (40%) in the study than Europeans (25%). Women (47%) were more in favor of the registry than men (34%). The other popular option, blacklisting the companies who participated in spamming activities, was favored by the Europeans (27%), but not as strongly by the Americans (17%). Very few respondents favored unsolicited mailings, but only 8% of respondents wanted legal action taken to ban spamming. Of the respondents, 14% recommended that the spammers be charged a fee for their mailings. The majority of people using e-mail just delete the unwanted messages, but would prefer having filters on their systems to prevent the messages in the first place. One of the more interesting questions the pollsters asked of the study participants was if the respondent had ever provided false information to Internet sites. Generally, the study coordinators found that people tended to falsify information because they really don't trust the site collecting the information. Mostly they complained that the majority of sites don't wear a label stating what they're going to do with that information. Of the respondents, 60% said that they had never given false information while registering at a web site. Women who participated in the study were less likely than the men in the study to admit to falsifying information. In the section of the survey dealing with problems using the web, it was no surprise that of linkrot (that's broken links for the lingo impaired), speed of downloading/viewing, not being able to find information that the user knows is available, not being able to organize web-collected information, not being able to revisit sites, not being able to visualize sites and potential sites, cost, and speed came out on top. Although 66.31% of the respondents said that speed was their biggest issue with the web, this figure shows a 10% drop from the previous year's study (76.55%). The study coordinators attribute this trend to the increase in connection time of Internet users. The second biggest thorn in the side of the web user is linkrot (49.90%). This situation is only remedied by e-mailing the location where the user found the bad link to let the host know that their link died. Finding the new link is another story, however, as some pages are discontinued, some move to different servers, or any number of mysterious explanations. Cost, surprisingly, doesn't appear to be an issue with the respondents, as only 5.41% said that it was a problem. As far as breaking down issues by age, 35.84% of 19-25 year-olds, as opposed to 26.44% of 50+ers, were more likely to complain about not being able to find information that they know is out there.



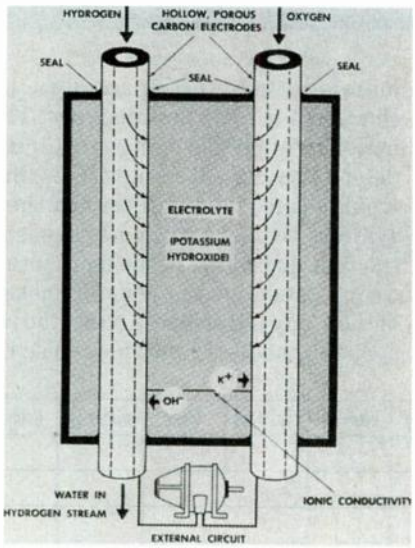
For more information, contact the Research Communications Office, Georgia Institute of Technology, 223 Centennial Research Building, Atlanta, DA 30332-0828; (404) 894-6986; fax (404) 894-6983; e-mail: www-survey@cc.gatech.edu.—**DS**

40 YEARS AGO IN ELECTRONIC DESIGN

Electricity From Gases Now Practical

The direct conversion of the chemical energy of gases into electricity, long a dream of scientists, and for years a laboratory curiosity, has been accomplished with the development of the first chemical fuel cell capable of economically producing thousands of watts of power. Using hydrogen and oxygen as fuel, the new silent source of power has been developed by scientists at the Research Laboratories of National Carbon Co., New York.

Present designs call for the grouping of a number of specially catalyzed, hollow porous carbon electrodes in a sealed cell containing a solution of potassium hydroxide as the electrolyte. Hydrogen and oxygen enter the cell through the hollow electrodes, and diffuse through porous carbon to the surface, where the gases come in contact with the electrolyte. At the hydrogen electrode, the electro-chemical reaction with the potassium hydroxide produces water and releases an electron which enters the electrical circuit. The electron flows through the external circuit, and returns to the cell at the oxygen electrode. In the electro-chemical reaction of the oxygen and the electrolyte, the electron is accepted. Ionic conductivity through the electrolyte completes the circuit.



The general efficiency of the cell ranges from 65 to 80 per cent when operated at normal pressures and temperatures. At lower currents, a greater percentage of the chemical energy is converted into electrical energy. Research to date indicates that the optimum fuel cell design will be one which will produce approximately one kilowatt of power from a packaged unit one cubic foot in volume. The voltage developed across the electrodes of the cell is about one volt, and any voltage can be obtained by connecting many cells in parallel. *(Electronic Design, Oct. 1, 1957, p. 5)*

With developments in fuel cells and solar cells, a whole new world was opening up in power generation. Note the final sentence; surely the cells should be connected in series to obtain higher voltages.—**SS**

Machine Tells If Heart Is Still Beating

Vital information on the condition of the heart of an unconscious, pulseless person is made immediately available by an electrical monitoring device, presented before the fall meeting of the AIEE in Chicago. The device was described as a cardiac monitor and is portable, battery-operated, inexpensive, explosion proof, and uses transistors. This monitor is used in aiding in the detection of stoppage, fibrillation, or quivering of the heart.

Diagnosing the condition of an unconscious, pulseless patient, resulting from disease, accident, or drugs, is difficult. Serious brain damage or death will result if the heart does not resume normal beating within four minutes, and death is almost certain over 12 minutes. Attempts to restart the heart by making an incision in the chest and massaging the vessel, or using defibrillators or pacemakers, may be futile unless there is a correct diagnosis of the heart condition. The cardiac monitor will give a continuous, instantaneous, visual monitoring of the rate and rhythm of the heart, indicating its condition and serving as a guide to attending physicians. *(Electronic Design, Oct. 15, 1957, p. 6)*

This piece is light on the circuitry, but it does give us a benchmark in the history of medical electronics.—**SS**

BACK TO SCHOOL

Data Communications and Networking provides a comprehensive update on today's newest datacom and networking techniques. During the course, attendees will receive an overview of modems, LANs and WANs, T1, TCP/IP, routers, and the Internet. The two-day course will be held in various locations throughout the U.S. The registration fee is $795. Contact Data-Tech Institute, P.O. Box 2429, Clifton, NJ 07015; (973) 478-5400; fax (973) 478-4418; Internet: http://www.datatech.com.

How To Produce Effective Multimedia Training gives an overview of managing production of a multimedia training project from initial assessment through roll-out. Using examples from case studies, each phase of production is detailed, including initial concept development, design, prototyping, media production, and programming for the alpha, beta, and final versions. The two-day seminar will be held Nov. 18-19 at The Westin Hotel, Chicago, Ill., and Dec. 11-12 at The San Francisco Hilton & Towers, San Francisco, Calif. Course fee is $795. Contact Influent Technical Seminars, 498 Concord St., Framingham, MA 01702-2357; (888) 333-9088; fax (508) 872-1153; Internet: http://www.influent.com.

A self-study course on Electromagnetic Compatibility (EMC)/Electromagnetic Interference (EMI) teaches approaches to modeling and understanding the sources of EMI; techniques of measuring EMI; procedures for measuring immunity to pulsed interferences; and useful practices to minimize EMI and improve EMC. The 14-lesson course includes learning objectives, reading assignments, and discussion topics. A self-testing quiz follows each lesson, and a final examination follows the course. Those who successfully complete the course will be awarded eight CEUs and a Certificate of Achievement. Price for the course is $349 ($279 for IEEE members). Contact the IEEE, Educational Activities Dept., 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331; (800) 678-4333; fax (732) 981-9667.

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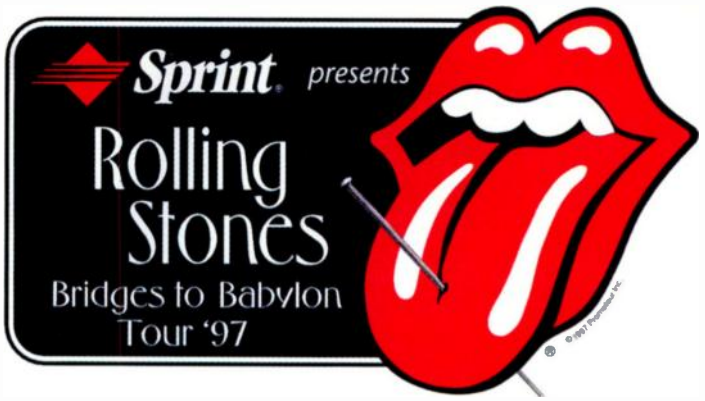

By the time this story is published, rock and roll legends The Rolling Stones will be embarking on their "Bridges To Babylon" tour, and will be appearing at a stadium or arena near you. Though you may think that the band is a bit too old to rock and roll (Mick Jagger just turned 54), they are (arguably) the number one musical act in the entire world. It is estimated that this latest tour will break all box office records (previously held by the Stones) and gross over $350 million.

Wait a minute! What's this doing here in *Electronic Design?* Shouldn't I be reading this in *Rolling Stone* or *Entertainment Weekly?* Well, yes, normally you would. However, you might be interested to know that Sprint, Kansas City, Mo., the global communications company, is sponsoring the tour. And according to company officials, this sponsorship offers them a number of ways to use the Stones' marketing muscle to raise its profile.

At an outdoor news conference held under the Brooklyn Bridge in New York City, William Esrey, chairman and CEO of Sprint, said that "the Rolling Stones and Sprint are a perfect fit. They (the Rolling Stones) were the original rock and roll rebels. Sprint is willing to break from convention and redefine telecommunications."

In conjunction with the tour, Sprint will implement a promotion geared toward new and existing business and residential customers. If you sign up for Sprint's long-distance service for your home or business by calling a special toll-free number [1-800-FALL-TOUR (325-5868)], you will be given an opportunity to purchase Rolling Stones concert tickets before they are offered to the general public. Fans can get the latest tour information by accessing Sprint's web site (http://www.sprint.com), and also get a chance to look at the company's product offerings and services.

At the news conference in front of more than 300 journalists and photographers, the band—Mick Jagger, Keith Richards, Ron Wood, and Charlie Watts—arrived in grand style in a red 1955 Cadillac convertible which Jagger himself drove over the Brooklyn Bridge (with a police escort) to the press area. The band talked about their plans for the tour and answered questions from the press as the conference was televised via satellite throughout the world.

"We're really pumped up, and we can't wait to get out and play," said Jagger. The band's new album, also titled "Bridges To Babylon," was released on Sept. 30.

For the opportunity to link themselves with the band, Sprint reportedly paid the Stones $5 to $6 million in fees. In return, the band will allow the company to market their products and services at the concerts and use the Stones' image and music in television and radio ads.

"The addition of the Rolling Stones tour to Sprint's sponsorship portfolio, which also includes the National Football League, will continue to help distinguish ourselves from our competitors," said Esrey. "Our sponsorship of the Rolling Stones will provide us with a high-profile marketing platform."

The North American leg of the tour kicked off in Chicago, Ill., on Sept. 23 will continue through next February. After a short hiatus, the band will make stops in the Far East and Australia before heading off to Europe.—**MS**

It's Only Rock And Roll

We here at *QuickLook* and the rest of the staff at *Electronic Design* constantly have to remind ourselves that engineers are people, too. Of course, you engineers have to remember that as well. In keeping with that spirit, here's a list of some upcoming dates and cities where the Rolling Stones will be appearing. Ticket prices range from $25 to $60. For complete information, check out Sprint's web site (see above).

Oct. 10—Hippodrome, Quebec, Canada
Oct. 12—Veterans Stadium, Philadelphia, Pa.
Oct. 16—Giants Stadium, East Rutherford, N.J.
Oct. 20—Foxboro Stadium, Boston, Mass.
Oct. 23—Jack Kent Cooke Stadium, Washington, D.C.
Oct. 26—Vanderbilt Stadium, Nashville, Tenn.
Oct. 28—Owen Field, Noman, Okla.
Oct. 30—University of New Mexico, Albuquerque, N.M.

Additional dates may be added during the tour.—**MS**

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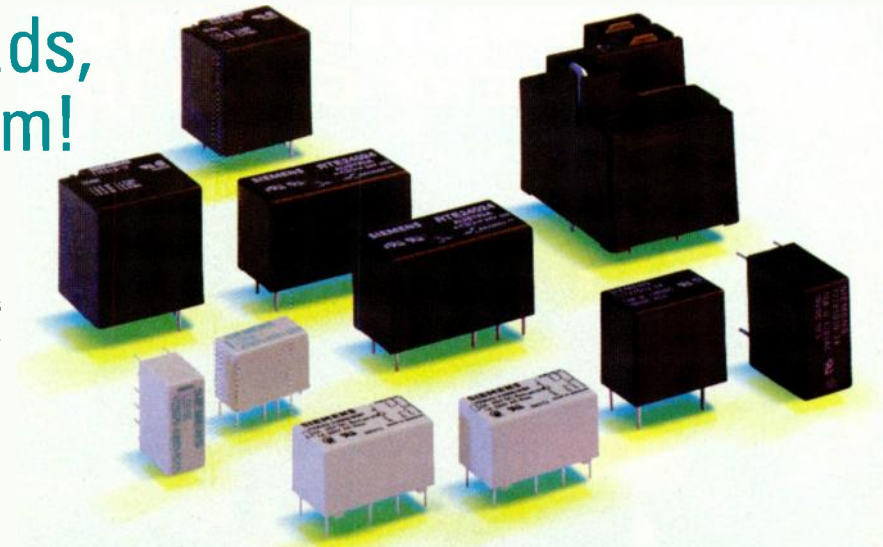

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HOT PC PRODUCTS

The Newton Message Intercept Kit is a PC card pager receiver and software tool package targeted toward mobile communications users. Socket Communications' newest offering is support for the Newton MessagePad for the PageCard SDK. Specifically, the kit eases the work of creating wireless applications for mobile users.

With the PageCard SDK, programmers can use the world's largest digital wireless network to send information from Windows networks to any alphanumeric pager or PageCard SDK. The SDK allows users to download wireless data from mobile computers like the Message Pad. Various applications can benefit from the new software developer's kit: wireless e-mail, webcasting updates, calendar changes, stock market quotes, sales leads, service dispatches, health care, finance, and real estate.

Functions such as API, run-time Dynamic Link Libraries, and C/C++ and Visual Basic header files are included with PageCard SDK. These functions will help develop and test page-enabled Windows 95 and NT applications that convert data into wireless messages. To save users fees associated with simulating wireless pager networks, a TAP simulator with customizable carrier profiles is included for developers.

Taking advantage of Newton's new architecture for wireless messaging, the Newton Messaging Enabler, Socket Communications has endowed the PageCard SDK with the PageSoft Receiver for Newton. The receiver uses the enabler to send wireless messages to the MessagePad InOut Box or to custom programs. Developers can fashion their custom programs via the NewtonScript application generator. Sample NewtonScript programs are included with the PageCard SDK.

The PageCard SDK is packaged with sending libraries for Windows 95 and NT; PageCard download libraries for Newton, Windows CE, 95, and NT; two PageCard receivers; and two months of wireless service. The new software developers' kit is priced at $599.

For more information on the PageCard SDK, contact Socket Communications, 37400 Central Court, Newark, CA 94560; (510) 744-2752; fax (510) 744-2727; Internet: http://www.socketcom.com.

The TransPort XKE is the latest in Micron's line of notebook computers. The powerful new notebook packs the optimum desktop experience into a portable medium for a reasonable price. Micron Electronics has an extensive line of PCs for consumer, business, government, and educational use.

TransPort XKE's communications features such as full-duplex telephony, direct connectivity, and AutoPlay allow users to connect their cellular phones directly to their notebooks, search for information on the Internet, and conduct video conferences from mobile locations. AutoPlay, the 20X modular CD-ROM drive lets users hear their compact discs without powering up their notebooks.

Other features include SoundBlaster with 16 bit stereo, built-in hardware wavetable, and 3D spatializer; built-in stereo speakers and microphone; and S-video and NTSC video out capability.

Standard features of the TransPort XKE are 166-MHz Mobile Intel Pentium processor with MMX, 512-Kbyte L2 pipeline burst cache, PCI bus with 128-bit graphics accelerator, 2 Mbyte EDO DRAM, Pick-a-Point dual pointing devices, Universal Serial Bus interface, Motorola 33.6-kbits/s fax/modem with full duplex telephony (free upgrade to 56.6 kbits/s when available), CardBus-ready, zoomed video-ready, two infrared ports (front and rear), built-in game port, two modular expansion bays, Microsoft Office 97 SBE CDs, built-in Desktop Management Interface support, and a five-year/three-year Micron Power limited warranty.

With the optional MicronExecutive option, users can purchase a matching black 17-in. monitor, mouse, keyboard, and MicronDock multimedia port replicator. The MicronDock has a built-in battery charger, and supports hot docking. The TransPort XKE starts at $5149.

For more information, contact Micron Electronics, 900 E. Karcher Rd., Nampa, ID 83687; (208) 893-3434; fax (208) 893-3424; Internet: http://www.micronpc.com.

Palm Postage, from Postal Electronics, is a handheld, portable franking device that will issue stamps of all national post offices and major courier and shipping companies. The N.J.-based company recently received a patent for their digital postage system, Postage Mate. A PC-based software platform will be available before the end of 1997.

Previously, mailrooms had to lug portions of their postage machines to regional post offices for certification or other inconveniences. Additionally, most companies have at least one account with a major carrier such as UPS or Federal Express. Now, all

an enterprise has to do is connect with Palm Postage.

The system works through standard telephone jacks and computer networks, and uses an ac adapter or batteries for a power supply. Because the U.S. Post Office requires that all new franking devices operate digitally by 1994, and that every franking machine work digitally by 2004, those using PalmPostage will be ahead of the game. As a result, up to 1.5 million postage machines will be replaced over the next seven years.

For more information, contact Postal Electronics, 30-34 Okner Pkwy., Livingston, NJ 07039; (201) 740-9283; fax (201) 740-9422.

Distributors Take A Hit In UPS Strike

Among the many groups happy to see those big brown trucks back on the road are electronic distributors. The 15-day Teamsters Union strike at UPS caused an average weekly loss of $124,705 to members of the National Electronic Distributors Association (NEDA), who responded to the group's fax survey sent out August 13.

The total weekly loss was $9.85 million, but that figure will likely go much higher because many companies were unable to calculate losses immediately, according to the NEDA. Overall, 71.4% of respondents said the strike interfered with their shipments. The association received 162 responses (45.8%) from 354 surveys sent out to it members, which represent nearly 95% of products handled through distribution channels.

The strike had a major impact on 66.25% of respondents and a minor impact on 23.75%. A total of 7.5% said the strike's impact was devastating. Because of the strike, distributors increased prices to cover added costs (44.35%), reduced work forces or hours worked (18.26%), or shut down operations completely (5.22%). Even companies that said they were not seriously affected by the strike reported that new business had slowed. Many firms had to use sales personnel to deliver product instead of generating new business.

"It is too soon to assess the long-term impact of the strike," noted NEDA executive vice president Robin B. Gray Jr. "The strike just ended today [August 22] in the Chicago area and other distributors whose packages have to go through the Chicago hub have continued to be affected." Approval of a local contract in Chicago prolonged the strike there.

Most problems involved shipping product to customers (91.98%), but receiving product from suppliers also was high on the list of adverse effects (86.42%), as was increased shipping cost (85.19%). A decrease in customer orders was reported by 48.77%, 32.1% reported administrative problems, and 23.46% experienced problems with delivery of office consumables.—**John Novellino**

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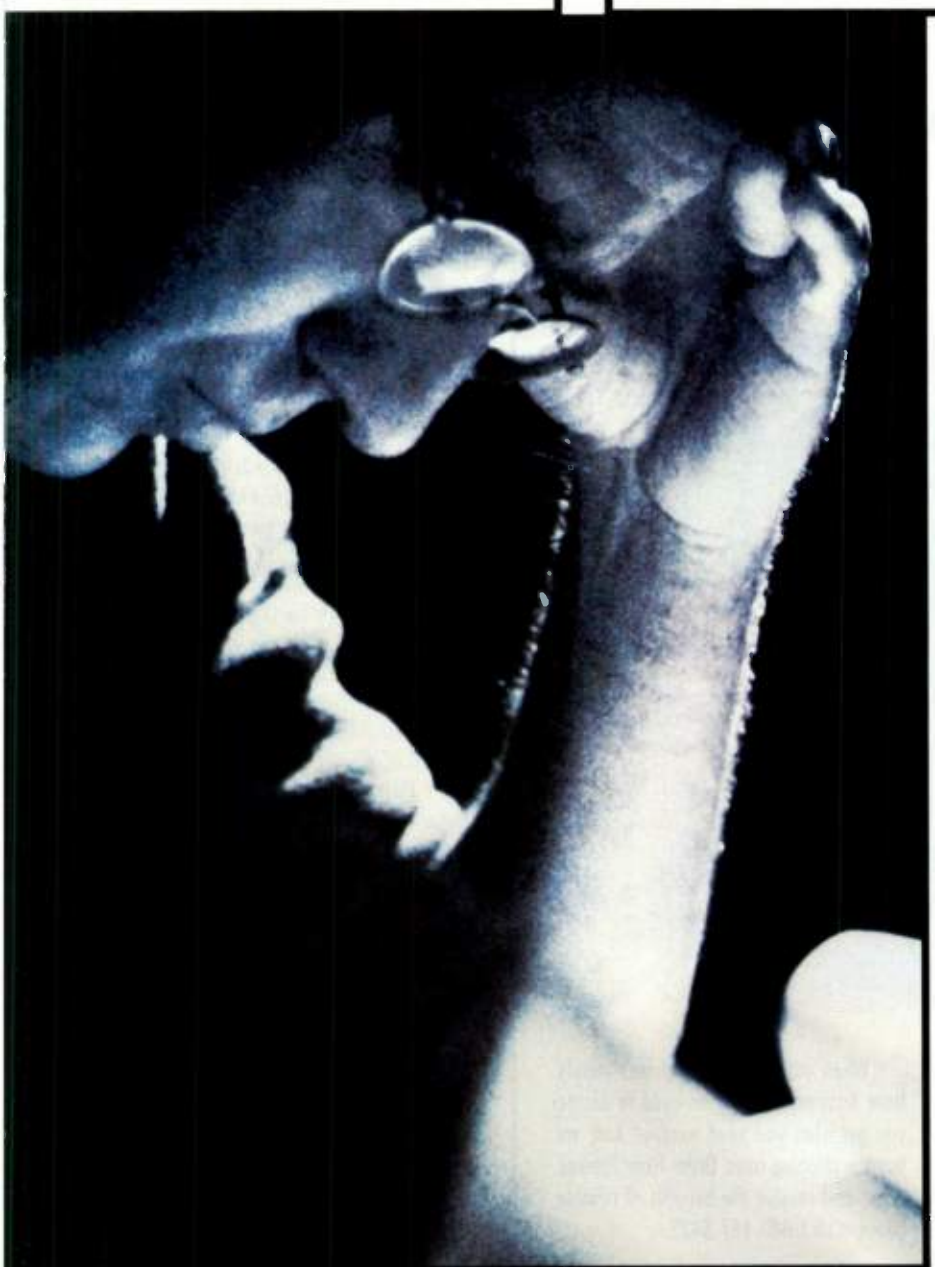
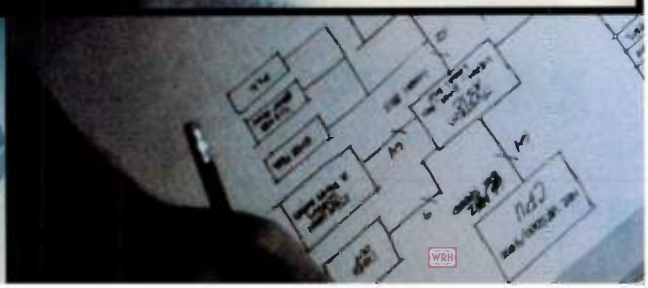
Chipset Support	Yes	Yes	Yes	Yes
Feature Highlights	5 Ch. DMA Controller RAM/ROM Controller Serial Interface IrDA™	Soft Modem 4-mode PMU 10-bit DAC/ADC Single-cycle MAC	High-perf. MMU, Single/ Double Precision FP *Ideal for high-performance embedded applications*	400 MFLOP FPU L2 Cache controller Two-way superscaler pipeline





V_R4101. Created for Windows CE products, it offers ultra-low power and incredible MIPS per Watt.

V_R4102. Offers Windows CE hand-held computers tremendous power and performance in a high-integration system on a chip.

V_R4300. A high level of performance. An extremely low price. Ideal for office automation, video games & X-terminals.

V_R5000. For advanced applications like internetworking it provides the ultimate performance at an incredible price.

NEC

READER SERVICE 185

JUST 4 THE KIDS

If you didn't already know, America's favorite dog isn't Lassie anymore. Wishbone, the Nineties answer to Clifford, reaches over eight million kids a week via PBS. Now, kids between the ages of 6 through 12 have a new way of expressing how much they like the canny canine through Wishbone Print Tricks by Big Feats! Entertainment. Software publisher Palladium Interactive made sure that the CD-ROM also includes a fully integrated Internet component.

The program is a hybrid Windows/Macintosh print utility that's compatible with PrintShop, PrintMaster, Print Artist, and Corel Print House, among others. Wishbone Print Tricks also comes with official photographs and drawings of the publishable pup. Kids can place these graphics in banner and greeting card projects included in the software.

Over 20 print projects are on the CD-ROM. Each of those projects includes 12 preproduced templates that feature graphics and text that the character would say. The templates can be used "as is" or edited to suit the child's needs.

Other projects that may be pursued with the Wishbone Print Tricks CD-ROM are signs, stationery, certificates, framed pictures, electronic postcards, placemats, bookmarks, and posters. Graphics from other sources also may be imported into projects for more personalized works.

The Internet component of the CD-ROM takes users to the Members Only World Wide Web site. The kids need only use a standard web browser and an Internet connection. Once at the site, the kids can make the most of special print options that can only be found on-line. If parents do not already have an Internet connection, Print Tricks also offers a complete on-line solution.

Electronic postcards may be selected, customized, and mailed from the site, as well. Kids can electronically flip the postcards over to post images on the front and their message on the back or inside. There's even an option to put Wishbone's voice on the card via sound clips available at the site.

Also at the site, kids can download art Theme Packs which offer several new Wishbone images for particular holidays and events. They're updated and timely, so no Santa Wishbones in March.

Wishbone Print Tricks is priced at $19.99. More information about Wishbone can be found at *http://www.wwwishbone.com*.

Contact Palladium Interactive, 900 Larkspur Landing Cir., Suite 295, Larkspur, CA 94939; (415) 464-5500; fax (415) 464-5530; Internet: http://www.palladium.net.—DS

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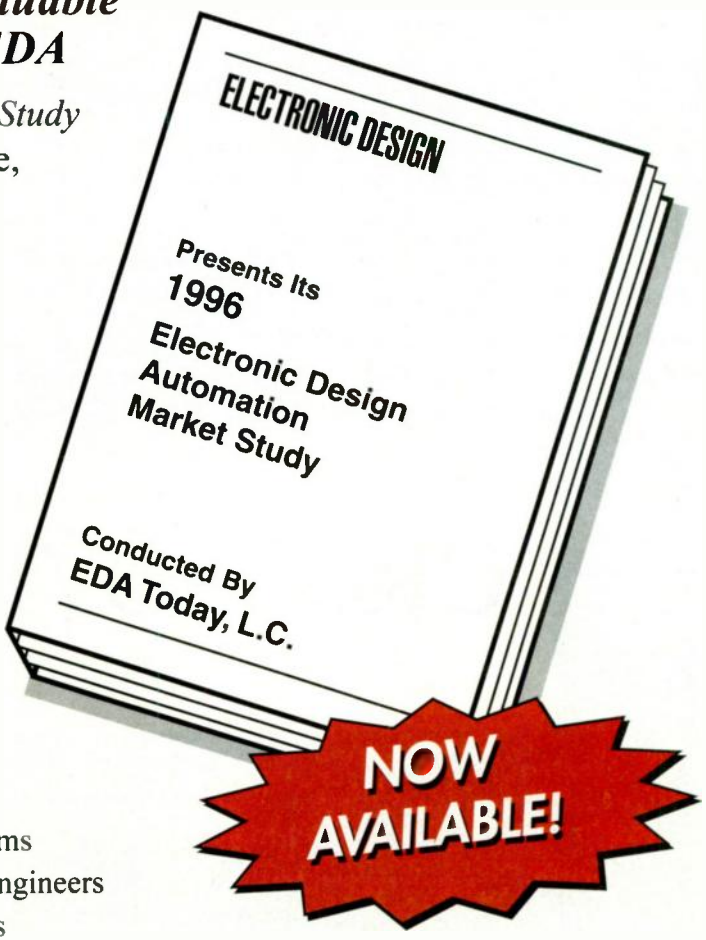
The Results Are In! An invaluable study for those involved in EDA

The *1996 Electronic Design Automation Study* sponsored by *Electronic Design* magazine, provides critical survey information with a focus on EDA marketing executives and user/engineers. Conducted by the market research firm, EDA Today, L.C., results have been compared, compiled, and studied to serve as strategic marketing opportunities for suppliers.



Survey results will present information on:

- The respondents, types of jobs and designs, size of design teams, budgets, and companies
- Platform trends, hardware and operating systems
- Internet and web usage trends among design engineers
- Spending patterns: budget increases, decreases
- Cross tabulation results on significant issues ocurring in the EDA industry
- Design trends of IC, ASIC, board-level/system-level design, and programmable logic

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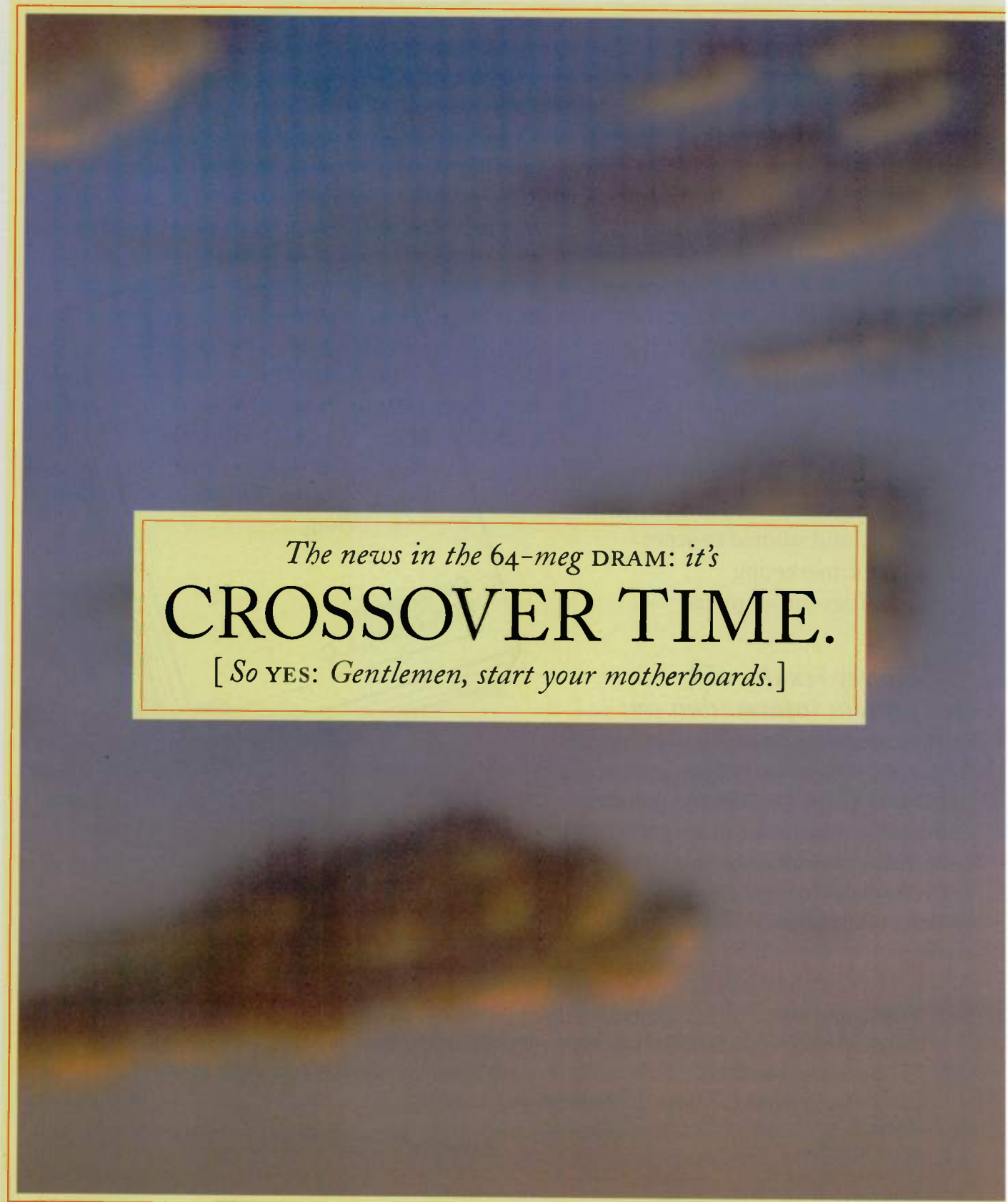


The news in the 64-meg DRAM: *it's*

CROSSOVER TIME.

[*So* YES: *Gentlemen, start your motherboards.*]

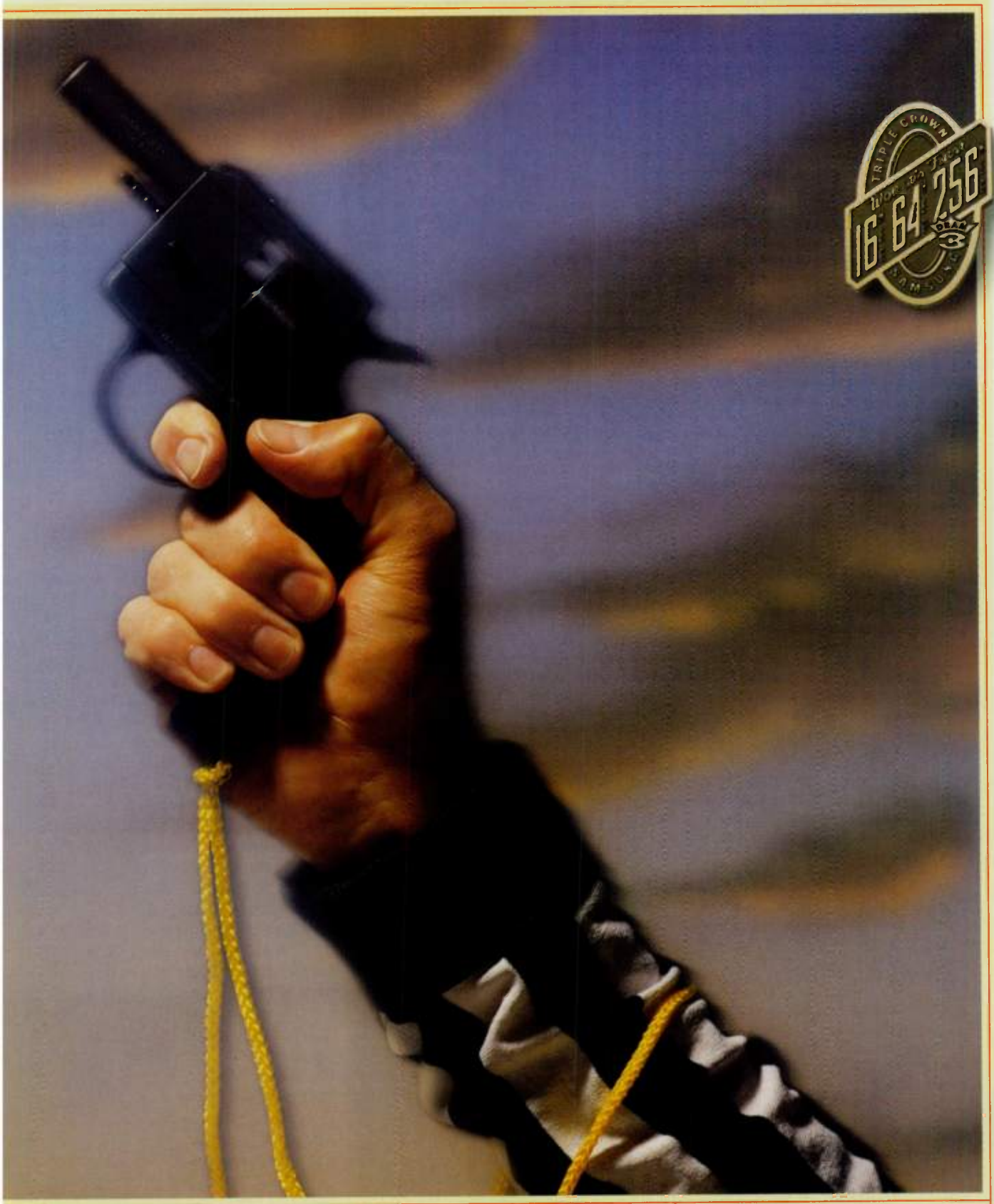
When something as important as DRAM crossover is ready to happen, you want to be prepared.

And what we have to tell you is exactly that: it's ready to happen.

Which means you're going to be able to capitalize on the competitive advantage the 64-meg can give you.

But only if you are in fact prepared. Designed in, ramped, ready to go. With your motherboards started.

Because like most races, this one belongs to the swift.



And speaking of swift, the people you want to turn to for crossover are the leaders in memory, in DRAMs, and of course in the 64-meg. Samsung.

For 64-meg data sheets, call 1-800-446-2760 now. We'll shoot them off to you right away. Or you may visit us at our Web site, at www.sec.samsung.com.

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Still A *Generation* Ahead.

READER SERVICE 147

Y2K UPDATE

In anticipation of the Year 2000 Date Change (Y2K), new companies are being formed to handle code changes, established companies are adding Y2K compliance to their roster of services, and news outfits are predicting widespread panic. There are now thousands of "solutions" available for compliance-seeking enterprises. There also are equally as many services available to come in and perform the conversion for the enterprise. But, as far as information about which software or hardware is compliant goes, there appears to be a deficit. Except for one source, Indelible Blue.

Indelible Blue's web site *(http://www.indelible-blue.com/ib)* features a great resource for federal, state, and local government; large corporation; academic; and small business computer hardware and software buyers. Specifically, Indelible Blue offers the Volume Incentive Program (VIP). Within VIP is VIP Online which features the latest Y2K compliance information on all IBM and Lotus products.

To get there is a bit tricky, though. When you point your browser to the address above, you land at the welcome page. Click on Volume Incentive Program (at the left) to get to VIP. The first entry on the VIP page is "VIP Online," click on it. The next page asks you for a password; skip that and click on "IBM/Lotus Catalog" (also on the left). The next page offers a few options, the most important for us is "Year 2000 Compliant Products." After clicking on the Y2K link, you'll be brought to a list. I recommend expanding the list right away to see all the products at once.

The IBM list includes Application Development, Data Management, e-Business, Java, Networking, Operating Systems, Systems Management, and Transaction Processing software. Lotus' list shows cc:Mail, Domino/Notes, e-Business, Java, SmartSuite, and Other (includes NetObjects Fusion and WebRunner Toolkit) as the links.

I decided to do some research and I clicked on PC DOS. The link took me to a brief description of PC DOS v7. Also on the page is a link to more information and a pricing chart. There are two pricing versions—20% Price and 45% Price, depending on the volume purchased.

Typically, finding this kind of information regarding compliant products is time consuming and trying on the nerves. With Indelible Blue's VIP Online, buyers get a quick look at pricing, as well as finding out which new products are Y2K compliant, saving you valuable research time and effort.

For more information, contact Indelible Blue Inc., 3209 Gresham Lake Rd., Suite 135, Raleigh, NC 27615; (919) 878-9700; fax (919) 878-7479.

Of the "solutions," most usually only handle one kind of code conversion such as COBOL. ConSyGen's toolset, ConSyGen 2000, handles conversions on BULL, IBM, UNISYS, PC1, PC2, and now, Hewlett-Packard 3000 systems. ConSyGen's conversions take place either at the company's conversion factory or on-site with ConSyGen professionals.

Sending the stock market into a frenzy, ConSyGen recently announced that it had completed and tested a 1.4-million-line conversion on Hewlett-Packard's 3000 system. The big news was that the conversion took less than a day to complete. Currently, the company expects to convert two million lines of code per day.

The automated toolset works by cataloging the code into a database, analyzing the code, producing reports, and converting the code. The reports show each date occurrence, allowing the conversion managers to set the rules for the final conversion. After all the preliminary work is finished, the conversion takes only a matter of hours.

This particular project of over a million lines of uncompiled COBOL code comprised approximately 4000 original source-code modules. In the code were over 96,000 date references. These references were all translated by the toolset.

For more information, contact ConSyGen Inc., 10201 S. 51st St., Phoenix, AZ 85044; (602) 496-4545; fax (602) 496-9889; e-mail: rbishop@consygen.com.

One of the more valuable certifications available in the Y2K arena is ITAA's 2000 Certification. The Information Technology Association of America is an 11,000-member strong organization that deals with such subjects as taxes, intellectual property, telecommunications law, encryption, securities litigation reform, and human resources policies. ITAA's certification program gives companies a third-party evaluation of their Y2K processes and methods.

The 2000 Certification Program first asks enterprises to reply to an in-depth, technical questionnaire. Eleven prime areas are covered on the questionnaire: assess situation, analyze candidate solution, ensure quality, integrate systems, manage configurations, monitor and control technical effort, oversee and manage acquisitions, oversee and manage subcontracts, plan technical effort, reengineer product/data, and verify and validate systems.

Many of the questions in each section require supporting documentation. Companies will be asked about all of their products and services. Applicants pay a fee of $250 for the questionnaire. Processing and review of the questionnaire is priced at $8200, with a $1000 discount for ITAA member companies.

When an organization is certified by ITAA, they are immediately entered into an Internet-based database of companies who've earned the certification. Certified companies also are recognized in the "ITAA Directory of Year 2000 Solution Providers." And, of course, the ever-so-important camera-ready certification mark is awarded to certified companies, suitable for advertising, packaging, and other materials.

Companies that don't cut the mustard the first time can reapply for a fee of $3500.

For more information, contact ITAA, 1616 N. Ft. Meyer Dr., Suite 1300, Arlington, VA 22209; (703) 284-5333; fax (703) 525-2279; Internet: http://www.itaa.org.—**DS**

Looking for Consultants?

IEEE-USA's Directory of Electrotechnology Consultants is a must for any company or institution that uses technical or management consultants. The **Directory** lists independent consultants who are operating as sole practitioners or in small businesses and also gives detailed information regarding specific areas of expertise.

Prepared by the Coordinating Committee of the Alliance of IEEE Consultants' Networks, the **Directory** is available as a searchable database on the Web at <http://www.ieee.org/usab/DOCUMENTS/CAREER/AICN/dbform.html>.

Or, for a free hard-copy version, contact Bill Anderson at:

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KMET'S KORNER

...Perspective on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

Two engineers in the front seat, headed northeast on 99W for Portland. Good open road, not a cloud in the sky, with the temperature just right, Mount Hood stands majestically in the distance—a perfect setting for stimulating conversation. Somehow the topic of engineering productivity emerged. My friend and his team of engineers were once again been tapped on the shoulder and told they needed to get product out faster for less money. He described his work environment and how they were doing it. He first described a typical day at work, one spent in service to e-mail, voice-mail, physical mail, desk-based phone, pocket pager, groupware tools, project intranet tools, members of the project team, management, and, finally, to doing his assigned job. See if this mirrors your own situation.

RON KMETOVICZ
CONTRIBUTING EDITOR

His day begins with a reading of e-mail collected overnight because the last act performed before going home was to clear the in-box. He reports that some messages fall into the garbage category, but most retain a high degree of importance. Project-team members generate messages either from work or home. Some responses take little time; others require hours to resolve.

Next, voice-mail demands attention. A blinking red light on the phone makes this need known to my friend's total state of being—the light must be extinguished. But my friend says he has a trick to keep its persistent demands from his conscious mind; he places a rubber cap over the lens to completely block its transmission of productivity robbing photons. The cap goes on upon going home and comes off only after the e-mail is done.

Here again, messages come in only from those working late or from others in different time zones.

Attention shifts to the physical mail. My traveling partner confessed that e-mail, voice-mail, and other labor-saving appliances don't reduce the stack of physical artifacts received each day.

Many engineers in my friend's work environment use a company-supplied meeting-scheduling tool. The tool lets anyone who wants to call a meeting schedule your attendance without your prior knowledge, much less approval. My front-seat companion tried this madness and now refuses to participate. The only way you can get him at a meeting is by prior contact and discussion. He does, however, consult a personal tool to refresh his memory on the meetings he's agreed to attend.

Groupware and intranet activity demands immediate attention. Progress and status reports must be updated at the end of each day for team and management consumption. He places the information on the 'Net, but doubts it being effectively utilized as measured by the e-mail, voice-mail, and other communication that continues to flow.

Some time appears to work on the assigned task, but wait, new input continues to arrive and it must be serviced. Around 3 or 4 in the afternoon, calm returns. It's time to go to work!

Sadly, my friend and his coworkers get new products to market faster and for less money by working longer for the same pay while enduring extreme organizationally imposed hardship. There must be a better way!

To obtain an e-mail copy of "The Complete List for Late Product Information," readers may contact Mr. Kmetovicz at kmetovicz@aol.com.

THE ENVELOPE, PLEASE

The nature of an entrepreneur is, by definition, one of a risk taker. In order to start up a business, an entrepreneur must assume all responsibility for that business, whether it succeeds or fails. But, there are those entrepreneurs who stand out, who shine brighter than the rest because their business not only thrives, but keeps the employees that it had in the beginning.

In Arizona, these folks are recognized with the Master Entrepreneur of the Year award from Ernst & Young, LLP. This award is given to those individuals who perform highly in a variety of areas. These areas include: strong financial performance, continuity of management team, management excellence over a sustained period, and innovation in the running of a business.

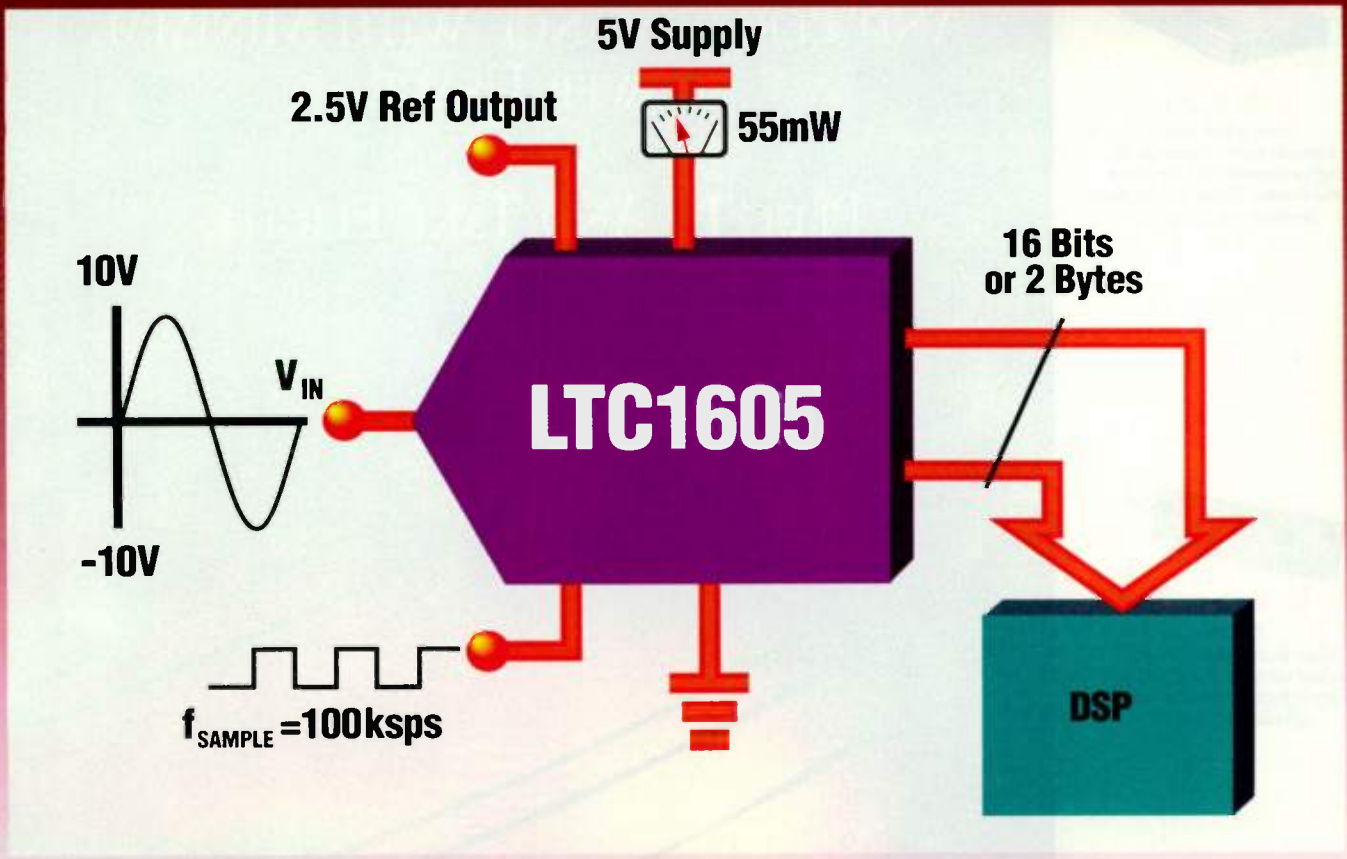
This year's Master Entrepreneur of the Year is James N. Farley, chairman of SpeedFam International. Farley attributes his success as an entrepreneur to his supportive employees and his president and chief executive officer, Makoto Kouzuma. He describes Kouzuma as, "my right-hand man." Farley will be inducted into the Entrepreneur of the Year Institute in November, and will be in the running for the National title.

Farley joined SpeedFam International back in 1960 as a business manager. He rose through the ranks to vice president of sales, and on to president from 1967 to 1993. In 1993, Farley was appointed chairman and chief executive officer by the board of directors. The company credits Farley for developing the worldwide organization. Currently, the chairman develops and directs the future strategy of SpeedFam International.

According to the company, SpeedFam manufactures 85% of the world's surface processing machines used in semiconductor wafer manufacturing. It also is responsible for 50% of the thin-film memory disk media market. The company also has begun to enter the chemical-mechanical polishing system market, specifically the semiconductor device sector.

For more information, contact SpeedFam at (602) 705-2100; Internet: http://www.speedfam.com.—**DS**

16-Bit, 100ksps ADC

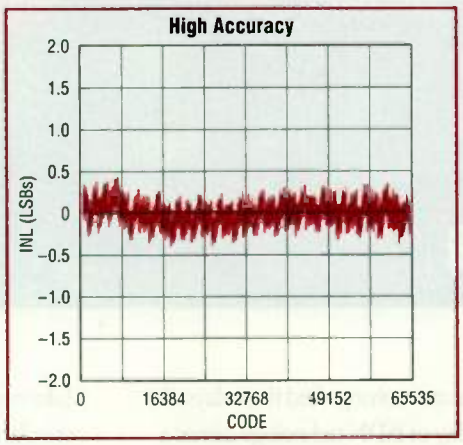


LTC1605: Draws only 55mW from single 5V supply.

The LTC1605 is perfect for low power industrial, instrumentation and data acquisition applications. This low cost ADC guarantees high accuracy without messy autocalibration. The robust analog input has a ±10V industrial input range with overload protection for harsh environments. The LTC1605 has a 16-bit or 2-byte parallel output and is available in the industry's smallest footprint: 28-pin SSOP.

Features

- 16-Bit, No Missing Codes
- ±10V Input Range and 5V Supply
- ±20V Overload Protection
- Reference and Sample-and-Hold On Board
- Pin-Compatible with ADS7805 and AD976
- 28-Lead DIP, SO and SSOP Packages
- $18.00 for 1000 Pieces



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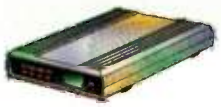

ISDN Modem

Travel at high speeds. Motorola semiconductors are the high-performance fuel that power digital modems. Taking you just about anywhere you want to go.

PC Add-In Card

Plug it in. Motorola semiconductors drive the cost out of ISDN PC cards to make high-speed internet access an affordable alternative.

Personal Router

Catch the wave. Motorola's EN302 and QUICC™ communications processors & transceivers power personal routers so you can manage your home office network and surf the Internet to catch the latest wave of information.

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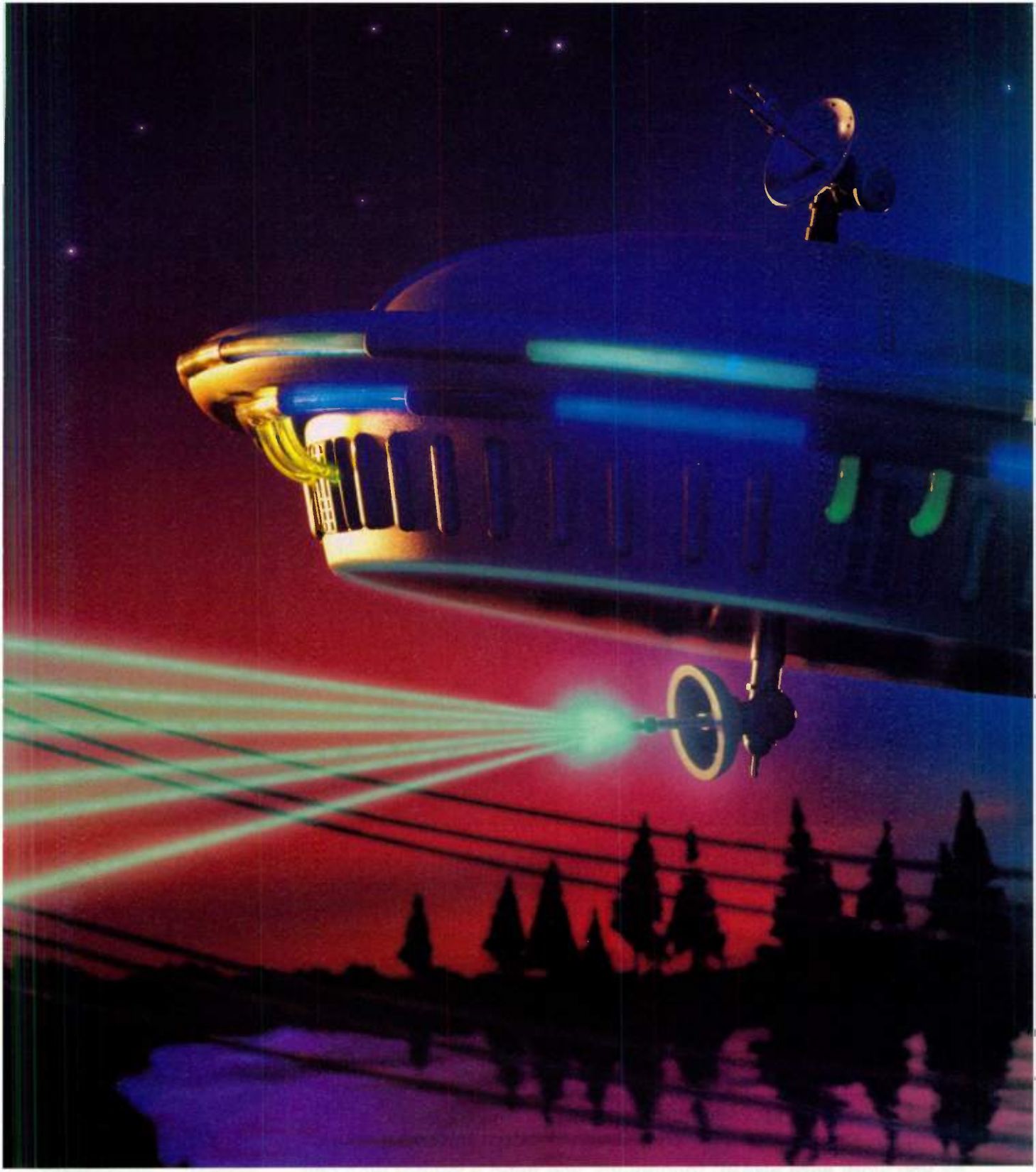
Communications are evolving. And these days, the speed and reliability of ISDN technology carries a multiplicity of information that buzzes around the earth. That's where Motorola's ISDN system level solutions come in. We offer a broad portfolio of products to satisfy your needs on a global scale.

Like our family of communications processors and standards-compliant, single-chip NT1, U-transceivers and S/T-transceivers that give your designs the furthest reach with minimal power consumption. So this new standard of systems integration gives you the opportunity to take your designs



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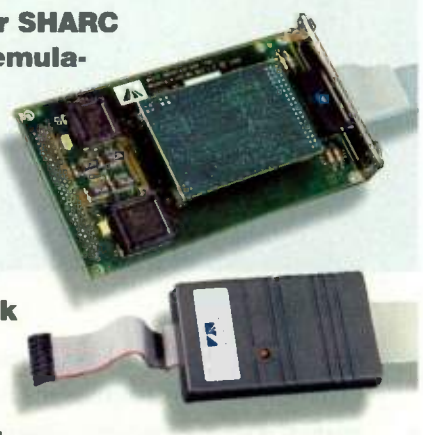
WHITE MOUNTAIN DSP

Two Rules For SHARC Infested Waters: 1. Get The Right Tools 2. Swim With A Buddy. To Do Both, Call White Mountain DSP.

The ADSP-2106x family of SHARC DSPs from Analog Devices provides a new species of DSP. With its 120 MFLOPS of processing power, six link ports for interprocessor communication, and up to 4 Mbits of on-chip memory, it can bring your application to the cutting edge. But swimming with SHARCs can be a dangerous proposition – unless you have the proper tools. That's where White Mountain DSP comes in.

White Mountain DSP offers a full emulation and debug tool set for SHARC development. Another first in the industry, the Mountain-ICE/WS emulation system for Sun workstation platforms (shown) provides complete multi-DSP debugging support for both the ADSP-21060 (4 Mbit) and ADSP-21062 (2 Mbit) SHARC devices. And you know White Mountain DSP will continue to expand its range of options to enable you to work with SHARCs and not get bitten.



As you work with SHARC technology, you need a vendor who can support and enhance your efforts. At White Mountain DSP you talk directly with experts who provide the appropriate technical support before you get in too deep.

Phone 603-883-2430 or fax 603-882-2655 today for more information, or contact us via e-mail at *info@wmdsp.com*.

White Mountain DSP, Inc., 20 Cotton Road, Nashua, NH 03063 (603) 883-2430 Fax: (603) 882-2655 E-mail: *info@wmdsp.com*

READER SERVICE 159

Merged Embedded Controller And DSP Designs Simplify Systems

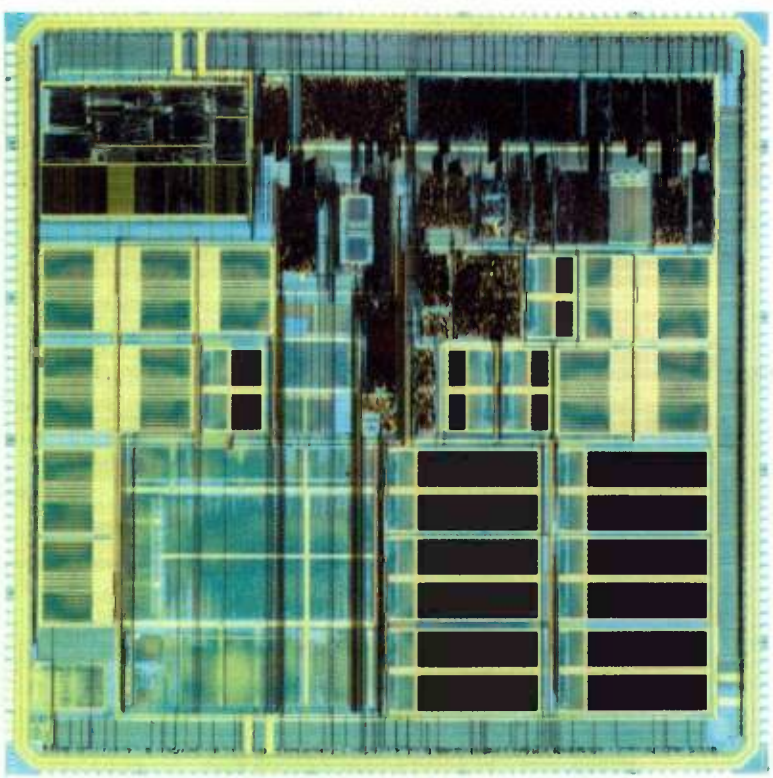
Adding DSP Support On Microcontrollers (Or Vice Versa) Provides More Efficient Silicon And Lowers System Costs.

Dave Bursky

SPECIAL REPORT

The need for many systems to perform both control and signal-processing operations has led to a proliferation of embedded controllers and digital-signal processors (DSPs) working in tandem. The multiple-processor solution, now in use in many systems, can muster sufficient processing power in most cases, but the multiple chips often require more complex programming, consume more power, occupy more board space, and often duplicate on-chip resources.

Coming to the rescue are more highly integrated solutions that combine control and DSP functions on the same chip, saving power, space, resources, and simplifying programming. Depending on the complexity of the DSP or control operations to be executed, designers have several integrated alternatives to the multichip solution. These include microcontrollers with some DSP computational support added to architecture (or conversely, DSP circuits with controller features and peripherals), highly integrated chips with embedded controller and DSP cores co-resident on the same chip, fully merged DSP and controller architectures into a single processing engine, and full custom solutions assembled with design library building blocks.



Art Courtesy: GEC Plessey Semiconductor

The addition of some hardware, typically a multiplier or multiplier and accumulator, is the least costly answer because it can leverage the design of an existing microcontroller, and then add just a little bit of logic. In the case of an MCU, designers of the controller would typically add hardware multiplication support so that it can more rapidly perform the signal-processing algorithms used in applications such as servo loops and modem subsystems.

One of the first to add such hardware, Motorola, did so back in 1990, by including multiplication support on its 68HC16 MCUs. The chip performs a 16-by-16-bit multiplication and 36-bit accumulation, which can be used for adaptive filtering, and many other algorithms. Many other MCU and embedded processor manufacturers have since followed suit. Some of the latest include the M32R/D from Mitsubishi, a 32-bit RISC processor with a 16-bit two-cycle MAC and 16 Mbits of DRAM on a single chip; and the SH processor family from Hitachi, which has a 32-bit data path, but 16-bit instruction words for high code efficiency.

A fully parallel MAC requires a considerable amount of silicon area on the already area-conscious microcontrollers, so to reduce the area and minimally

increase chip cost, the word size of the multiplier can be reduced. The penalty is reduced throughput because the multiplier in the MAC must be cycled several times to get the desired result. Although this approach reduces the multiplier performance, the dedicated hardware is still several times faster than the simple shift-and-add operations executed by an ALU for multiplication and accumulation.

When the performance of MCUs with on-chip MACs can't deliver the throughput needed for more demanding algorithms, designers can turn to higher levels of integration that co-integrate the microcontroller and DSP cores on the same chip. Because the cores share the same silicon, wide, high-speed buses can be integrated on the chip to allow rapid data transfers between the two blocks, or between the blocks and the on-chip memories, eliminating some data bottlenecks. Additionally, some of the on-chip memory or logic can be shared between the two processors, allowing a reduction in the total amount of on-chip memory or logic required.

Combined Functions

This multiprocessor approach has been used by several companies. Zilog has a family of Z8-based microcontrollers that include DSP cores. Motorola developed a chip that combines a 68k-series CPU and a 56000-family core on the same chip (the 68356). Advanced RISC Machines (ARM) and Hitachi have developed processors that incorporate DSP blocks that supplement the controller, the Piccolo and the SH-DSP, respectively. Still other companies such as Lucent Technologies, SGS-Thomson Microelectronics, The DSP Group, and Texas Instruments offer DSP cores that can either be licensed, as is the case with Oak and Pine cores from The DSP Group, or used as part of the firm's ASIC design library for a custom solution.

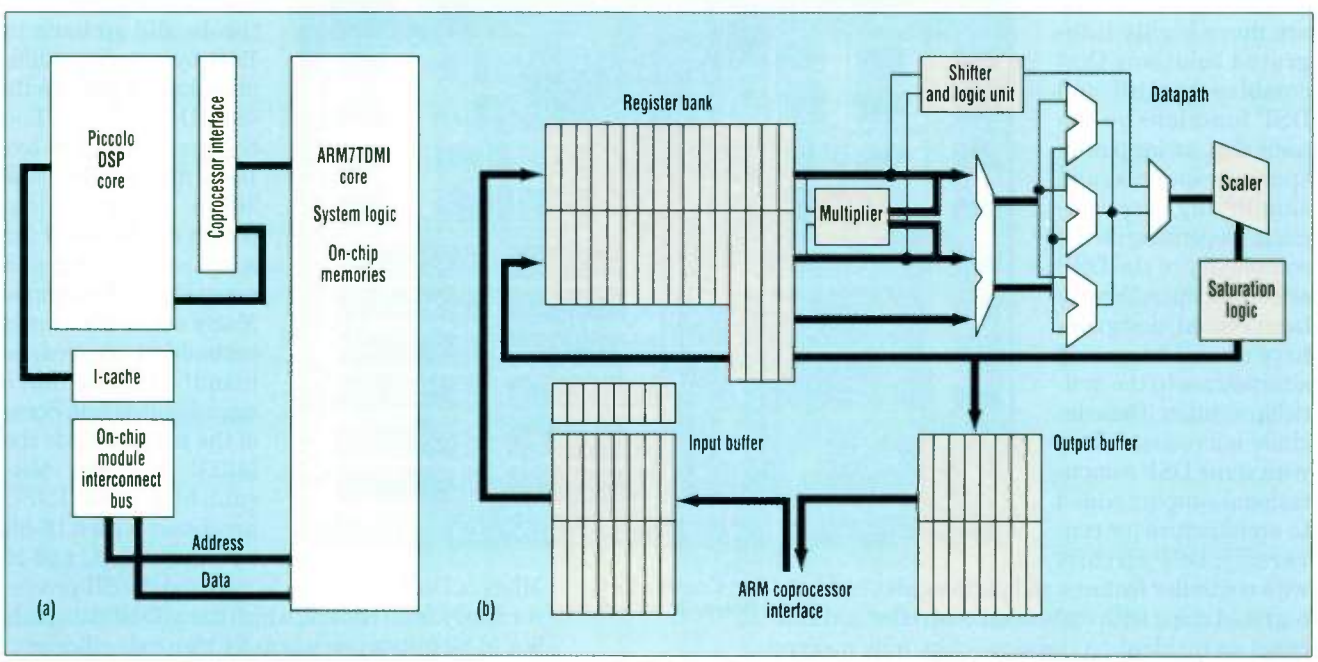
It's also possible to start with an embedded controller core and add DSP features. Licensees of the ARM core, for example, have added their own DSP capabilities. GEC Plessey, for example, released a chip earlier this year, the GEM310, that combines the ARM7TDMI (Thumb) 16/32-bit core and an Oak DSP core the company licensed from The DSP Group. The combined functionality and additional resources integrated on the GEM chip suit it for GSM telephony applications. Both cores are part of GEC's ASIC design tool suite and can be used to implement a custom controller/DSP system on a chip.

Another ARM licensee, VLSI Technology, also co-integrates the Pine or Oak DSP cores along with ARM6 or ARM7TDMI cores. The latest version, the WS3670, includes the ARM7TDMI core with a 1-kword by 16-bit direct-mapped instruction cache, an Oak DSP core, a codec, and a 1-kword by 16-bit instruction cache. Additional resources include an interrupt controller and phase-locked loop. Each core can also run at a different frequency, depending on their repsective processing loads, delivering a combined performance of 150 MIPS.

In the MIPS-architecture licensee camp, Integrated Device Technology was the first to add hardware multiplication support to the MIPS processor. And, as part of its CoreWare ASIC program, LSI Logic offers the MIPS core and various DSP building blocks *(see "Creating A Custom DSP/Control Solution," p. 78.)*

Similarly, designers at SGS-Thomson Microelectronics have used their own 32-bit ST-20 processor core, and on the same chip integrated a special 12-channel global-positioning system DSP block. Additional functions incorporated on the ST20-GP1 chip include 4 kbytes of SRAM, an interrupt controller, two serial ports, a real-time clock/calendar, programmable I/O lines, and a programmable memory interface that supports off-chip RAM, ROM, and flash memory.

SGS also has a proprietary 16-bit DSP core, the D950, which performs single-cycle 16-bit multiplication and accumulation, and packs 40-bit accumulators to minimize rounding errors. The core



1. Merging Advanced RISC Machines' ARM7TDMI RISC processor core and its Piccolo DSP engine on the same chip allows systems to perform control and DSP operations with maximum efficiency (a). In the Piccolo core, a large register bank and four wide accumulators provide the multiplier with two operands every cycle. At the end of the data path, a scaler can adjust the final result, and saturation logic will help normalize the output (b).

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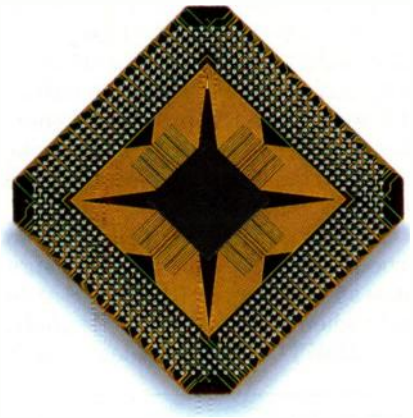

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mold and uses a 32-bit instruction width for the DSP commands. The wider word allows a 32-bit instruction to accommodate the three-address instructions common to DSP computations. The efficiency of the instruction set allows the SH-DSP to execute up to four operations in a single cycle.

Taking a different approach to add DSP functionality to its ARM7TDMI (Thumb) core, designers at ARM used the core's coprocessor interface to attach the DSP block (*Fig. 1a*). The Piccolo chip, also known as the ARM7TDSP, implements the DSP operations using a RISC approach, placing no restrictions on register usage.

The DSP core employs 32-bit instructions, most of which execute in a single cycle, and a 16-bit fully-parallel, single-cycle multiplier. Part of the core includes an extended register bank consisting of a dozen 32-bit general-purpose registers and four 48-bit extended-precision accumulators. Each register holds one 32-bit value or two 16-bit values. A scaler provides a number of immediate arithmetic or logical shifts followed by an optional saturate in either direction (*Fig. 1b*).

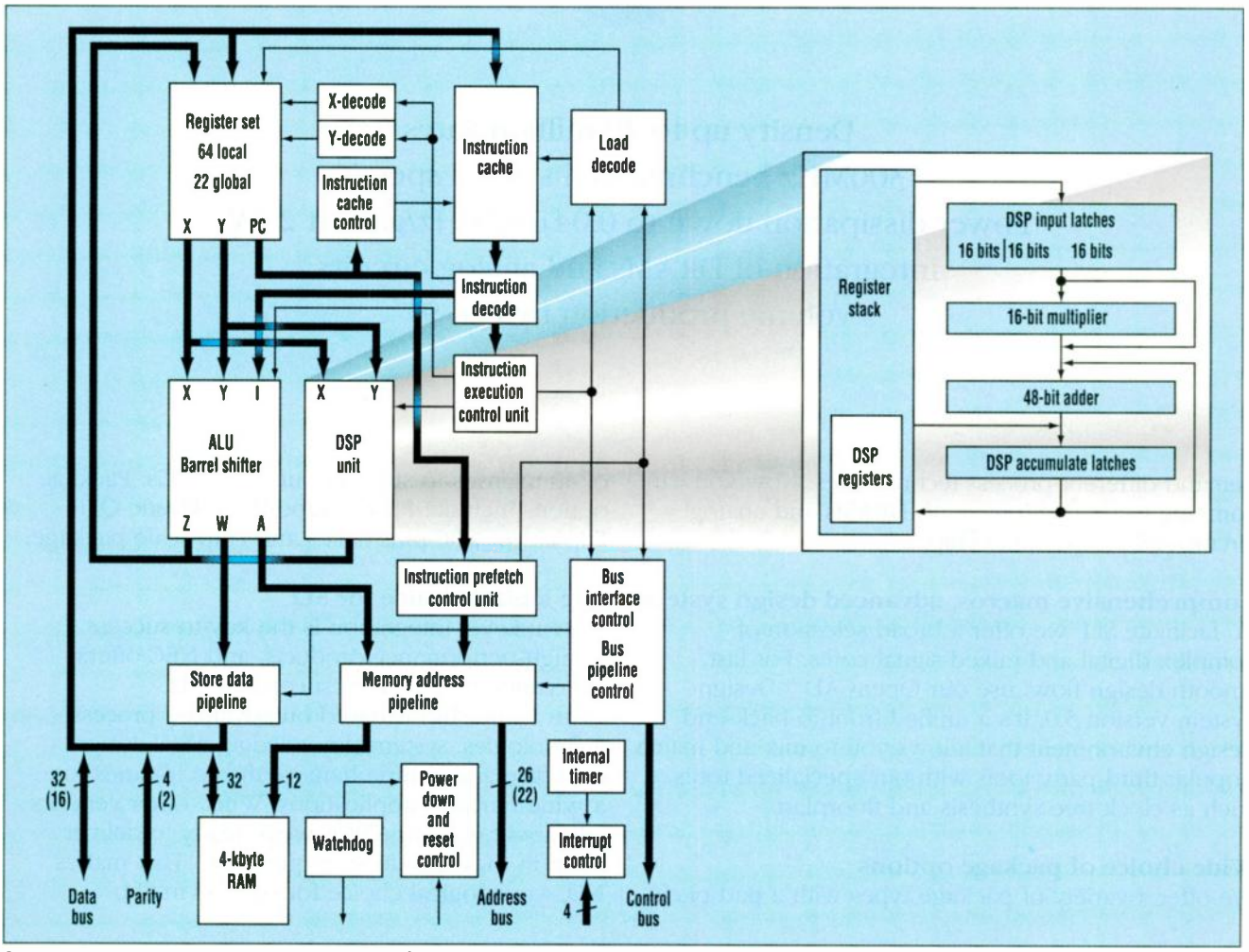
Also included are four zero-overhead loop constructs that help to efficiently execute DSP algorithms. The ALU also can be split, permitting the unit to perform single-cycle, dual 16-bit arithmetic and logical operations. The Piccolo core has its own program counter and fetches instructions from its private buffer. However, the ARM processor generates all data addresses for the Piccolo, and data transfers take place over the coprocessor interface.

The initial version of the Piccolo processor is based on 0.6-µm design rules and delivers 40 DSP MIPS at 40 MHz when powered by a 3-V supply. The ARM7TDMI core also delivers a simultaneous throughput of about 30 MIPS. Migration to 0.35-µm design rules will raise throughput by more than 50%, yielding a power consumption of less than 0.9 mW/MIPS when running from a 3-V supply.

Add Control To DSP

The highly focused architecture employed by most DSP chips is, in many ways, similar to early RISC processors. It is a bare-bones device with few system peripheral support functions on board—just the opposite of most microcontrollers, which often are highly integrated to provide a single-chip solution. Thus, one of the key design challenges is to add all the support blocks around the DSP core and some instruction/ALU enhancements to better handle the control operations.

One company that offers control-oriented capabilities on their DSP chips is



2. Hyperstone's E1-32 processor merges a 32-bit RISC processor and DSP support. The DSP core can hold two pairs of 16-bit data values that can be fed to the 16-bit multiplier (see insert). A wide, 48-bit adder accepts the multiplier's output and minimizes potential rounding errors by allowing full-resolution results to be accumulated.

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Analog Devices, which actually calls its DSP chips "DSP microcomputers." The company has two families, one based on the SHARC architecture, the ADSP-2106x series, and one based on a 16-bit integer core, the ADSP-2100 family. The SHARC family chips carry a 32-bit core DSP engine, a 32-bit IEEE-compatible floating-point math capability, and a large amount of on-chip RAM. The SHARC chips deliver a top throughput of 40 MIPS and 120 MFLOPS. The 16-bit ADSP-2100 architecture includes dual independent address generators, which contribute to the single-cycle execution of all instructions. The DSP engine can deliver up to 40 MIPS of computational throughput.

The 16-bit processors can run at 33 MIPS and perform single-cycle context switches, a feature that could speed the ability to respond to interrupts. On-chip DMA controllers also allow the processors to perform transparent program and data memory transfers. Control-oriented instructions such as bit-manipulation operations and various math operations also have been added to the core.

Dubbed DSP controllers, the Zilog Z893xx series combines a 16-bit DSP engine with many control-oriented peripheral support functions. However, to keep costs down, the on-chip MAC results are truncated to 24-bit, 2's-complement results with fractional representation. A barrel shifter included in the core also was reduced from a full 16-bit shifter to a block with single-bit shift left, no shift, and 1- or 3-bits shift right.

The chip operates at speeds up to 20 MHz, and at that speed can deliver a throughput of 20 MIPS. This family is currently one of the few, if not the only one, that offers an off-the-shelf version with a four-channel, 8-bit analog-to-digital converter (the Z89323) or a PCM codec (the Z89321).

"The modified Harvard architecture of most DSP chips allows multiple simultaneous operations on the chip," explains Nick Marshall, the strategic and technical marketing manger for the Wireless Messaging Division of Motorola. The address generators can operate in parallel with the ALU. Dual address paths provide X and Y operand values using dual parallel moves to keep the ALU busy. "In contrast," continues Marshall, "MCUs typically employ a von Neuman architecture with a single address generator that provides the data addresses." Register-to-register operations are more common with microcontrollers, and data moves can actually bypass the ALU if arithmetic operations are not required.

Modifying a DSP chip to handle control operations requires considerable planning because its register architecture and instruction set are not suited for bit-manipulation operations and I/O control. And that's exactly what designers at Motorola did to craft the currently available DSP56L811 and the forthcoming 56L812. Both are DSP microcontrollers

Creating A Custom DSP/Control Solution

The traditional method of implementing DSP algorithms is to code software to run on commercially available DSP chips, such as those offered by Analog Devices, Lucent Technologies, Motorola, Texas Instruments, and others. Increasingly, however, designers are being challenged to implement the complete system-on-a-chip to meet various design constraints. Reduced size, blazingly fast signal processing for video applications, and reduced power consumption for hand-held devices are three examples of those constraints.

Such challenges drive designers to implement DSP algorithms in custom hardware. Now, more than ever, such a design methodology requires EDA software tools that understand signal processing and provide a seamless path to hardware implementation, explains Rahm Shastry, the senior product manager for the Alta Business Unit at Cadence Design Systems, San Jose, Calif.

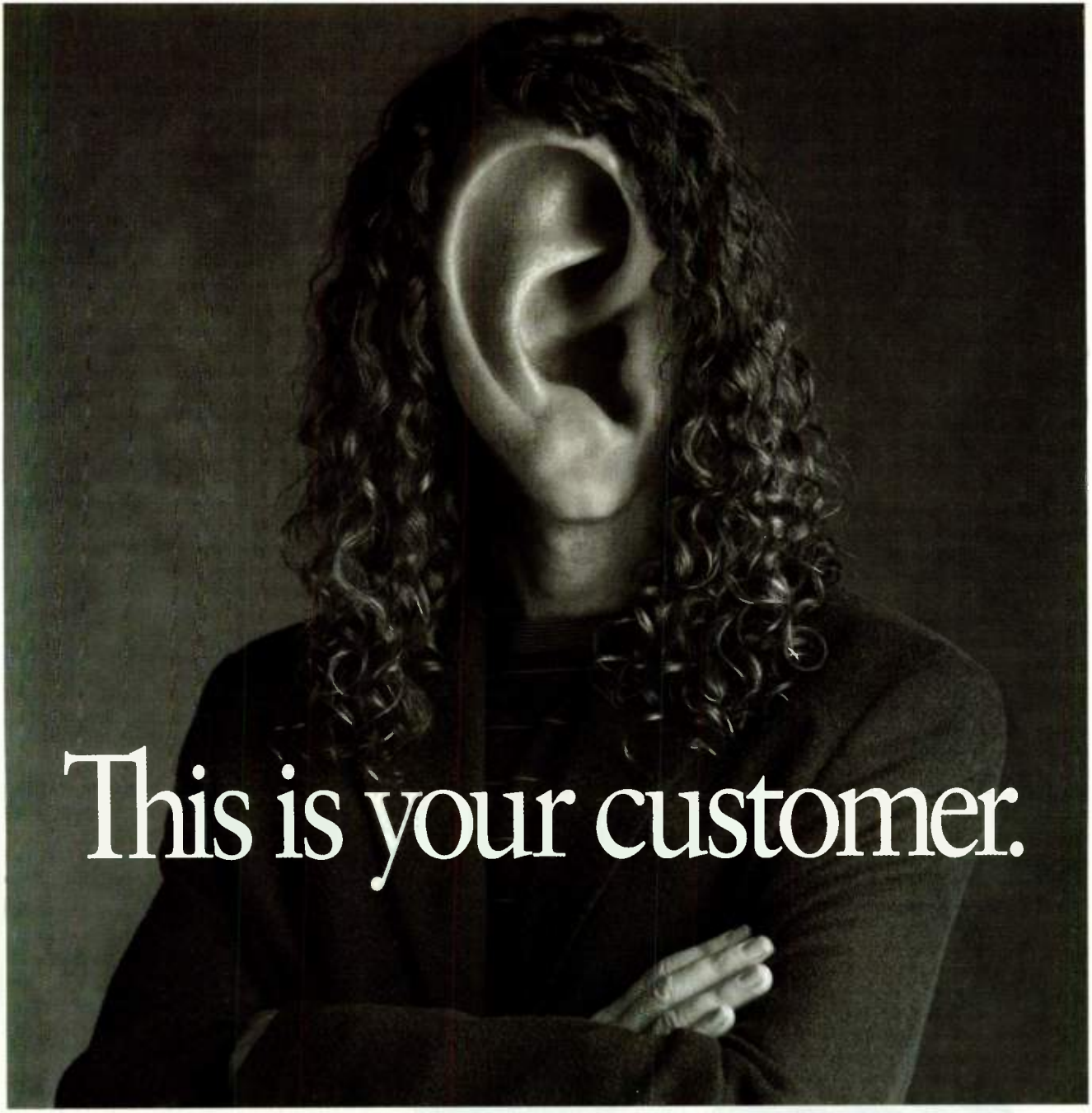
The advanced DSP design solutions available today provide a block-based, application-specific design, analysis, and implementation environment. Using DSP-specific design tools, algorithms are typically captured and verified. Then, designers can partition the algorithmic architecture into hardware and software functions. Software routines are usually written in assembly code for the specific DSP processor. Hardware functions are mapped into building blocks that implement the algorithm.

One way of mapping the functions is by using hardware library elements created as fixed-point elements—registers, RAMs, ROMs, multipliers, adders and multiplexers, for example. Library elements must be able to support variable bit widths, adjustable radix points, and signed and unsigned types. A finite-state-machine editor also can be employed to graphically capture control functions required to support the hardware architecture. The output should be synthesizable at the register-transfer level (RTL) with Verilog or VHDL.

Alternatively, designers can employ a behavioral synthesis tool, which transforms the behavioral description of DSP algorithms into synthesizable RTL Verilog or VHDL. The tool interactively maps algorithms into the hardware architecture by automatically performing resource sharing, scheduling, and allocation. This method allows designers to explore the design space, since such tools have the ability to provide quick estimates of area and speed for the implemented design.

The use of a block-based, application-specific approach, such as that delivered by Cadence's Alta SPW, continues Shastry, provides a path to design DSP-oriented communications and multimedia systems, from concept through synthesizable RTL and final implementation. Moreover, SPW's integrated DSP processor models allow co-simulation of instruction set simulators (ISS) within the environment.

This methodology offers significant advantages over traditional approaches since block-based designs extend design reuse. The same test-bench signals and analysis routines, developed at the system level, can be used to verify the design, downstream at the RTL level and beyond. Design integrity is maintainable and verifiable, from concept through implementation. Thus, the product implementation works as intended from the first silicon onward.



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based on the 56800 core. They include three execution units that all operate in parallel—the data ALU, the address-generation unit, and the program controller—and actually allow a total of six operations during each instruction cycle.

The microcontroller-style programming model and optimized instruction set allow straightforward generation of compact DSP and control code on the 56L811. Additionally, a software stack that resides on the chip allows the user to set up any length stack to handle nested Do loops or subroutines. Additionally, the stack can be used for good context switching as well as for variable passing to support C-language compilers.

The DSP56L811 includes 1024 words of program RAM (16-bits wide), 2048 words (16-bit words) of data RAM, and a small 64-word-by-16-bit boot ROM. I/O resources include two serial peripheral interfaces, one synchronous serial interface, three 16-bit timers, 32 general-purpose I/O lines, and a JTAG test port. The forthcoming DSP56LF812 has the same resources, except that SRAM-based program memory is replaced by flash.

Preceding the Motorola chips, designers at Texas Instruments worked hand in hand with Maxtor to develop a single-core DSP/controller for small-format hard-disk drives. They modified the TMS320C20 series core, giving it about the same performance as the TMS320C25, about 20 MIPS. At the high end, TI has several multiprocessor-on-a-chip solutions with the TMS320C80 and the recently released TMS320C6x families, which deliver throughputs of several hundred to 1600 MIPS.

For maximum efficiency, processor designers also have created radically new processor architectures. These start with basically a clean slate and define a merged-architecture processor that combines both DSP and control operations in a single CPU. Two of the companies that have taken this approach include Hyperstone and Siemens. Their processors, the E1-32 and E2, and the Tricore, respectively, deliver throughputs of up to 130 MIPS in their initial implementations, and provide performance growth paths to over 200 MIPS in 1998 and beyond.

The Tricore is a 32-bit RISC processor that employs 16-bit and 32-bit instructions, but performs a superscalar three-instruction issue every cycle. The core is based on a real-time multitasking engine that performs high-speed context switches and leverages the designer's ability to integrate large amounts of memory on the chip. In the chip the key operations can take place very quickly (*see "RISC Controller Merges DSP And Control Functionality," Sept. 15, p. 39.*)

The E1-32, from Hyperstone, starts with a 32-bit RISC processor that handles both 16- and 32-bit arithmetic based on a 16-bit instruction set. That instruction set can be extended to 32 or 48 bits for immediate operands or displacements. An on-chip cache doubles as both a cache and a buffer. It is supported by an efficient look-ahead prefetch algorithm that allows the cache to be relatively small. Two 16-bit instructions are fetched with just one memory access, delivering hit rates comparable to much larger caches *(Fig. 2)*.

Keeping the architecture simple, the main datapath is only two stages: read and execute. Supporting the datapath is a set of 64 registers, each 32-bits wide; and a set of six registers. The second set of registers is referred to as a stack frame. The stack frame is automatically allocated upon subprogram reentry and released upon subprogram return. The number of registers used in a frame can vary, and is set by the Frame instruction, which can define the frame to any value up to 16 registers. To speed DSP computations, a 16-bit MAC is part of the pipeline. It can perform a 16-bit MAC in a single cycle and execute the operation in parallel with the on-chip ALU, which performs its independent calculations.

When clocked at 40 MHz the E1-32 RISC/DSP processor delivers about 40 MIPS, yet consumes less than 800 mW. A second version, the E2 is currently in development. It will be fabricated with 0.5-µm design rules, operate at clock speeds of up to 100 MHz, and deliver a throughput of 100 MIPS and 300 MOPS, while occupying less than half the area of the E1-32 chip.

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Moderately	555
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DESIGN NOTES

High Power CCFL Backlight Inverter for Desktop LCD Displays

Design Note 164

Jim Williams

Large LCD (liquid crystal display) displays designed to replace CRTs (cathode ray tubes) in desktop computer applications are becoming available. The LCD's reduced size and power requirements allow much smaller product size, a highly desirable feature.

CRT replacement requires a 10W to 20W inverter to drive the CCFL (cold cathode fluorescent lamp) that illuminates the LCD. Additionally, the inverter must provide the wide dimming range associated with CRTs, and it must have safety features to prevent catastrophic failures.

Figure 1's circuit meets these requirements. It is a modified, high power variant of an approach employed in laptop computer displays[1]. T1, Q1, Q2 and associated components form a current fed, resonant Royer converter that produces high voltage at T1's secondary. Current flows

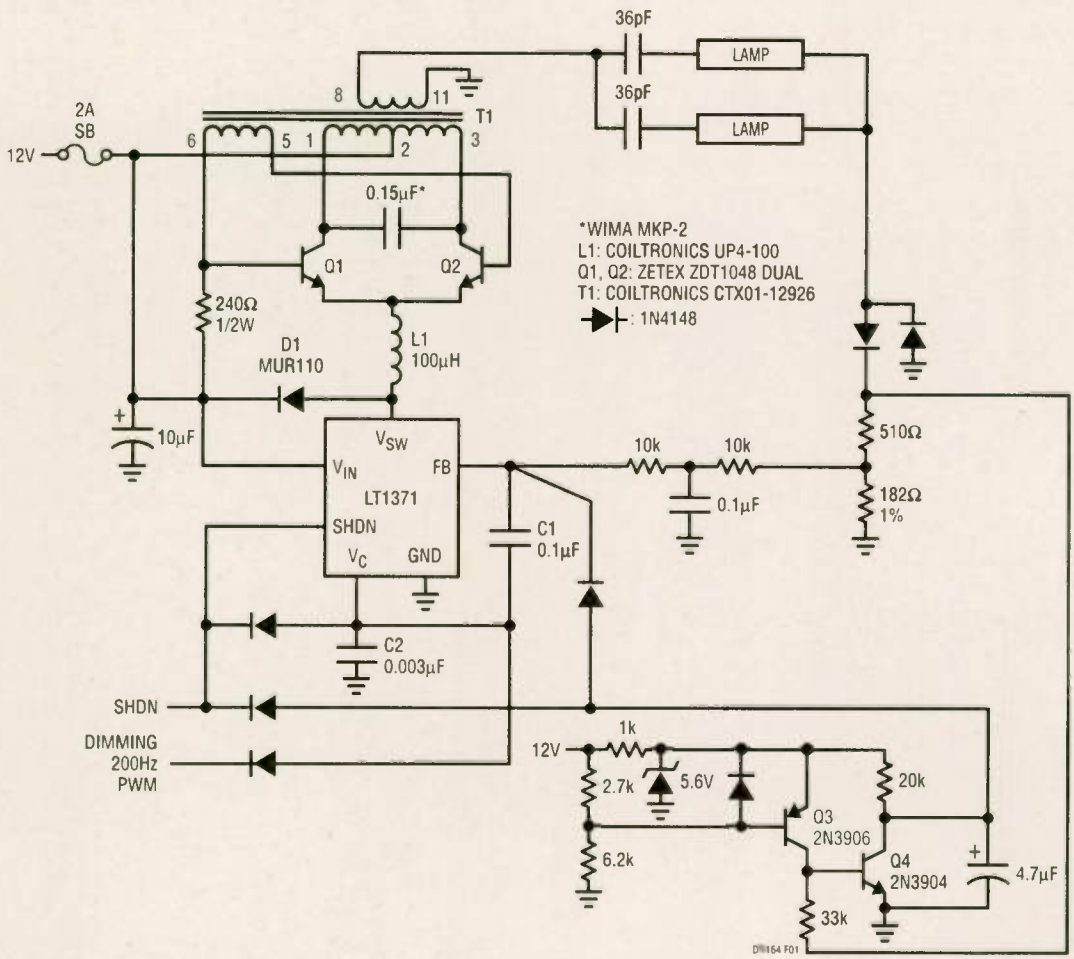

Figure 1. 12W CCFL Backlight Inverter for Desktop Displays Provides Wide Range Dimming and Safety Features

through the CCFL tubes and is summed, rectified and filtered, providing a feedback signal to the LT®1371 switching regulator. The LT1371 delivers switched mode power to the L1–D1 node, closing a control loop around the Royer converter. The 182Ω resistor provides current-to-voltage conversion, setting the lamp current operating point. The loop stabilizes lamp current against variations in time,

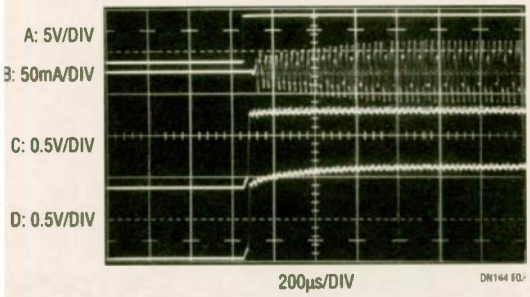

Figure 2. Fast Loop Response Maintains Regulation at 200Hz PWM Rate. Waveforms Include PWM Command (A), Lamp Current (B), LT1371 Feedback (C) and Error Amplifier V_C (D) Pins. Loop Settling Occurs in 500µs

supply, temperature and lamp characteristics. The LT1371's frequency compensation is set by C1 and C2. The compensation responds quickly enough to permit the 200Hz PWM input to control dimming over a 30:1 range with no degradation in loop regulation. Applicable waveforms appear in Figure 2.

Q3 and Q4 shut down the circuit if lamp current ceases (open or shorted lamps or leads, T1 failure or similar malfunction). Normally, Q4's collector is held near ground by the lamp-current-derived base biasing. If lamp current ceases, Q4's collector voltage increases, overdriving the feedback node and shutting down the circuit. Q3 prevents unwanted shutdown during power supply turn-on by driving Q4's base until supply voltage is above about 7V.

Figure 3 shows the shutdown circuit reacting to the loss of lamp feedback. When lamp feedback ceases, the voltage across the 182Ω current sense resistor drops to zero (visible between Figure 3's 2nd and 3rd vertical graticule lines, trace A). The LT1371 responds to this open-loop condition by driving the Royer converter to full power (Q1's collector is trace B). Simultaneously, Q4's collector (trace C) ramps up, overdriving the LT1371's feedback node in about 50ms. The LT1371 stops switching, shutting off the Royer converter drive. The circuit remains in this state until the failure has been rectified.

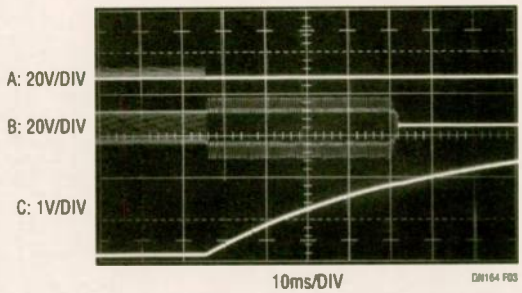

Figure 3. Safety Feature Reacts to Lamp Feedback Loss by Shutting Down Power. Lamp Current Dropout (Trace A) Allows Monitoring Circuit to Ramp Up (Trace C), Shutting Off Drive (Trace B)

This circuit's combination of features provides a safe, simple and reliable high power CCFL lamp drive. Efficiency is in the 85% to 90% range. The closed-loop operation ensures maximum lamp life while permitting extended dimming range. The safety feature prevents excessive heating in the event of malfunction and the use of off-the-shelf components allows ease of implementation.

1. See LTC Application Note 65, *A Fourth Generation of LCD Backlight Technology.*

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JANUARY 1998

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Photonics West, January 24-30. San Jose, California. Contact the SPIE Exhibits Dept., P.O.Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

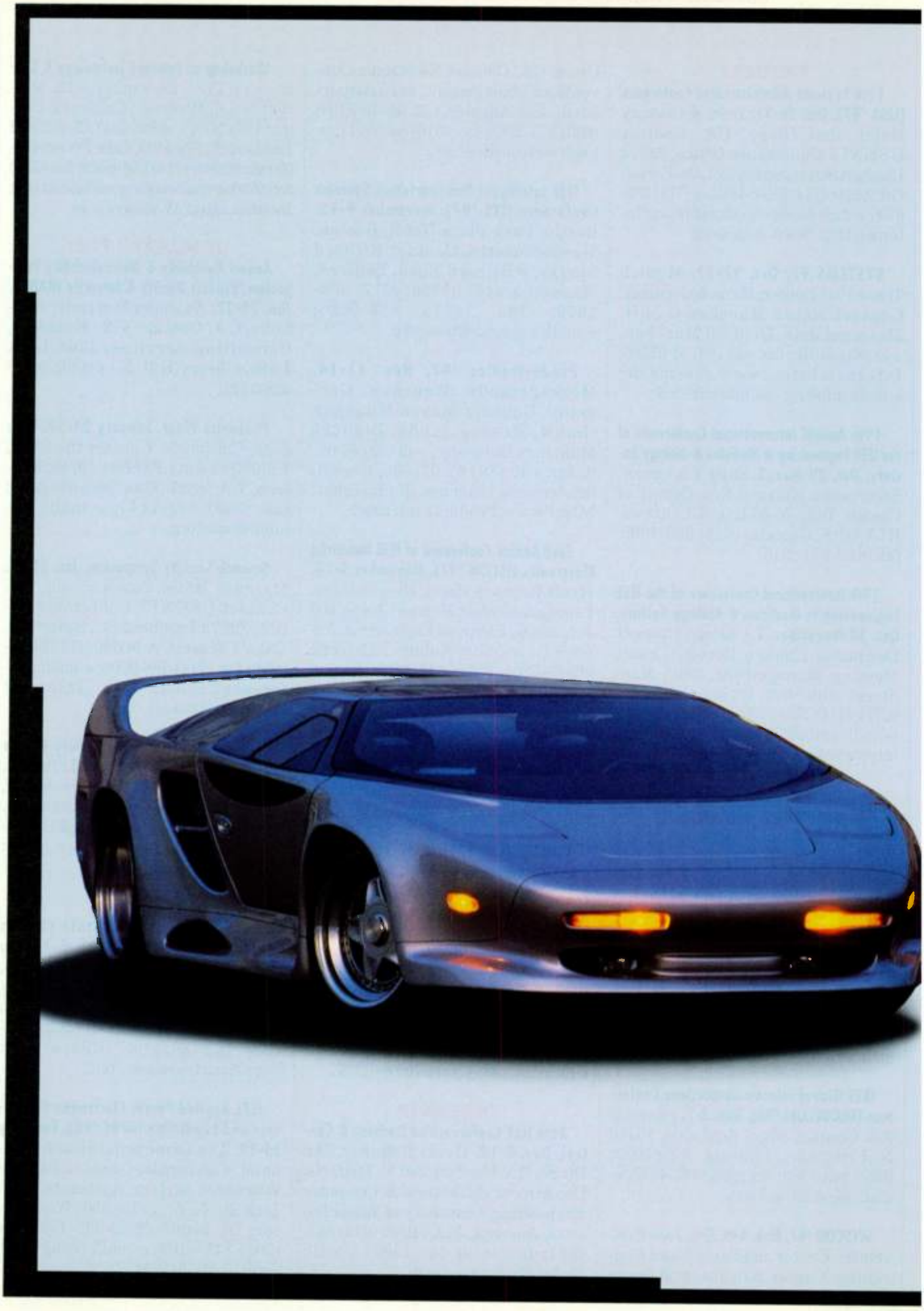
Seventh Security Symposium, Jan. 26-29. Marriott Hotel, San Antonio, TX. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Winter Meeting, January 31-February 5. Tampa, Florida. Contact Jim Howard, Tampa Electric Co., P.O. Box 111, Tampa, Florida 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

FEBRUARY

IEEE International Solid-State Circuits Conference (ISSCC '98), Feb. 5-7. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

IEEE Applied Power Electronics Conference and Exposition (APEC '98), February 15-19. The Disneyland Hotel, Anaheim, California. Contact Pamela Wagner, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 639-4990; fax (202) 347-6109; e-mail: pwagner@courtesyassoc.com.



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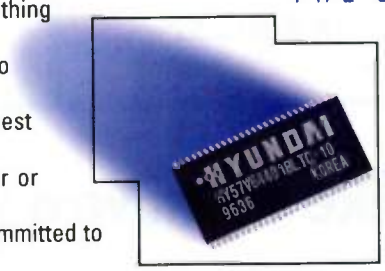

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8M x 8 EDO	3.3V	50/60/70 ns	4K/8K
4M x 16 EDO	3.3V	50/60/70 ns	4K/8K
16M x 4 Sync.	3.3V	66/83/100MHz	4K/8K
8M x 8 Sync.	3.3V	66/83/100MHz	4K/8K
4M x 16 Sync.	3.3V	66/83/100MHz	4K/8K

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Embedded C++ Slashes Code Size And Boosts Execution

New Specification Lets Developers Take Advantage Of The Object-Oriented Features Of C++ , And Avoid Some Of Its Pitfalls.

MIKE HADEN, Green Hills Software, 30 W. Sola St.., Santa Barbara, CA 93101; (805) 965-6044; fax (805) 965-6343; e-mail: mike@ghs.com or craig@ghs.com.

Embedded system programmers have by and large remained loyal to the C language, while their counterparts working on desktop applications have enjoyed the object-oriented features of the C++ language. However, the robust C++ language does have one major pitfall: Using it results in code that's simply too bloated for memory-sensitive embedded applications.

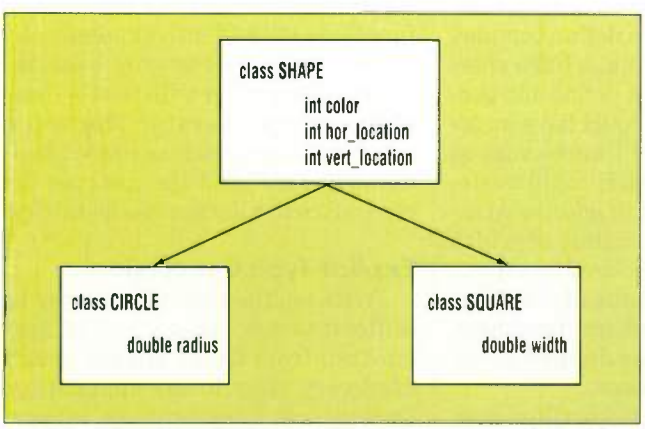
To address the shortcomings of C++ for embedded applications, an industry group led by major Japanese CPU manufacturers, including NEC, Hitachi, Fujitsu, and Toshiba, has set out to define a new dialect of C++ called EC++. The goal of the effort is to preserve the most useful object-oriented features of the C++ language yet minimize code size while maximizing execution efficiency.

The EC++ Technical Committee has already produced a draft specification for the new dialect targeted squarely at the 32-bit processors widely used in embedded applications. The committee also is working on a style guide that will help embedded systems programmers maximize the efficiency, readability, reliability, and maintainability of their EC++ programs. Development of validation suites for a broad range of processors, including MIPS, PowerPC, 68k families, Coldfire, Hitachi's SH family, and NECs' V800 also is underway.

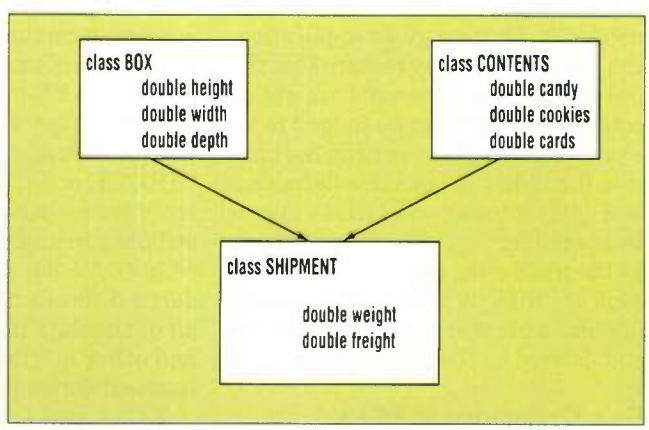
EC++—A Few Simple Reasons

Some C++ features such as exception handling and multiple inheritance add code-size and performance overhead, even when they are not used in a program. Features such as namespaces, mutable specifiers, and new-style casts are difficult to understand, increasing the chances of programmer errors. Moreover, these features are overkill for many embedded applications. The use of templates often results in code bloat and programmers struggle to accurately judge the amount of code that will be generated when using templates. C++ library functions including standard I/O functions result in large amounts of code being added to a compiled program, even though most of the code is never executed.

Before examining the features that have been omitted, programmers should consider the advantages of the object-oriented features that



1. In basic inheritance, the classes CIRCLE and SQUARE are derived from the class SHAPE. They both inherit the attributes "color," "hor_location," and "vert_location." Each, however, has additional unique attributes that characterize it.

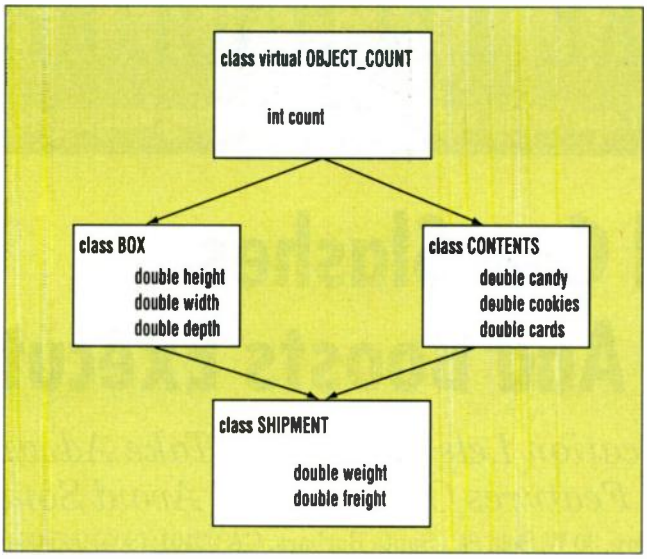


2. In multiple inheritance, the class SHIPMENT inherits the data members of both BOX and CONTENTS. It then adds its own characteristic variables. Any class derived from SHIPMENT would carry all the inherited attributes.

remain in EC++. Object classes have proven to be the most useful concept of C++. These classes allow programmers to partition code so that housekeeping functions like memory allocation and the initialization of data structures are separated from the main part of an application. The ability to separate these functions results in more readable code. The class definitions create objects that can be reused throughout a program.

For example, a programmer can use classes to describe objects ranging from arrays to geometric shapes to animals. A class called BOX can be defined with attributes such as height, width, depth, and even color or weight. When created, each instance of a BOX object automatically includes all class attributes or data members. The class definition includes the necessary object constructors, destructors, memory allocation code, and functions that are specific to the BOX class—for example, a function that returns the volume of a box.

Both EC++ and C++ also let programmers redefine standard operators—a technique called operator overloading—in such a way that they have meaning relative to a specific object type. For example, a programmer could redefine the "=" operator for use with two BOX objects. The programmer could specify that box A = box B when the two have equal dimensions. Or for a given application, the programmer may require that the boxes must share the same weight or color before they can be judged to be equal. The programmer can harness this flexibility in the class definition and apply it to any valid EC++ operator, including "+,-,*/, >, <" and others. In the main code, a simple expression such as "BOX_A > BOX_B" is unambiguous and returns precisely the result desired by the programmer.



3. By combining multiple inheritance with a virtual base class, the objects BOX and CONTENTS have access to a single copy of the OBJECT_COUNT class that can be used to track the active number of objects in existence.

C++ Omissions in EC++

EC++ actually retains much of the value found in C++, and discussion of the omitted features will both illustrate and detail other valuable features and limits imposed in EC++. The list of omitted features is short:

- Multiple inheritance and virtual base classes
- New-style casts
- Mutable specifiers
- Namespaces
- Run-time type identification
- Exceptions
- Templates

In reality, of course, classes are a significantly more complex concept than our BOX example indicates. Multiple inheritance and virtual base classes fall at the complex end of the robust class concept implemented in C++. Programmers often use a hierarchical structure to define complex classes. For example, a base class called SHAPE might define any geometrical shape and could have an attribute such as color. Classes such as CIRCLE or SQUARE could be derived from shape with additional attributes including radius or width *(Fig. 1)*. An object declared based on a derived class automatically includes all of the data members, functions, and other attributes defined in the base and derived classes.

EC++ and C++ both allow programmers to build multilevel class hierarchies in a linear fashion. C++ also allows multiple inheritance in which the programmer defines a new class based on two or more peer classes. For example, a programmer could define one class called BOX and a second class called CONTENTS. A new class called SHIPMENT could then be derived from BOX and CONTENTS. An object declared using the SHIPMENT class would inherit the data members, functions, and other attributes of both BOX and CONTENTS *(Figs. 2 and 3)*.

Multiple inheritance can be valuable in a number of applications and is regularly used in graphical desktop environments such as Microsoft Windows. In Windows, for example, a useful object class can be derived based on a WINDOW class with display attributes such as size and borders; a MENU class with attributes such as menu names and styles; and a DISPLAY class with attributes that describe objects displayed in a window. Virtual base classes can be used along with multiple inheritance to share a base class which is inherited multiple times in a deviation hierarchy.

Some embedded applications could make use of multiple inheritance and virtual base classes but it's not nearly so useful a tool as in desktop applications. Supporting multiple inheritance in a compiler can carry a significant burden and the technique is tricky to use correctly. Multiple inheritance can result in multiple base classes that include data members or functions with identical names and therefore must be correctly identified by the programmer with the C++ resolution-scope operator. Moreover, real-world applications like embedded systems lend themselves far more often to a linear class hierarchy.

Explicit-Type Conversion

While multiple inheritance may be difficult to use, other C++ features omitted from EC++ simply aren't used very often in any application. Despite such infrequent use, support for these features in C++ libraries results in bloated code, and it's usually better just to do without them. One good example is the dynamic_cast fea-

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ture that was added as part of the new-style casts.

The C and C++ languages support the concept of "casting" to convert from one data type to another. For example, an integer must be converted to a floating-point number before it can be added to another floating-point number. Programmers also can use the casting concept to convert pointer types. In general, programmers should strive to minimize the need for casting because it's often indicative of a poorly structured program. EC++ and C++ class structures already reduce the need for casting relative to typical C programs.

In C, and therefore C++, since it's a superset of C, an expression such as (double)X will cast the value in X as a floating-point number, even if X had originally been defined as integer or short. C++ includes new more-explicit cast operators including 'static_cast,' 'reinterpret_cast,' 'const_cast,' and 'dynamic_cast.' With the exception of the dynamic case, these new-style casts don't so much add functionality to traditional C casts, but rather make the intentions of the program author more explicit. The features, however, haven't garnered much popularity in the programmer community. In fact, most popular C++ books don't even mention the new-style casts. Once books are revised to the current ANSI C++ level, they will probably discuss the new-style casts and possibly lead toward wider usage.

Mutable specifiers also represent an arcane feature of C++ that is essentially a special case of explicit type conversion. Programmers can use the keyword 'mutable' to cast a data member of a class in a way that it can be modified even though the class is logically constant. Because new-style casts and mutable specifiers are rarely used, they are not justifiable for EC++, especially in light of the code overhead required to support dynamic_cast and the complexity of using mutable specifiers correctly.

Namespaces, Run-Time-Type ID

Some other C++ features including namespaces and run-time-type identification (the mechanism used by dynamic_cast and other features) are primarily useful in extremely large applications. More specifically, these features are useful in projects where many programmers working on a single code base. They also come in handy when a programmer must interface an application with multiple libraries and code modules from different sources.

Namespaces give the programmer a way to avoid name conflicts. When several programmers work together, or when a programmer uses libraries from a third party, there is a good chance that they will run into duplicate function, class, or variable names. The programmer can declare a namespace and essentially contain a code module within that namespace. Within the module, the programmer can access any variable or function normally. Code outside the namespace, however, must use the name of the namespace with the resolution-scope operator to refer to a variable or function within the namespace.

In most embedded applications, the programmer or programmers will be dealing with a much smaller code universe—especially relative to desktop environments such as Windows. Experiment with Microsoft Visual C++ for Windows, and you'll discover thousands of arcane functions that have been developed over a decade and remain in libraries so that legacy applications will still work in the latest Windows release. Moreover, the typical Windows application is partitioned into dozens of header and source files. Namespaces can be critical to successful Windows programming.

Namespaces, however, are difficult to use correctly. Programmers can measure namespaces inappropriately and simply add complexity to code unnecessarily. Embedded system programmers typically need namespaces, and therefore should not need to deal with the associated complexities.

Run-time-type identification, meanwhile, solves a different problem that programmers regularly encounter when using libraries and classes developed by third parties. In C++, a program can be passed to an object of unknown type, and may need a way to identify that object's type. In a simple case, a code library could pass a pointer to an application and the type of the pointer could be associated either with a base class or a derived class. In the case of the SHAPE example used earlier, an application could receive a pointer to an object that is of type SHAPE. In reality, however, because SHAPE is a base class, the pointer could be of type SHAPE, SQUARE, or CIRCLE. C++ provides the keywords 'dynamic_cast' and 'typeid' that programmers can use for identifying the actual type at run time.

Much like namespaces, the run-time-type identification feature is far more useful in desktop environments than in embedded systems. Windows libraries, for example, pass pointers to display windows, menus, and content indiscriminately. Embedded system programmers typically have more control of the code base and will benefit more from the overhead eliminated by omitting the feature from EC++ than they would from using the feature.

Exception Handling

Unfortunately, not all C++ features omitted from EC++ can be dismissed quite so easily. Exception handling, for example, provides a robust mechanism through which a programmer can centralize and organize code to handle runtime errors or exceptions. Embedded systems need precisely these capabilities to handle conditions such as out-of-range input values in a data-acquisition system, or dangerously high air-pressure readings in an industrial-control scenario.

C++ exception handling allows the programmer to specify "try blocks" of code and anywhere within that block, or within code called from the block, throw control to an exception handler contained in a "catch block." C++ offers significant flexibility in how exceptions are handled and, in all cases, lets the programmer separate the exception-handling code from the mainline application. The programmer can dedicate a catch block to each try block. Alternatively, a single catch block can service an entire program.

Unfortunately, exception handling is the leading offender when it comes to bloated code. Typical exception-handling libraries and user code even bloat code when the feature isn't used in a C++ application. In addition, progammers can't determine the latencies associated with C++ excep-

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UPDATE ON DSP RTOSs

DSP Applications Are Attracting The Makers Of Real-Time Operating Systems

The growing volume of applications using digital-signal processing (DSP) technology is creating an attractive environment for commercial real-time operating-system (RTOS) support. The pioneer in the DSP-specific RTOS arena, Spectron Microsystems, Santa Barbara, Calif., will soon start seeing competition to its SPOX operating system. Imitation—or in this case, competition—may be the sincerest form of flattery. Two players offering real-time operating systems that bridge the worlds of traditional microcontrollers and DSP chips are Eonic Systems, Silver Spring, Md., and Wind River Systems, Alameda, Calif. Spectron is not sitting still, however, and has recently announced a developer's kit for the DSP/BIOS from Texas Instruments, Dallas.

The move toward commercial RTOS support for DSP is a natural result of the increasing performance and functionality of the silicon, which is moving from being high-speed math engines to chips incorporating many of the kinds of features found on mainstream microcontrollers. The attractiveness of DSP in communications, multimedia, aerospace, and other applications is fueling the time-to-market pressure familiar to other embedded-systems designers. Consequently, this leads to the need to focus the expertise of DSP designers on application issues rather than focusing on repeatedly implementing system-level functions.

Scaling Down The System

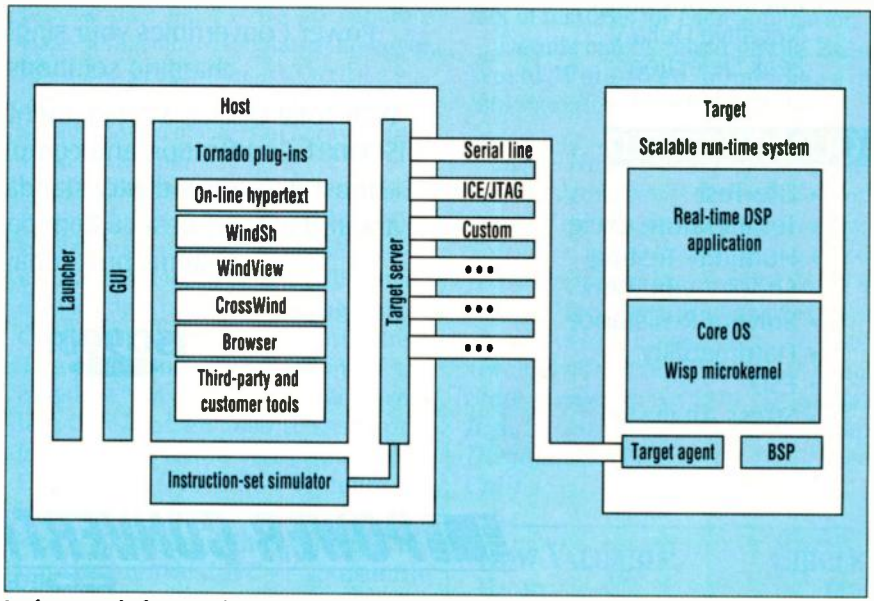
DSP-based systems often include multiple DSPs and also conventional microprocessors. The Virtuoso 4.0 RTOS and its SoftStealth technology from Eonic Systems focus on optimization and scalability based on a single programming model called the virtual single processor (VSP). The VSP programming model presents the same API for developing real-time applications with 8-bit microcontrollers and large parallel DSP systems. The SoftStealth technology lets designers remove unneeded resources to pare the footprint down to the minimum use of memory and power required by the application.

The SoftStealth technology works with the four-level architecture of the Virtuoso 4.0 RTOS. The lowest level is called ISR0 and is used for FIFO-based, synchronous interrupt handling. Often, this is the hardware mechanism of the processor and requires little or no code. The second level, called ISR1, allows the prioritization of asynchronously arriving interrupts. Eonic equates ISR1 with the functionality of the Texas Instruments DSP/BIOS and it also is frequently supported by processor hardware. Using ISR1 requires attention to the application logic since interrupt handlers cannot deschedule. ISR1 is best limited to applications that are highly predictable or where interrupt handlers can be kept short enough that delays won't affect the operation of the system.

The third level of the Virtuoso 4.0 architecture adds a prioritized round-robin-scheduling nanokernel. Mainly intended for handling asynchronous data streams, the nanokernel can be programmed for multimode operation with the higher-level microkernel. The nanokernel can handle lower-priority traffic while the microkernel could be given a high priority for handling a set of critical pre-emptable interrupts. This final level, the fully pre-emptive microkernel, adds the ability to interrupt a running task when a higher-priority interrupt occurs. All program code written at the microkernel level is portable to other processors running with Virtuoso 4.0. It also can be freely scaled across a multi-processor network.

Initially, Virtuoso 4.0 generates a maximum system, and then the developer can use the SoftStealth tool as an optimizing system-generation tool to pare the system down to size. The tool works at three levels. First, you can selectively remove one or more higher levels of the architecture, such as the pre-emptive microkernel, if their services are not needed. This in itself can dramatically reduce the memory footprint.

Second, if the system does require nanokernel or microkernel services, you can selectively remove all unused services, thus minimizing the nano- or microkernel code actually present in the system. If needed, you can then



In the Tornado for DSP development environment, Tornado tools plug in along with third-party tools and share a common user interface. The target server can connect to a variety of links to the target-resident agent. The agent communicates between the DSP code running under the Wisp kernel and the host-based tools.

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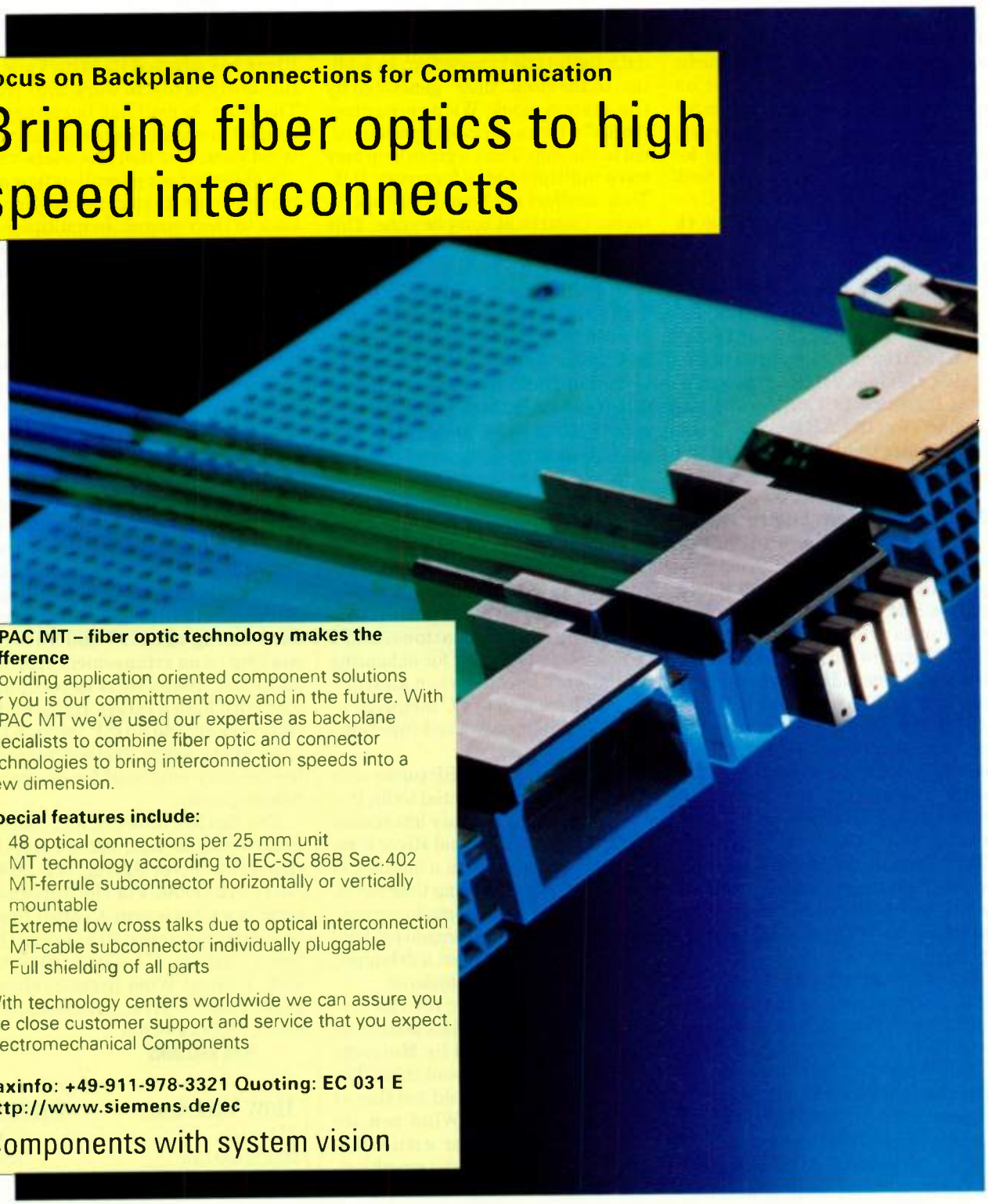

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add application-specific services without carrying the baggage of unneeded kernel code and minimizing the run-time overhead. Third, when a service exists in several versions, such as blocking, nonblocking, and timed-out versions, you can remove the less-frequently used versions and simply let the application use a single version.

Virtuoso 4.0 comes with a GUI-based development environment that includes a system editor that works with the SoftStealth optimization tool. In addition, there is a console for initializing and booting the target, graphics services, and a task-level debugger and tracing monitor. A host server is provided as a set of C++ classes that allow integration with other programs. The host server can be integrated with a specific target by using one of several board support packages or—for unsupported or custom boards—by using a board porting kit. Virtuoso 4.0 supports the Analog Devices 21020, 2106x, the Texas Instruments TMS320C3x, -4x, -5x, and -6x, the ARM6-7-7-T, the DSP Group's OakDSPCore, and the Hyperstone E1-32 DSP ICs.

DSP Development Environment

Where Eonic supplies a DSP-oriented RTOS that comes with a development environment, Wind River supplies a development environment that comes with a DSP-oriented RTOS. Tornado for DSP reflects the view that current DSP development tools focus exclusively on DSP-related issues, and are not integrated into a greater framework for embedded application development. Tornado is a tool integration and target connection environment that's built around Wind River's VxWorks RTOS. Tornado for DSP uses a similar architecture with DSP-oriented tools, a new DSP kernel called Wisp, and a tools-to-Wisp connection strategy *(see the figure)*.

The Wisp kernel was written from scratch, but was designed to retain much of the VxWorks API along with special features oriented to the needs of DSP. While it offers fewer features than the full VxWorks, it requires only about 2000 to 6000 bytes of system memory. The first release of Wisp is targeted for the Motorola 563xx series of DSP chips and is written in assembler. It uses a subset of the target DSP's register set in order to improve context switch time. It also separates system and task memory stacks. Since system stacks handle interrupts, tasks running on the system only need to account for their own memory blocks, thus reducing memory requirements.

Wisp has implemented a finer-grained interrupt scheme for periodic data-path-type processing. In addition to the clock "ticks" generated by the system clock, Wisp recognizes "tocks" which are clock signals internal to the chip. Thus, a given chip may have multiple tocks for every tick. Tock handlers are bound to a tock interrupt source at compile time. This allows an interrupt service routine to be invoked at a tock boundary, rather than waiting for a system clock tick. This allows application code that has very high periodic requirements to be bound into the tocks. Wind River is claiming an interrupt latency of 0.75 µs and a context switch time of less than 4.5 µs on an 80-MHz Motorola 563xx.

While Wisp represents a pared-down kernel at run time, users can optionally expand the run-time capabilities to suit their applications' needs. There is, for example, an exception-handling library, a semaphores library to enhance interprocessor communications, and a message-queue library for enhancing communications between multiple tasks. There also is a C language library of commonly used functions and algorithms.

While Tornado for DSP comes with a number of DSP-oriented tools, it is designed to allow the easy integration of third-party tools. Wind River is reportedly working with a number of DSP tool vendors to bring their development tools into the Tornado environment. Included with Tornado for DSP are a compiler, a browser, a debugger, and an instruction set simulator.

The GNU compiler for the Motorola 563xx family and its associated tools were developed by Motorola specifically for their line of chips. The debugger is an updated version of Wind River's CrossWind remote source-level debugger with Wisp-specific extensions and a graphical-user interface (GUI). The Tornado code and object browser graphically displays Wisp code, objects created by the code, memory allocations, message queues, semaphores, register usage and other structures. The Wisp kernel is bundled with 563xx instruction set simulation libraries that permit code development without the presence of hardware.

In addition to the standard tools included with Tornado for DSP, Wind River has adapted its WindView visual-analysis tool to work with Wisp. The Wisp kernel has been instrumented to enable visual analysis with WindView. The tool lets users visually observe task execution flow and trace events that generate errors back to their source. In multitasking applications, one task can send false data to another task, which may cause an error in a third task. WindView lets you see what messages are being passed, which tasks are blocked, running, or waiting for data.

The goal of Tornado's target-connection strategy is to minimize the impact of the host tools on the target environment. Tools on the host communicate via Tornado's host-based target server. In some cases, target server can communicate directly with the target hardware via an in-circuit emulator. In other cases, it would use a connection such as a serial link to communicate through a target-resident debug agent. Wind River is working on an arrangement that will allow host-based tools to communicate with both a target-resident microprocessor and a DSP through the same proxy agent, further minimizing memory overhead for designing mixed systems.

For further information, contact Eonic Systems Inc., 12210 Plum Orchard Dr., Silver Spring, MD 20904 (301) 572-5000; Via the Internet: http://www.eonic.com. Contact Spectron Microsystems, 315 Bollay Dr., Santa Barbara, CA 93117 (805) 968-5100. Contact Wind River Systems, 1010 Atlantic Ave., Alameda, CA 94501; (510) 748-4100.

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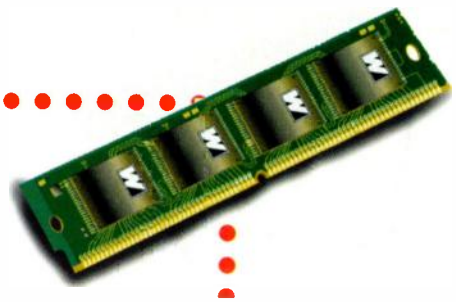

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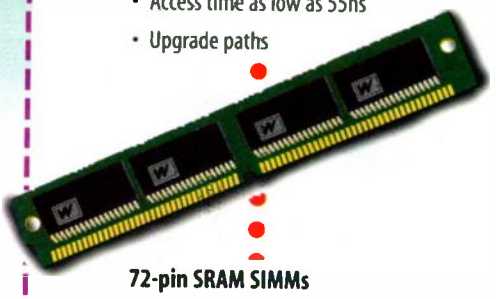

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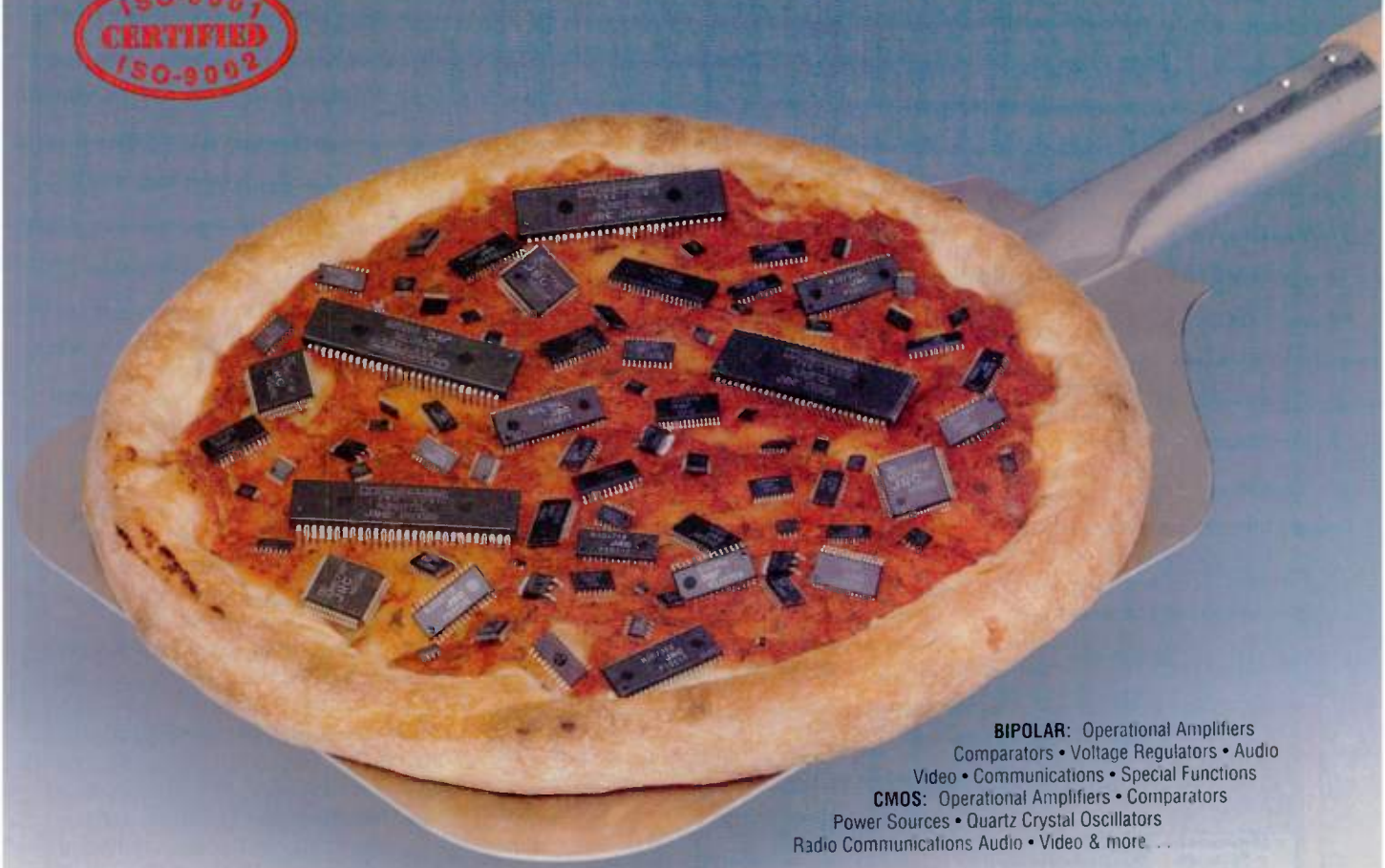

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UPDATE ON REAL-TIME WINDOWS NT

Tools Add Fault Tolerance, Scalability To Real-Time Windows NT

Moving Windows NT into real-time applications brings the advantages of a familiar user interface, a wealth of off-the-shelf software, and the availability of a wide selection of development tools. But it also brings to the table a set of problems. In addition to the fact that Windows NT was not originally designed for real-time, deterministic performance, there are issues of size and reliability.

RadiSys, Hillsboro, Ore., has addressed the problem of determinism with its INtime product, which adds real-time extensions to standard Windows NT. To tackle the problems of size and reliability, RadiSys has partnered with Kirkland, Wash.-based Intrinsyc to offer a pair of products that provide fault tolerance for running applications and the ability to configure systems for optimal use of resources.

Since Microsoft will not license the Windows NT source code, it is impossible to modify the kernel for real-time behavior. RadiSys has added its own real-time kernel and corresponding applications programming interface (API) onto Windows NT 4.0. To ensure that real-time tasks will always have priority over any NT task, all of NT is made a single low-priority INtime task under the real-time kernel. All tasks under Windows NT run as they normally would. However, when the real-time portion receives an interrupt, all of NT is suspended and the higher-priority real-time task runs.

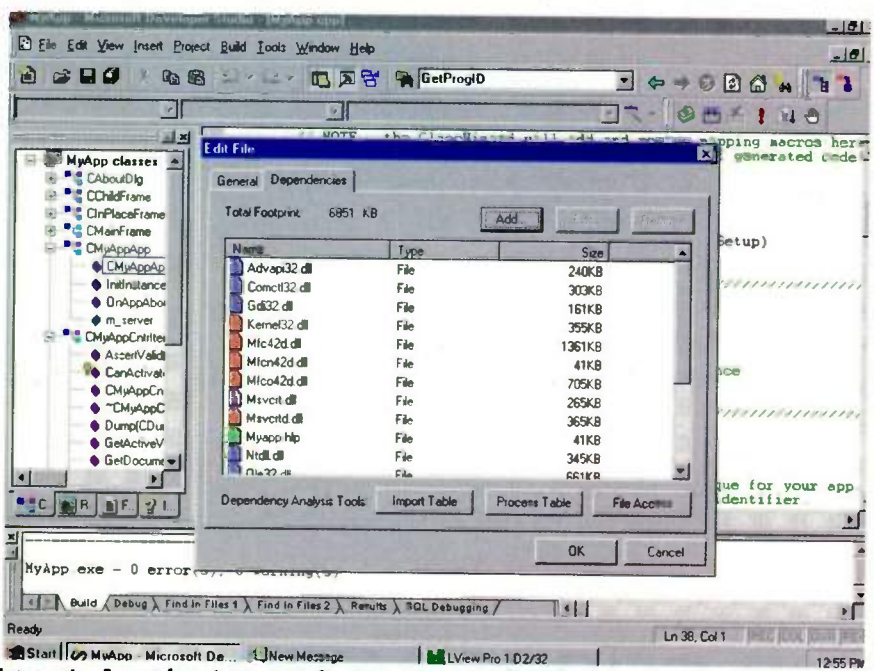
The real-time side of INtime has its own protected memory space separate from that of Windows NT. Therefore, real-time tasks and drivers cannot overwrite NT memory, and vice versa. In addition, each real-time task is assigned its own protected memory segment at the hardware level using the descriptor table registers in the processor. RadiSys did write one kernel-level driver as part of the INtime package. This is the NTX driver that provides cross communication via the operating-system extension mechanism (OSEM). This lets you have semaphores, mailboxes, and shared memory between WIN32 threads on the NT side and threads written on top of the real-time kernel.

Even for applications, size and optimal use of system resources is an important matter. The Integration Expert (IX) from Intrinsyc offers software component analysis of both the OS and the application to help optimize the integration on Win32 platforms *(see the figure)*.

IX has four functions: Dependency analysis, profiling, configuration, and target generation. Automatic dependency analysis examines the static and dynamic relationships between the OS and application layers and identifies how all the application DLLs are linked with the operating system. IX then produces an information metafile and a visual display of a component dependency tree and a unique components list. The profiling function uses this information to calculate the size of the total target footprint and what components it is using. It also lets you identify where all the DLLs are being called from the application.

The configuration function of Integration Expert lets users produce a library of platform-specific information that describes specific single-board computers in terms of their peripheral requirements, memory limitations, disk space, and so forth. This helps determine what components must be or can be left out of Windows NT to be able to integrate the OS/application combination to that board. In addition to the configuration models that can be built using IX, the tool can use a variety of OEM adaptation kits (OAKs) supplied by third parties. Naturally, RadiSys supplies a full set of configuration models for all the board-level products that it offers.

The process of dependency analysis, profiling, and configuration is an iterative activity and not fully automatic. The tool presents you with certain information; you then make decisions and refine the process. There also are certain choices involved with the target generation process. For example, you might choose to partition the application between disk and memory, put it in ROM, or have the whole thing loaded from disk. The target generator uses these choices to interact with the information model of the software system and deploy it accordingly onto the hardware.



Integration Expert from Intrinsyc Software analyzes the dependencies among Windows NT modules for a given application. From the analysis, the programmer can tell what components and DLLs must be included (and which can be left out) to optimize the code size. The tool also displays the current size of the memory footprint.

Fault Tolerance

While INtime can survive a full crash of Windows NT, there is a need

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WRH

for fault tolerance at the real-time application layer for faults that cannot be resolved by hardware techniques or by the underlying operating system. Intrinsyc's WinFT offers a watchdog utility and services so that developers can implement fault tolerance in their applications. Using the static and dynamic C++ libraries, you can instrument portions of your code to set up scenarios to watch for invalid data or events. In addition, you can set up procedures for recovery and exception handling. These can include the detection and restart of failed processes, rebooting of a malfunctioning OS, checkpointing, and recovery of volatile data.

WinFT also can perform software rejuvenation where it shuts down the running application and then brings it back and restores the checkpointed data. Checkpointing involves writing essential application data to disk at critical times. If an application fails between checkpoints, it can be restarted from its last checkpoint. Software rejuvenation involves gracefully terminating a persistent application at an appropriate time, such as when it is not busy. This can help correct such results of "aging" as memory leaks or the loss of resources due to a badly behaved application. What WinFT offers is a tool, but, actually designing the fault tolerant aspects of the system depends on the programmer.

Obviously, shutting down and restarting a critical real-time control application would not always be appropriate or safe. WinFT comes with a number of pieces of demonstration code that let users get an idea of how to use the various options to put together a fault-tolerant scenario appropriate to their needs. In addition to scenarios set up using the libraries, applications can pass system error messages to the watchdog server. As specified by the programmer, the server can then either restart the application or even reboot the operating system.

Contact Intrinsyc, 550 Kirkland Way, Suite 205, Kirkland, WA 98033; (206) 739-2009; Internet: http://www.intrinsyc.com; RadiSys, 5445 NE Dawson Creek Dr., Hillsboro, OR 97124.

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Avoiding The Twists And Turns When Choosing Flexible Cable

A Sound Knowledge Of Cabling Options Can Greatly Improve System Reliability.

RICHARD A. BUCHICCHIO, Olflex Wire & Cable Inc., 30 Plymouth St., Fairfield, NJ 07004-1697; (800) 774-3539; fax (201) 575-7178.

Automated electronic systems increasingly require different types of flexible cable that can withstand millions of flexing cycles in precise, demanding applications. As is the case with power supplies, cable is just a step in the overall design process, and is usually the last component to be added in, even in the most sophisticated pick-and-place automation systems (*Fig. 1*). This is particularly unfortunate when you consider that more often than not, the cause for downtime can be directly attributed to a breakdown in the cable, not the equipment.

The first step toward a good cable choice is the realization that all flexible cable is not alike. A knowledgeable design engineer can dramatically increase the life of the cables—and the efficiency of the equipment—by specifying the proper cable for each application, installing it correctly, and understanding its requirements.

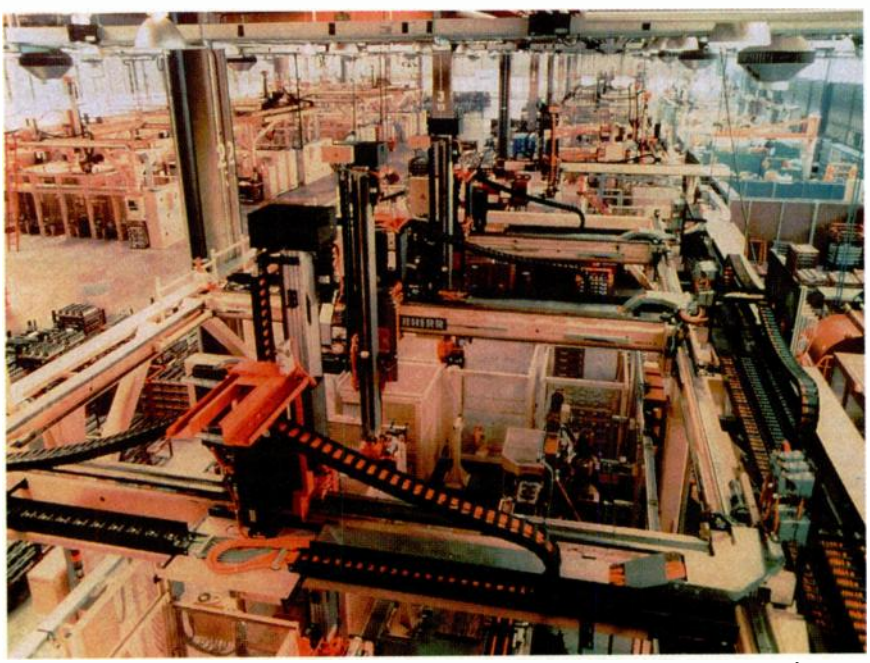
Cable Choices

There are eight main choices when it comes to flexible cable: continuous flex cable; torsional robotic cable; servo cable; flexible control cable; flexible data bus cable; European wire, cable, and cordage; European Unitronic electronic cable; and crane and conveyor system cable.

At the top of the flexible cable scale is continuous flex cable. This cable is designed for high-speed automated equipment applications such as industrial robots, pick-and-place machines, automatic handling systems, machine tools and conveyor systems. While it is possible to use standard control cables in these applications, they will not deliver the long-term performance required of cables designed exclusively for this purpose.

Torsional robotic cable is designed to perform in twisting and bending applications, without failure or fatigue, generally for more than two million cycles. Standard cables use coarse copper stranding and plastic materials that need only satisfy flame, voltage, and aging requirements. Torsional robotic cables also must meet these requirements—while at the same time withstanding long-term twisting.

Continuous flex and torsional robotic cables both must use resilient materials, so that once the cable completes a flexing cycle, the cables immediately return to their original unstressed



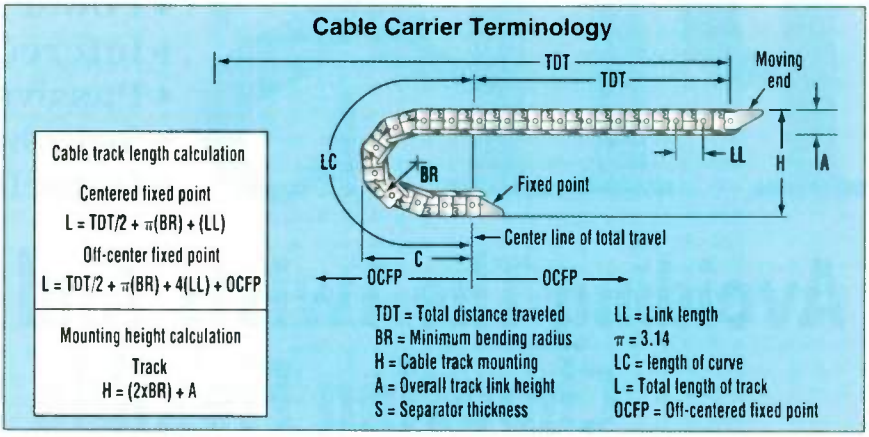
1. Despite its critical role in ensuring overall system reliability, cabling is just one step in the overall design process, and as such, is usually the last component to be speced in, even in the most sophisticated pick-and-place automation systems.

conditions. The copper conductors must be made of finely drawn strands rather than coarse strands. In addition, the cables must be designed so that the individual conductors inside the jacket have freedom to move, which prevents damaging stress to the conductors.

Servo cable comprises three different conductor types combined in one cable for power, signal, and control to servo motors that are used to obtain exact movement over large or small distances. Due to the nature of their use in factory environments, certain types of servo systems require cables that have a high flex-cycle life, and may contain several different gauge conductors. Power conductors drive the motor, while control conductors are required to direct the desired movements correctly. Feedback pairs, needed to indicate the position and orientation of the moving components, are used to connect motor temperature and revolutions-per-minute (rpm) monitoring instrumentation.

The environment these servo motors often operate in mandates the use of shielding to prevent electromagnetic interference (EMI) from distorting the precise control and feedback signals. If the feedback/control conductors or pairs are in the same servo cable with the power conductors, they must be individually shielded from EMI.

The fourth major flexible cable category, flexible control cable, permits easier handling and installation of control cable in confined areas of automated factories. Usually chosen for its adaptability in harsh environments, it can be unshielded, shielded with a tinned copper braid, or armored with galvanized steel braid. Some common flexible cable categories are multiconductor signal and control cable (as used in the processing industries, for example); high-temperature control cable (foundries, steel mills, glass factories, and high-temperature processes); and chemical-resistant cable (water and sewage treatment plants, chemical processing treatment plants, and food and beverage washdown applications).



2. The required bend radius of the cable, its overall construction, its travelling speed, and its anticipated flex life are all factors that must be considered when specifying flexible cable.

JACKET-MATERIAL RESISTANCE TO COMMON ORGANIC/INORGANIC CHEMICALS

Chemical	Concentration	Jacket Compound						
		PVC	PUR	Silicone	Teflon	Oil-resistant PVC	Neoprene	TPE-CRF
Sulfur	100%	A	A	C	A	A	A	Not tested
Hydrochloric acid	Conc.	A	A	B	A	A	A	A
Ethyl alcohol	100%	A	B	B	A	B	B	A
Blassocut		B	C	A	A	B	A	A
Machine oil		C	A	C	A	A	C	A
Methyl alcohol	100%	C	C	A	A	C	A	Not tested
Cutting oil		C	A	Not tested	A	A	C	A
Skydrol		C	C	C	Not tested	C	C	A

A = zero to slight reaction; B = slight to average reaction; C = average to strong reaction. Values are for 20°C.

Flexible data bus cable transmits data in high-speed, multitasking manufacturing environments via device-level networks that connect plant floor devices to control systems without the need for input/output (I/O) interfaces.

European wire, cable, and cordage, better known as "harmonized" cables, are ideally suited for use in electronic and electrical equipment designed for export to European countries adhering to European Committee for Electrotechnical Standardization (CENELEC) guidelines, while complying with CE directives. Harmonization cable standards apply to power-supply cable and hook-up wire. Specific color coding and cable-identification markings that differ from those cables meeting UL and CSA standards are required, and shielding is not permitted.

European Unitronic Electronic Cables are multipair cables that satisfy European standards such as VDE and DIN. They are used in electronics, communications, process control, and instrumentation applications.

Finally, cables for crane and conveyor systems are round, flat, and designed to meet the strength requirements of overhead cranes and materials handling systems. These cables are not governed by any specific standards.

Specifying Continuous Flex

The selection process for continuous flex cable is a critical part of a reliable system design—particularly for heavy-duty or harsh environments. At the top of the list of possible failure sources for any system troubleshooter is cabling and connections, regardless of the system. When specifying continuous flex

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cable, a number of factors must be taken into consideration:

• The required bend radius of the cable (*Fig. 2*). The overall construction of the cable, including stranding compounds, inner conductors, fillers, and jackets, influences the bend radius of the cable. A typical stationary flexible cable has a 15X or 20X bend radius, while a typical continuous flex cable's bend radius is 10X cable, and an ultra-flexible continuous flex cable's bend radius is only 5X the cable diameter.

• The traveling speed of the cable. This variable refers to the speed of the cable in the cable track. Any automated application where the traveling speed of the cable exceeds 6 feet per second demands that continuous flex cable be used either in or out of a cable track.

• The anticipated flex life of the cable. The cable's ability to flex long term is called the flex life, and represents the number of complete cycles the cable will travel in the cable track.

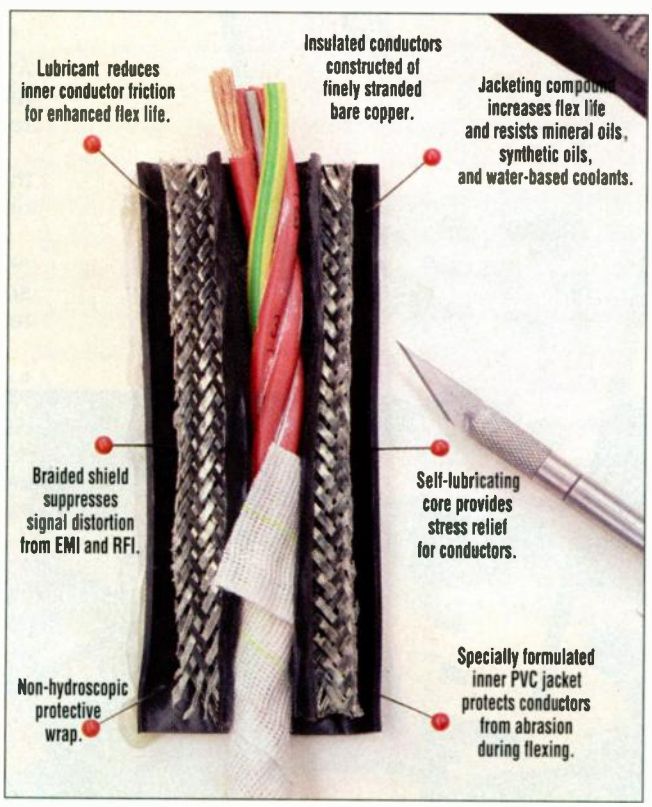
Cutaway

When a cable has to continuously flex or twist, it must be constructed with different materials and assembled in a manner that allows the conductors to have freedom of movement (*Fig. 3*). This capability is the direct result of a unique mechanical system that contains a number of moving parts. An essential aspect of a flexible cable's design is the spiral pattern in which the insulated conductors are combined. In addition, a conductor is never placed in the center of a continuous flex cable. Instead, a plastic filler is used in the center position. The filler is sized, as needed, to fit up to 12 conductors around it in a single layer. When a cable flexes, the insulation on conductors facing the outside of the bend will need to stretch, or slide, and the insulation facing the inside of the bend will have to buckle or slide.

The compound used in the cable's outer jacket, particularly its memory (resilience), is critical to achieve maximum flexibility. The jacket cannot relieve stress by sliding, so the memory becomes the critical flex endurance factor. The memory ensures that the jacket compound will return to the unstressed condition upon completion of the flex cycle. A compound with a poor memory will not completely return, but start with the next flex cycle in a stressed condition and be stretched further until it fails.

Copper stranding for continuous flex cables, in most cases, should be no larger than 34 gauge. The copper conductors—which can be either single or multipaired—are finely stranded and usually made of bare copper to allow the individual copper strands to move freely. They are encased in flexible insulating and jacketing compounds to increase flex life and provide optimum resistance to minerals and water-based and synthetic cutting fluids.

Depending on the application, continuous flex cables may be braided. In applications where electrical interference may distort signal transmissions or where the emissions need to be suppressed, a tinned-copper braid is recommended.



3. When a cable has to continuously flex or twist, it must be constructed with different materials and assembled in a manner that allows the conductors to have freedom of movement. This capability is the direct result of a unique mechanical system that contains a number of moving parts.

Jacketing Compounds

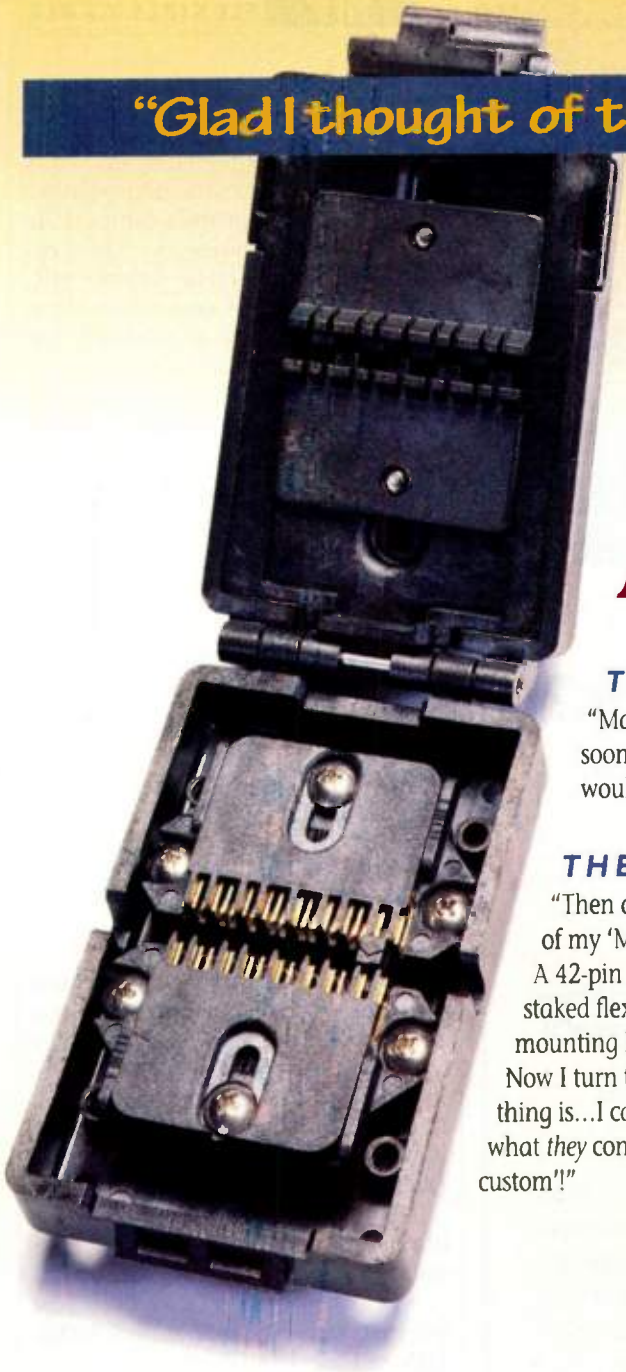
Jacketing materials are very important considerations for cable users. Chemicals and oils affect different jacketing materials in different ways, so it is important to understand both the operating environment and the characteristics of the jacketing materials before specifying cable (*see the table*). For example, polymeric plasticized PVC is good for oil resistance, polyurethane is suited for abrasive conditions, and certain TPEs are extremely chemical resistant. A slick surface jacket (untextured polyurethane) should be avoided, as it will cause adjacent cables to stick together in the cable track. If this occurs, one cable will be dominant and will force the other cable to flex without freedom of movement, causing both cables to fail.

Proper Installation

Care must be taken when installing cables in the flexible tracks that organize, guide, and support the cable during the flexing cycle. The cables and the track cannot interfere with other cables in the track. If the cables are separated from each other and tensioned correctly, they will not bend on the inner or outer arc surfaces of the track. Basic rules to follow include making sure there are no twists or kinks, allowing space of at least 10% of the cable diameter between cables, and making sure weight is evenly distributed with heavier cables on the outside. When a cable is correctly installed in a track, a flex life of 5- to 10-million completed flex cycles can be reached.

Continuous-flex cable track consists of two basic materials: metallic (steel) and nonmetallic (plastic). Steel track offers numerous design options for the most demanding carrier applications. It works best in temperatures up to 1200°F and can accommodate sharp or extremely hot debris. It is resistant to oils, gasoline, and coolants. Plastic

"Glad I thought of that!"



"Every time I need 'custom' interconnects, I go straight to my ARIES catalog."

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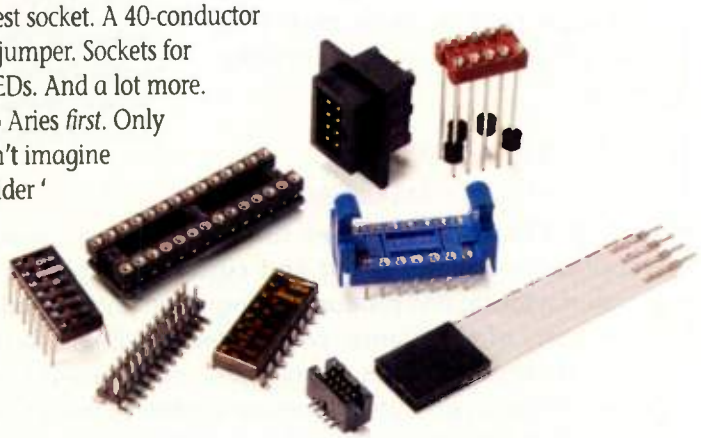

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track, however, is molded from high-strength, fiber-enforced nylon and is the most economical and innovative way to properly protect cables. It is usually self-lubricating, corrosion-resistant, nonconductive, lightweight, and durable. Unlike steel, plastic track cannot handle sharp or extremely hot debris. Its ideal application is in a working environment where temperatures range from -40° to 250°F. Just as with the cable itself, there are a number of environmental and operational factors to consider.

The Cost Factor

Even after equipment designers learn how and when to specify flexible cable, there is still the price issue. High-quality flexible cable is more cost-effective, especially if the cost-to-value analysis includes costs associated with lost production and cable replacement when incorrect cables are specified and installed.

In general, when specifying flexible cable, the design engineer needs to ask the following questions:

- What flexibility requirements does the machine's design and operation impose on the cable; namely, the cycle life?
- What is the working environment in which the machine will perform? Is the process oily, greasy, hot, or cold? Is it subject to radiation or open flame? Does it involve caustic chemicals?
- What are the electrical properties of the cable? Gauge size? Conductor count? Voltage rate?
- Does the machine have to satisfy international standards, such as VDE, DIN, or CE?

Richard A. Buchicchio has been marketing manager for Olflex since 1995 and is responsible for new and current product research and development. Prior to becoming marketing manager, Buchicchio worked for two years as an outside regional sales manager and for four years as a sales product specialist. He holds a BA in Political Science, with minors in Marketing and Sociology, from Rutgers University, New Brunswick, N.J.

How Valuable	Circle
Highly	577
Moderately	578
Slightly	579

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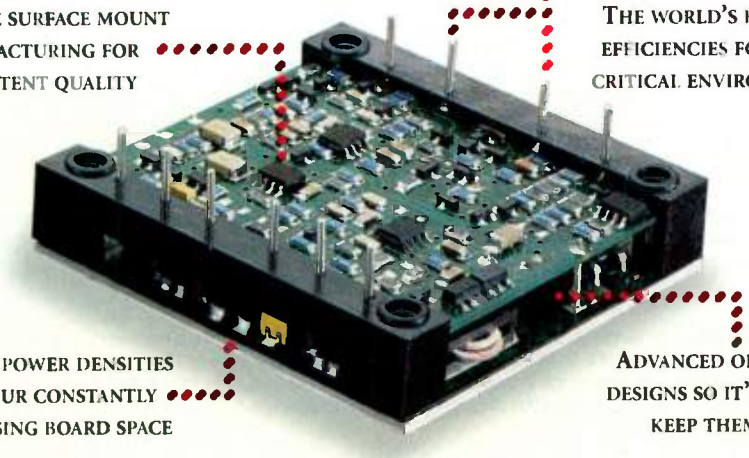

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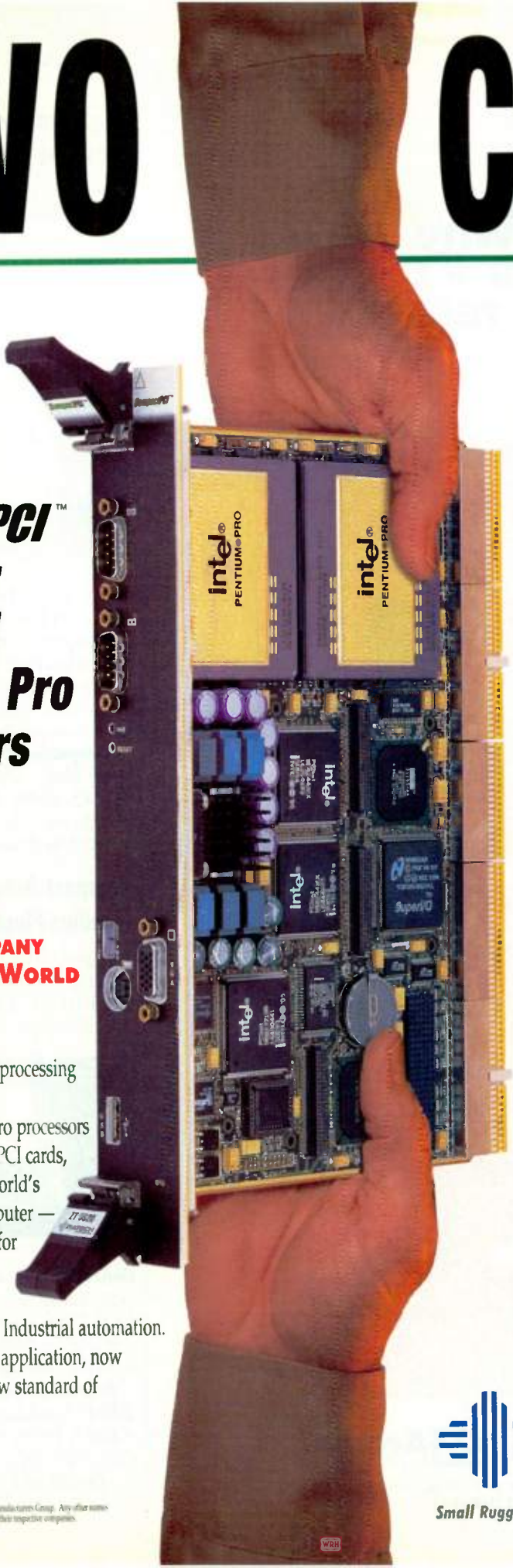
READER SERVICE 167

PRODUCT UPDATE: SENSORS

Manufacturer	Device	Description	Price & delivery	CIRCLE
Analog Devices **Norwood, MA** **Ray Stata Technology Center** **(617) 937-1428** **Fax (617) 821-4273** **http://www.analog.com**	TMP12 airflow and temperature sensor	This silicon-based sensor combines a self-heating element, a linear temperature sensor, and two user-selectable set-point comparators in a single eight-pin SOIC. The sensor operates off 5 or 12 V, and is specified for a temperature range of -40° to 125°C. The outputs can sink over 20 mA.	$1.95 each per 1000	580
Banner Engineering Corp. **Minneapolis, MN** **Sales (888) 373-6767** **Fax (612) 544-3213** **http://www.baneng.com**	Q10 dc photoelectric sensors	These self-contained 10- to 30-V dc photoelectric sensors come in a right-angle configuration with black ABS housings only 10-mm thick. Options include diffuse with a 20-in. range and opposed models with a 1.8-m range. Outputs can be NPN (sinking) or PNP (sourcing), and the operating temperature range is -40° to 70°C.	$60	581
Bourns Inc. **Riverside, CA** **Sales (800) X-DUCERS** **Fax (909) 781-5378** **E-mail: philip_butler@bourns.com** **http://www.bourns.com**	ST-2040 sapphire pressure sensor	This single-crystal sapphire pressure sensor guarantees accuracies of 0.25% and 0.50% FS, comes in ranges up to 1000 PSI, and is constructed of all corrosion-resistant materials. The stainless-steel-packaged device features a power consumption of 2.5 mA for 0- to 5-V dc, instant warm up, and a response time of 12 ms.	$199 each; six weeks ARO	582
DJ Instruments Inc. **Billerica, MA** **Michael Testa (508) 667-5301** **Fax (508) 667-6804** **E-mail: djisnt@aol.com**	Force/ deflection sensor	These force/deflection sensors are manufactured to specification by applying a strain gage transducer to a flat metal beam. The devices can exhibit 5- to 50-kΩ or less impedance and offer 4- to 8-mV/V output. Other features include up to 100 V excitation to measure from 50 g upward over the range of -60° to 150°C with 0.5% FS/yr stability.	$5 each in quantity	583
Dallas Semiconductor **Dallas, TX** **Michael Overlaur (972) 371-4448** **Fax (972) 371-3715** **http://www.dalsemi.com**	DS1624 digital thermometer and memory	The DS1624 is the first digital temperature sensor to feature 256 bytes of EEPROM on chip to store temperature compensation information. The 8-pin PDIP or SOIC device outputs temperature directly as a 13-bit 2's complement word. The temperature range is -55° to 125°C in 0.03125°C steps, and the accuracy is 0.5°C over 0° to 70°C.	$3.40 each per 1000	584
Efector Inc. **Exton, PA** **Sales (610) 524-2000** **Fax (610) 524-2010** **E-mail: info@efector.com**	quadronorm plus proximity switch	To ensure correct installation, this proximity switch comes with a setup LED. The two-wire dc device has four output functions: positive switching, normally open; positive switching, normally closed; negative switching, normally open; and negative switching, normally closed. The sensing ranges from 4 to 22 mm, depending on mounting.	$81 to $84	585
Exar Corp. **Fremont, CA** **Sales (510) 668-7000** **Fax (510) 668-7025** **http://www.exar.com/smi.htm**	SM5600 series pressure sensor	Available with a super-low pressure range of 0 to 0.15 psi, these sensors come in an 8-pin DIP, and are fully calibrated and temperature compensated over a range of 0° to 60°C. Versions are available for constant-current excitation mode (typically 1.5 mA) and for constant-voltage systems (typicaly 10 V).	$15 each per 1000	586
HiTech Technologies Inc. **Newtown, PA** **Sales (800) OEM-LEVEL** **Fax (215) 968-4515** **E-mail: info@hitechtech.com** **http://www.hitechtech.com**	SonicLaser ultrasonic proximity sensor	Available in 18 models, the UltraSonic proximity switch has a narrow beam of 2.5° off center axis and a range of 3.28 to 26.25 ft. The accuracy range is 0.08 to 0.2 in. The ultrasonic frequency ranges are 40, 60, or 160 kHz. depending on measuring range.	$231 to $390	587
Lucas Control Systems **Hampton, VA** **Sales (800) 745-8008** **Fax (757) 766-4297** **http://www.schaevitz.com**	PS-3300 series silicon pressure transducer	This "smart" pressure sensor comprises the company's ASIC with a silicon sensor in an IP65- and NEMA 4-compatible package. The ASIC provides both error correction and signal amplification. The sensor has its zero and span factory set at 0.25%, is available with a sensing range of 15 to 3000 psi FS, and operates over -40° to 125°C.	N/A	588
Motorola **Semiconductor Products Sector** **Denver, CO** **Carol Smith (602) 244-4556** **E-mail: R27828@email.sps.mot.com**	MPXT2010 pressure sensor	The MPXT2010 is an on-chip temperature-compensated and calibrated pressure sensor. The stress-isolated, piezoresistive device comes in a top-piston-fit package, has a range of 0 to 10 kPa, and has a full-scale span calibrated to 25 mV. The linearity is +/- 1.0% maximum.	$10.40 each per 10,000	589
Optek Technology Inc. **Carrollton, TX** **Application Support (972) 323-2200** **Fax (972) 323-2396** **E-mail: optek1@optekinc.com** **http://www.optekinc.com**	OHS3150U hall-effect sensor	This ratiometric, linear hall-effect sensor provides an output proportional to an applied magnetic field. The device has an operating temperature range of -40° to 150°C, and uses a quadratic hall sensing element and temperature-compensation circuitry.	$1.38 each per 1000	590
Opto Technology Inc. **Wheeling, IL** **Sales (847) 537-4277** **Fax (847) 537-4785**	OTR480 bar-code reader	This single-channel bar-code reader has better than 0.010-mil resolution. The device comes with a red or infrared emitter and a phototransistor in a single plastic housing. The operating temperature range is -40° to 85°C.	$5.14 each per 100	591
PCB Piezotronics Inc. **Depew, NY** **Sales (888) 684-0013** **Fax (716) 684-0987** **E-mail: sales@pcb.com**	Series 370 dc accelero-meters	The Series 370 accelerometers use variable capacitance sensing to achieve a sensitivity of 100 mV/g. All units come with air damping and are resistant to thermal transients and base strain. Operating off 16 to 28 V dc, all units are hermetically sealed and come with a titanium four-pin connector.	N/A	592
Victory Engineering Corp. **Springfield, NJ** **Sales (201) 379-5900** **Fax (201) 379-5982**	ISOTHERM thermistors	This line of matched sets of precision thermistors comes in five standard configurations ranging from 0.013-in. glass beads to 0.1-in.-diameter (max) glass probes. Available either in series or parallel, the sets come with various tracking options.	$9.95 each per 100; stock to eight weeks ARO	593

TWO COOL!



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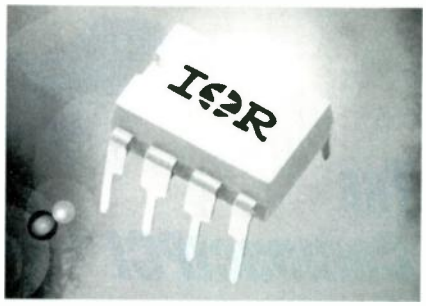
READER SERVICE 163

RELAYS

High-Current Telecom Relay Has Low On Resistance

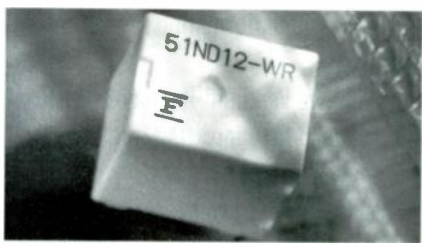
The dual-pole PVT322 photovoltaic telecom relay handles up to 170 mA per channel at an $R_{dd(on)}$ of 10 Ω (max). The maximum load voltage is ±250 V. The relay requires 2 mA of input LED current to actuate and has an optical isolation voltage of 4000 V_{rms}. Packaging is in a standard 8-pin DIP with either through-hole or gull-wing surface-mount lead terminations styles. Pricing starts at $3.21 each 10,000; samples are from stock, while production quantities take from eight to 10 weeks.



International Rectifier, *100 N. Sepulveda Blvd., 17th. Fl., El Segundo, CA 90245-4359; Pro Center (310) 252-7105; Fax-On-Demand (310) 252-7100; http://www.irf.com.* **CIRCLE 460**

Compact Automotive Relay Handles Flasher Loads

Designed with contact materials comprising a silver-indium tin-oxide alloy, the FBR51-WR flasher-lamp relay provides more than four million operations at 16 V dc with an in-rush current of 28 A. The relay measures 15.5 by 12.1 by 13.7 mm, weighs 6 g, and has a rated coil power of 600 mW. Pricing is $1.19 each per 1000; delivery is from stock.



Fujitsu Takamisawa America Inc., *250 E. Caribbean Dr., Sunnyvale, CA 94089; (800) 380-0059; fax (408) 745-4971; http://www.fujitsufta.com.*
CIRCLE 461

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- PBX Systems
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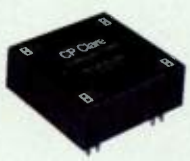

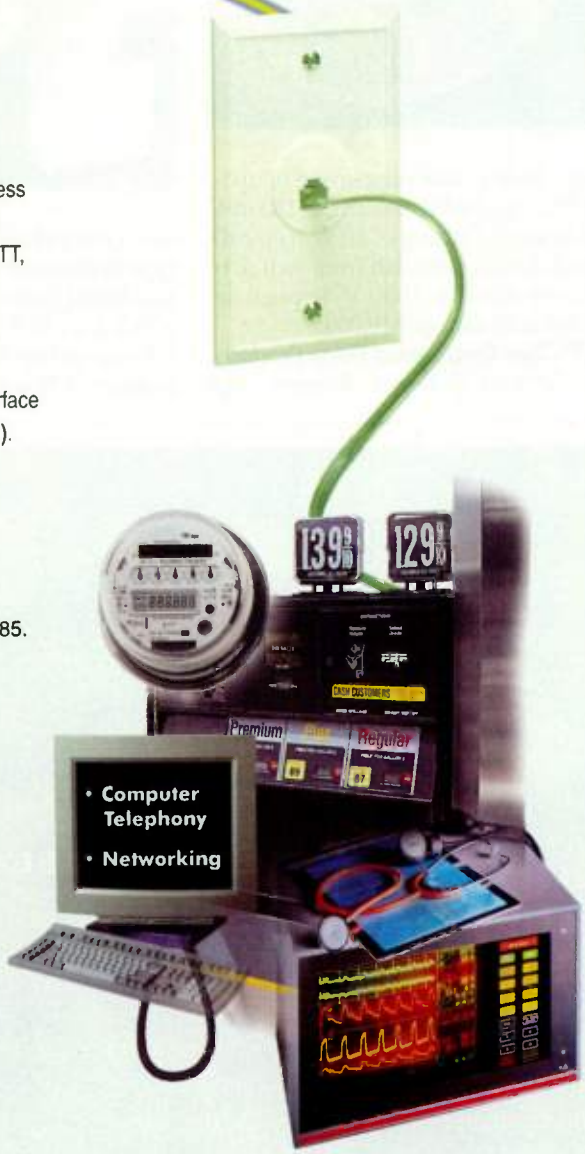

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READER SERVICE 99

RELAYS

Reed Relay Passes Signals At Frequencies Up To 1 GHz

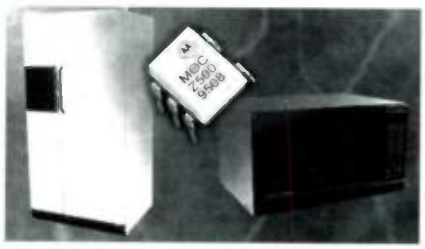
The ATE Series reed relay is capable of passing signals of up to 1 GHz with minimal distortion. Available with coaxial shielded 1 Form A and 1 Form C contacts for 50-Ω impedance matching, the

relays have a switching speed of up to 500 Hz, a contact resistance of 150 mW, and a contact rating of 10 W (typical). The dielectric strength from switch to coil and shield is 1000 V dc/peak ac. Pricing is $2 each per 10,000.

CP Clare Corp., Reed Relay Products, *78 Cherry Hill Drive, Beverly, MA 01905; Steve Christo (508) 524-6700; fax (508) 524-4700; Internet: http://www.cpclare.com.* **CIRCLE 462**

Optically Isolated Mini SSR Helps Protect Load

The MOCZ500 is a zero-crossing, optically coupled triac in a miniature DIL package. The first of a family of optically isolated ac power-interface circuits, the relay replaces up to five dis-



crete components. Features include a typical forward voltage drop of 1.2 V, a maximum current-handling capability of 0.5 A at 40°C, a minimum blocking voltage of 600 V, and a low, off-state leakage of 10 µA. Pricing is $0.50 each per 10,000; prototypes are from stock. Delivery is four weeks ARO.

Motorola, Semiconductor Products Sector, *MDZ207, 5005 E. McDowell Rd., Phoenix, AZ 85008; Steve Feist (602) 244-5406; fax (602) 244-5406; e-mail: rylp90@email.sps.mot.com.* **CIRCLE 463**

MOSFET Relays Come With A Variety Of Options

The G3VM line of MOSFET relays come in a four-pin configuration along with the standard 1 Form A six-pin and 2 Form A eight-pin configurations. The continuous ac, dc single, and dc parallel load current ratings are 120, 150, and 200 mA, respectively. The devices handle output voltages up to 350 V dc and have a maximum on-resistance of 35 Ω. Packaging is in standard surface-mount or through-hole. Pricing starts at $1.80 each per 1000 and delivery is from stock.

Omron Electronics Inc., *1 East Commerce Drive, Schaumburg, IL 60173; (800) 55-OMRON; fax (847) 843-8081.* **CIRCLE 464**

RELAYS

Electromechanical Relays Have Low Switching Resistance

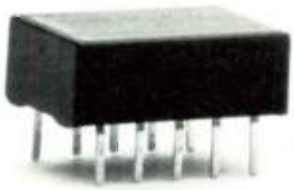
Available with coil voltages ranging from 5 to 48 V dc, the TC Series of electromechanical relays have a

switching resistance of 100 mΩ and consume 200 mW. Constructed with gold-palladium contacts, the fully sealed 2 Form C devices are rated at 30 W at 1.25 A and have a 4-ms operate time and a 1.5-ms release time. The devices are UL/CSA and BT approved. Pricing is from $1.25 each per 10,000.

GEM Electronics Inc., 5 Division St., East Greenwich, RI 02818; Todd La Londe (401) 885-8454; fax (401) 885-1741. CIRCLE 465

Sub-Miniature Relays Combine Low Profile With Low Power

The R74 series of miniature relays have a profile of 5 mm and consume 140 mW. The UL/CSA-approved relays handle up to 1 A and are available with coil



voltages of 3, 5, 6, 12, and 24 V dc and come in standard pc-board or surface-mount configurations with DPDT contacts. The devices weigh 0.05 oz, have a minimum mechanical life of 36,000 hours, and have a dielectric strength of 1000 V ac between coil and contacts. Pricing is under $3.50 each per 1000.

NTE Electronics Inc., *44 Farand St., Bloomfield, NJ 07003; William Horstmann (201) 748-5089; QuickFACTS (800) 683-3292, document #451.* CIRCLE 466

Pc-Board Mount Solid-State Relay Handles High Currents

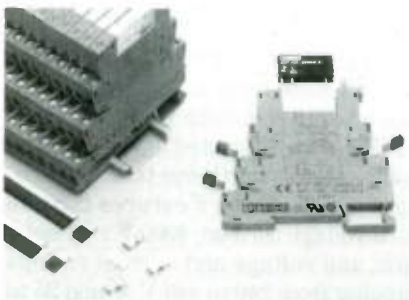
The LR1200480D40 is a dc-controlled ac solid-state relay capable of controlling up to 40 A at a line voltage of 480 V ac. The board-mounted device uses the company's Powertherm thermal management process. Features include zero-voltage turn-on, 4000 V rms isolation, and voltage and current ratings ranging from 240 to 480 V ac and 25 to 40 A, respectively. Measuring 1.4 by 1.12 in., the relay comes in a plastic package with Option-08 surface-mount leads. Pricing starts at $14.60 each per 500; delivery is stock to eight weeks.

Teledyne Relays, *7345 E. Acoma Rd., Scottsdale, AZ 85250; Paul Glenney (213) 241-1225; fax (213) 779-8161; http://www.teledynerelays.com.* CIRCLE 467

RELAYS

Slim, Pluggable Relays Facilitate Bridging

The PLC-REL relay module comes with three key features: a slim, 6.2-mm-wide package; a pluggable interface; and a bridging system that requires no tools and that can be used to jumper coil commons together to reduce wiring time. The device can be either electromechanical with a 6-A Form C contact, or solid-state with a 2-A switching capacity. No external power distribution terminal blocks are required, thereby saving 12 mm of DIN rail for every set of relay contacts. Pricing is approximately $16 each and delivery is from stock.



***Phoenix Contact Inc.**, P.O. Box 4100, Harrisburg, PA 17111; Technical Service (800) 322-3225; fax (717) 944-1625; e-mail: info@phoenixcon.com.*
CIRCLE 468

Low-Profile Relay Can Switch 16-A Loads

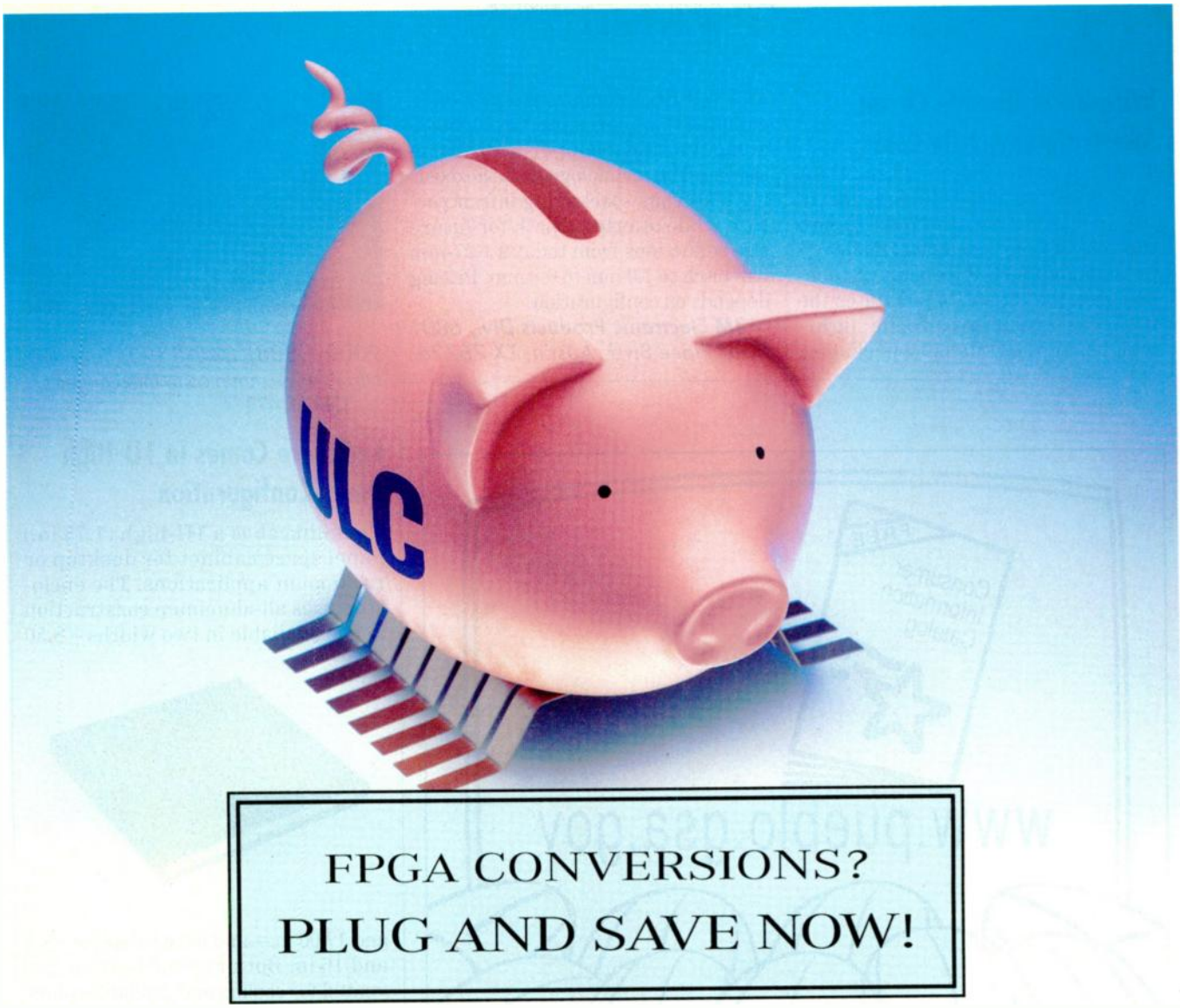
Measuring only 15.7 mm high, the RT series dc coil relay comes with silver-nickel contacts and can switch up to 16 A at 240 V ac or 10 A at 28 V dc. The compact device has a footprint of 3.68 cm^2 and comes with contact configurations of SPST NO to DPDT. The relay operates off voltages from 5 to 48 V dc and consumes 400 mW (nominal). Options include a sealed, immersion-cleanable case with knock-off nib or a flux-tight, top-vented plastic case. Pricing is $1.50 each per 1000; delivery is from stock to 10 weeks.

***Siemens Electromechanical Components Inc., Potter & Brumfield Div.**, 200 South Richland Creek Dr., Princeton, IN 47671-0001; Mark Rine (812) 386-2559; fax (812) 386-2072; e-mail: info@sec.siemens.com.* **CIRCLE 469**

High-Sensitivity Relays Have Low Thermal EMF

The TXS line of polarized relays measure 15 by 7.4 by 8.2 mm and come with a thermal EMF as low as 0.15 µV. The high-sensitivity relays come with 2 Form C contacts and can switch up to 1 A at 30 V dc. The initial contact resistance is rated at 100 mΩ (maximum).Relay versions are available for 1.5- to 24-V dc operation with single-side stable, one-coil, and two-coil latching operating functions. The nominal operating power for one-coil latching is as low as 35 mW. Pricing is $2.41 each per 1000 and delivery is stock to 11 weeks.

***Aromat Corp.**, 629 Central Ave., New Providence, NJ 07934; (800) AROMAT9; fax (908) 771-5658; or on the Internet at http://www.aromat.com.*
CIRCLE 470



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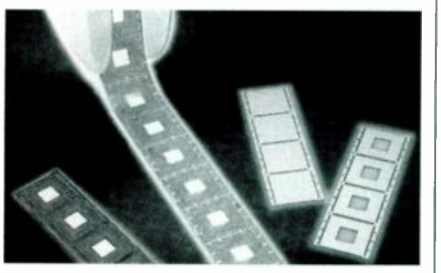
READER SERVICE 109

Wire-Bond Flexible Circuit Substrate Saves On Cost

The Microflex wire-bond tape BGA (WB BGA) is a wire-bond-based flexible circuit substrate. Designed to curb the cost of flex-based, thermal compression bond IC interconnect technologies, the substrate facilitates the manufacture of low-profile, lightweight, high I/O-density packages. The WB BGA comprises a microflex circuit, a thin thermoplastic polyimide adhesive, and a copper lead-frame stiffner. The technology uses the existing leadframe-packaging infrastructure while offering a path for future size reductions from today's 1.27-mm ball pitch to 1.0 mm to 0.8 mm. Pricing depends on configuration.

***3M Electronic Products Div.**, 6801 River Place Blvd. Austin, TX 78726-9000; (888) 845-3393; Internet: http://www.mmm.com/interconnects/.* **CIRCLE 471**



Enclosure Comes In 1U-High Panel Configuration

The Slimcab is a 1U-high (1.75 in.) panel space cabinet for desktop or rackmount applications. The enclosure uses all-aluminum construction and is available in two widths—8.50 and 17.00 in.—and in two depths—8.0 and 16 in. Both top and bottom are vented for cooling and available colors are sand texture or smooth black. Pricing ranges from $40 to $115.

***Bud Industries Inc.**, 4605 East 355th. St., Willoughby, OH 44094; Blair Haas (216) 946-3200; fax (216) 951-4015; http://www.budind.com.* **CIRCLE 472**

Rugged Axial Flow Fan Is Ultra Thin

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***Oriental Motor USA Corp.**, 2510 W. 237th. St., Suite 102, Torrance, CA 90505; Sales Dept. (800) 816-6867.* **CIRCLE 473**

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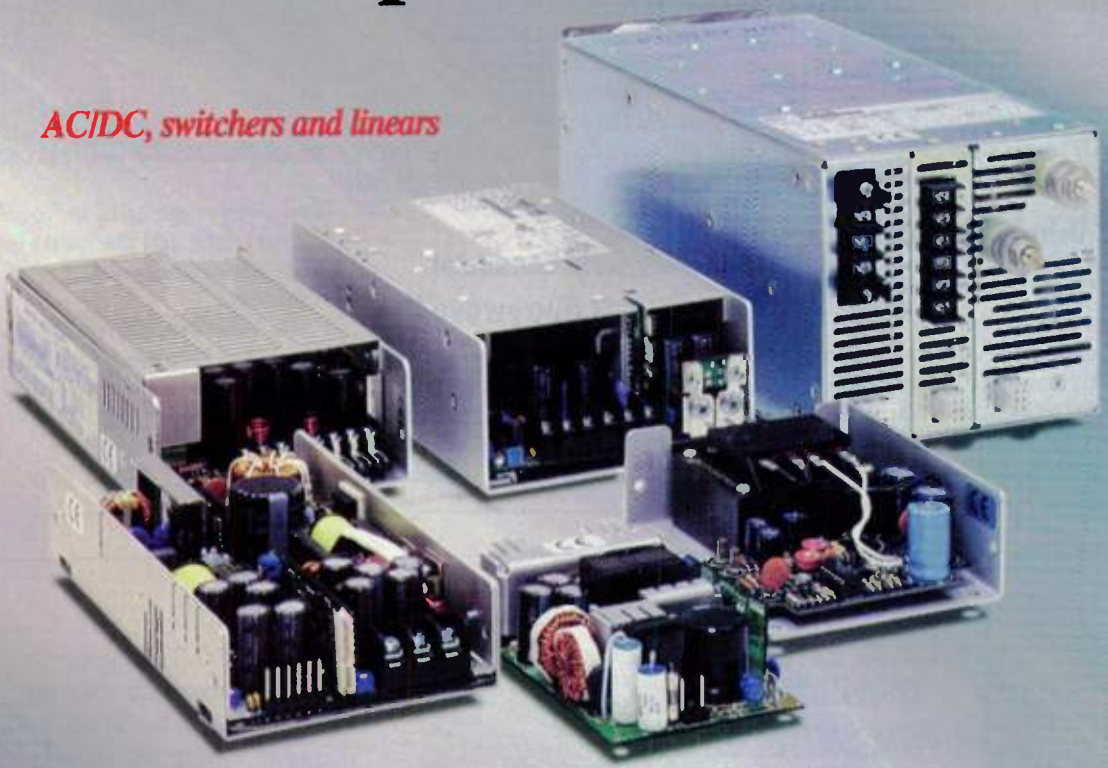

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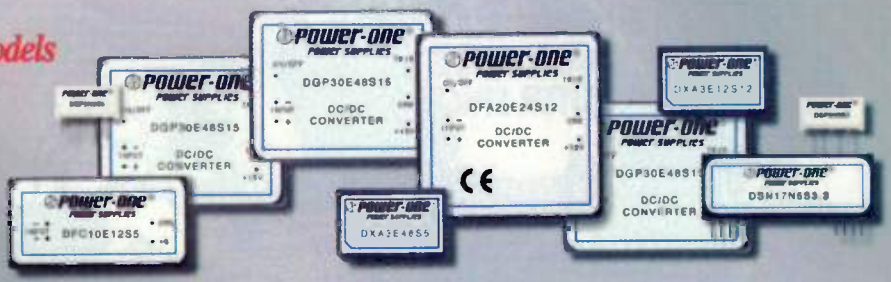

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Aavid Thermal Technologies Inc., *One Kool Path, P.O. Box 400, Laconia, NH 03247-0400; (603) 528-3400; Internet: http://www.aavid.com.* **CIRCLE 474**

Rugged 1U To 12U Chassis Are Low In Cost

Ranging in size from 1U to 12U, the BoxFlex line of rugged benchtop and rackmount chassis come with standard fan holes and optional fan kits. All chassis are EIA 19-in. rack mountable and come with removable feet, handles, and fan covers. The boxes use 14-18 Ga cold rolled steel construction and come with 1/16 to 1/8-in. aluminum front/back plates. Pricing ranges from $50 to $300 and delivery is from stock.

Hyperlab Corp., *330 Millway Ave., Concord, Ontario, Canada L4K 3W2; Andrew Calkin (905) 761-0055; fax (905) 761-6203.* **CIRCLE 475**

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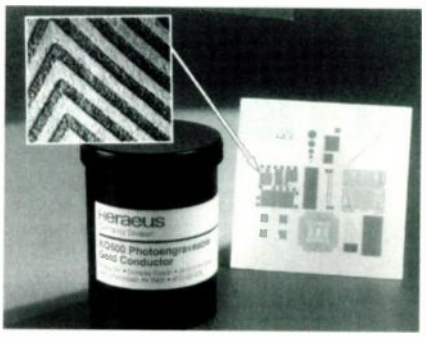
The KQ500 gold conductor paste is designed to produce extremely dense fired films with very smooth surface finishes for microstrip lines and microwave components. The paste is applied using conventional screen printing and photo-engraving techniques. Properties include a particle size ranging from 0.3 to 1.0 microns, a firing temperature range of 700° to 900°C, and a coverage of 12 in.^{2}/g. Minimum lots are 50 g and the material is guaranteed for six months from date of shipment.



Heraeus Inc., Cermalloy Div., *24 W. Union Hill Rd., West Conshohocken, PA 19428; Christina Kistler (610) 825-6050; fax (610) 825-7061; Internet: http://www.4hcd.com; e-mail: cbk@4hcd.com.* **CIRCLE 476**

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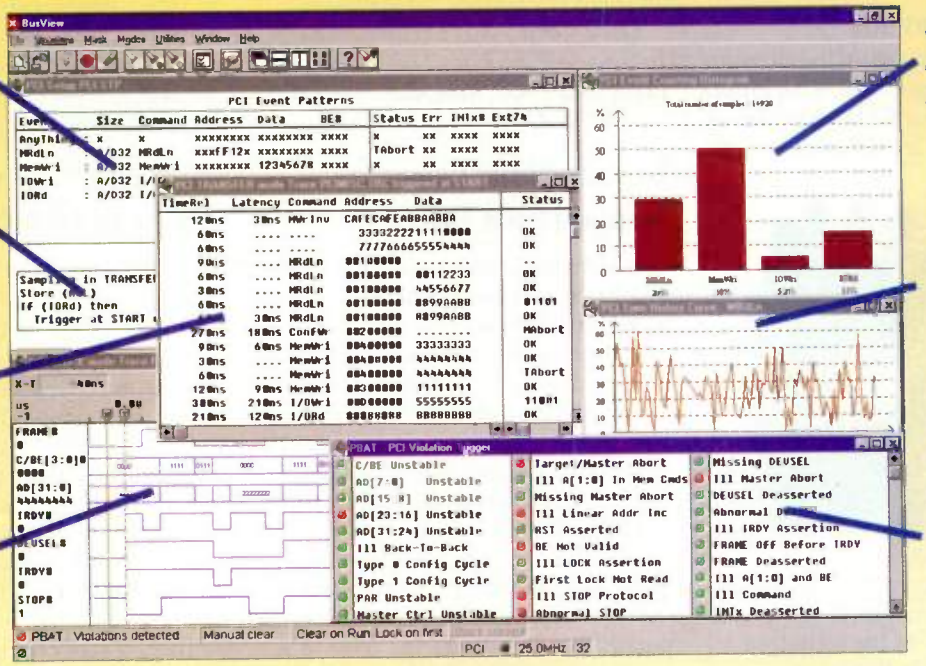

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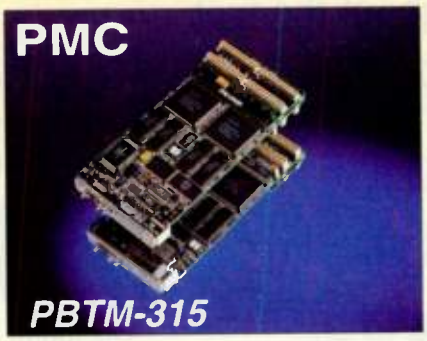

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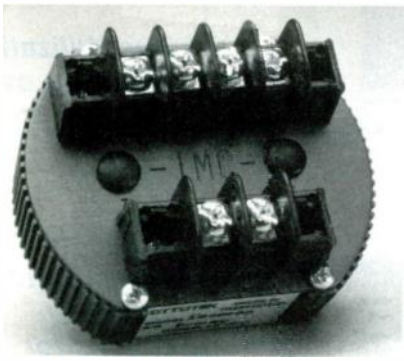
Current-Loop Transmitter Has Many Input Options

The Model 50 is a two-wire current-loop process transmitter with inputs for a thermocouple, RTD with open-element detection, resistance, mV dc,



and a strain gauge with internal/external excitation. The transmitter runs off 12 to 40 V dc, has an output accuracy of ±0.01% FSR, and a zero and span range of ±50%. The response time is 10 ms and packaging is in a 100% metal housing with DIN-rail clip or panel-mount options. Pricing is $75 and delivery is stock to four weeks.

***Otek Corp.**, 4016E Tennessee St., Tucson, AZ 85714-2130; Otto Fest (520) 748-7900; fax (520) 790-2808.* **CIRCLE 477**

Servoamplifier Comes In Eurocard Form Factor

The Model 4015 servoamplifier comes in a Eurocard form factor for export to Europe. The servoamplifier drives brush-type servomotors from a single-polarity 18- to 55-V dc supply and delivers ±10 A peak and ±5 A continuous. Other features include a 25-kHz switching rate, the ability to drive motors with inductances ranging from 400 µH to 40 mH, and bicolor LED status indication. Protection includes overload, overtemperature, and under/over supply voltage. A 16-pin component header allows the user to set peak current values and to match amplifier to motor inductance. Pricing is $246 each in quantity and delivery is from stock to four weeks ARO.

***Copley Controls Corp.**, 410 University Ave., Westwood, MA 02090; (800) 659-2675; fax (617) 329-4055; e-mail: sales@copleycontrols.com; Internet: http://www.copleycontrols.com.* **CIRCLE 478**

AC Brushless Drives Handle From 4 To 70 A Continuous

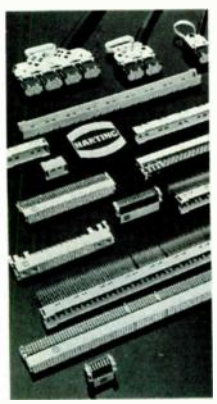
The SP Series of ac brushless servodrives comprises models ranging from 4 to 70 A continuous. The series is complemented by a line of performance-matched neodymium iron-boron permanent-magnet servomotors that range from 3 in.-lb to over 1000 in.-lb continuous torque. Features include feedback loss detection, open-collector I/O, and standard normally open and normally closed signal interfacing. Pricing for a system with an 83-in.-lb motor is less than $1800; delivery is stock to three weeks.

***Westamp Inc.**, 9006 Fullbright Ave., Chatsworth, CA 91311; Brad Landseadel (818) 709-5000 ext.203; fax (818) 709-8395.* **CIRCLE 479**

har-bus®64 New 160 Pin Connector For VME64

New series satisfies the new 64 bit computer architecture's requirement for higher speeds, more I/O and additional functionality. Offering a five row connector solution that is 100% backward compatible with the popular 96-pin Eurocard connectors, the new ***har-bus® 64*** has 160 pins with preleading contacts for live insertion. New contact rows can be used to improve signal speed of VME bus and as ground contacts. Current 96-pin Eurocard connectors mate to the 160 pin connectors, allowing all PCB's to be used in new or existing backplanes.

READER SERVICE 227



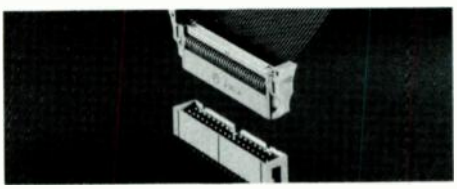
har-pak® 2.5MM High Density Connector System

Developed for backplane and daughter board applications in modern rack systems. The 5 row 2.5 mm connector design offers solderless PCB terminations, optimum utilization, of space three dimensional modularity, high contact density, EMI protection, and the ability to double-side surface mount components on daughter cards without loss of a 15mm card pitch. The *har-pak* connector system permits using a three dimensional 2.5mm grid. Only one connector style is required to solve your power, signal, ground, and high data rates, simplifying the design and manufacturing of future systems. The compliant pin technology utilizes the same 1mm plated through hole standard for many DIN 41612 compliant pin technologies. Consistency in design uses the many years of manufacturing and design experience already available. These attributes combined can lead to new advancements in board-level designs: 15mm card pitch with double-sided surface mounted daughter cards, butterfly or mid-plane techniques, modular design both horizontally and vertically, low number of system components combination with other standardized packaging systems, and lower applied costs.

READER SERVICE 228

New SEK "Press'n Snap" Press in Header

Low profile press-in headers can be added to single or double-sided surface mount printed circuit boards any time after reflow. Press-in terminations of the two row .100" pitch headers permit easy installation into plated through holes without soldering. Removable temporary inserts allow any flat die to press the connectors. The straight header is shrouded by four plastic walls and available in versions from 6 to 64 contacts. The mating connectors are flat ribbon terminated socket connectors from HARTING's SEK range. These can be latched to the headers by using the locking levers installed onto the strain relief. The levers secure the socket connector to the end walls of the



header. Placing the locking levers on the socket instead of the PCB header saves valuable board real estate.

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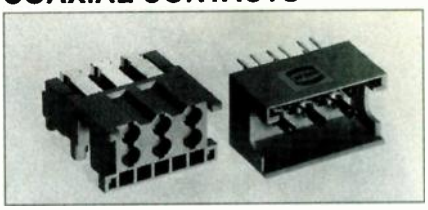
NEW HIGH DENSITY MICRO-COAXIAL CONTACTS



Designed for high speed data transfer rates. Can be used in the iec 1076-4-2 2.5mm High Density connector system, *har-pak*® Provides more space efficiency, high frequency capability, easy handling, low applied cost and application with current equipment and emerging metric equipment practices. Designed for PCB termination on both daughter card to backplane connection; allowing users to bring signal directly into the backplane without a cable transition.

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har-bus 64
CIRCLE 231

har-mik har-press®

CIRCLE 232

The new ***har-mik har-press®*** SCSI 3 connector with compliant pins is flat rock, and can be inserted into a PCB with one stroke of a press. Eliminates soldering and saves time. The 68-pin, receptacle vertical mount connector is made of liquid crystal polymer, a high temperature resistant material which allows use of IR reflow for SMT components, with no danger of damaging the connector. Compliant pins fit into finished, plated through holes of 0.022" to 0.027".

har-pak®
CIRCLE 233

Need high pin count equal to the Future bus +4 row 2.0 mm connectors that can withstand robust handling and assembly? ***HARTING'S har-pak®*** 2.5 mm connector system with greater contact spacing provides superior high frequency performance.

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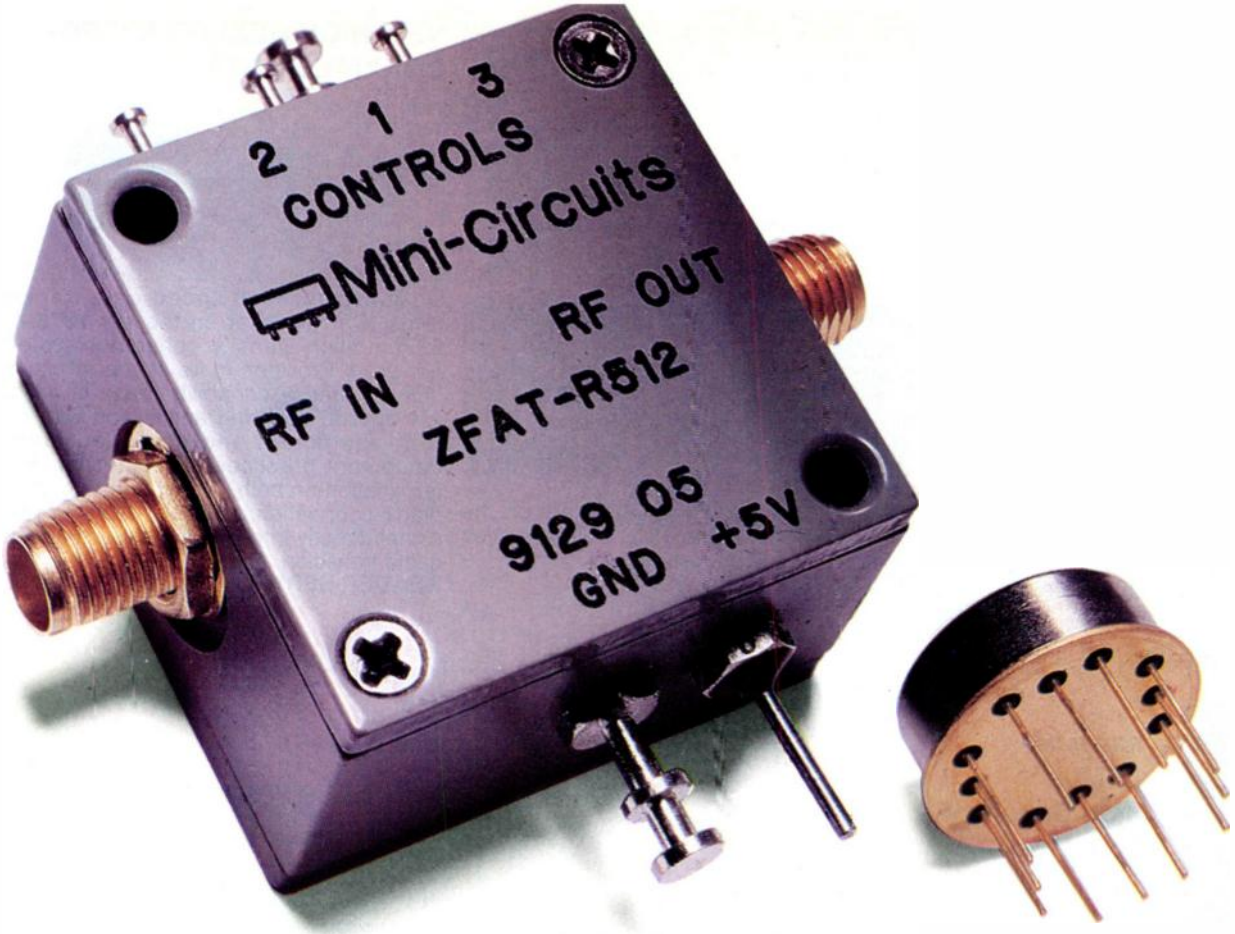

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1.5	0.32	3.0	0.4	9.0	0.6	12.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**16.0**	**0.5**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	20.0	0.8	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	24.0	0.8	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	28.0	1.1	35.0	1.0

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bold faced values are individual elements in the units

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Circle 520

π Filter Has Notch Just Outside Passband

JIM HAGERMAN
Science & Technology International Inc., 733 Bishop St., Suite 3100, Honolulu, HI 96813.

Some applications such as antialiasing could benefit from a lowpass filter with a notch just outside the passband. The filter in Fig. 1 is a Cauer or Elliptic type, but with a source impedance of zero. Typically, these filters as given in texts have a normalized source impedance that results in a –6 dB voltage gain. Through trial and error, I arrived at the coefficients as shown, which is why I chose to call it a π filter.

The filter has some useful properties *(Fig. 2)*. For instance, dc gain is exactly 0 dB with no offset, and is independent of component tolerances. The passband is flat with a 1-dB peak at about $0.8 \times f_{ref}$. The corner frequency f_{ref} is at –0 dB and the notch frequency is exactly $2 \times f_{ref}$.

The "T" configuration was chosen to accommodate conversion to an op-amp active filter. The filter is first transformed by multiplying all components by 1/s *(Fig. 3)*. Inductors become resistors, resistors become capacitors, and capacitors become frequency-dependent negative resistors (FDNRs). An FDNR is easily implemented with two op amps. The final filter schematic has its component values and corner frequency scaled in the normal fashion *(Fig. 4)*.

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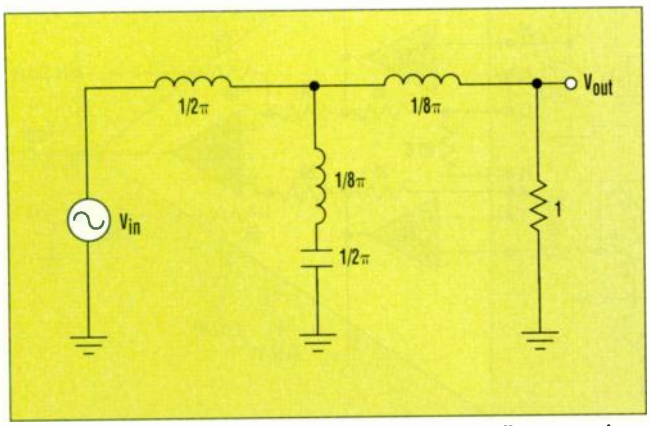
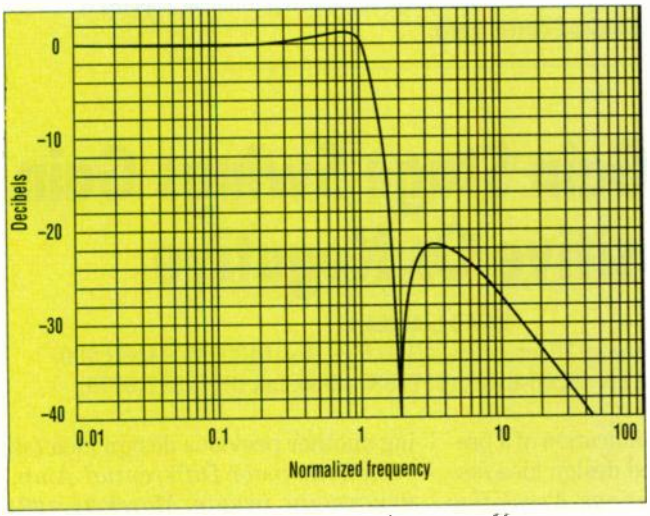
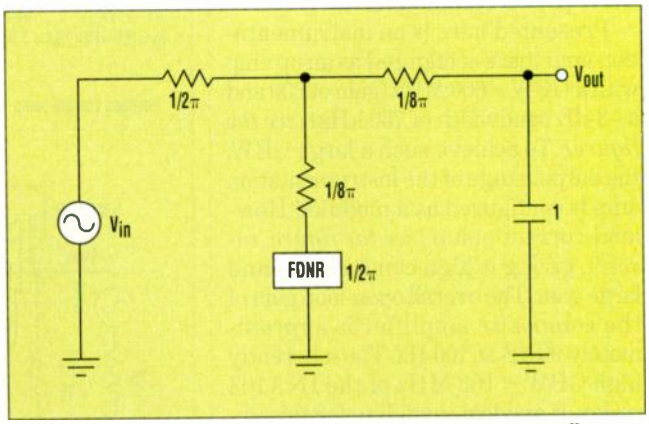


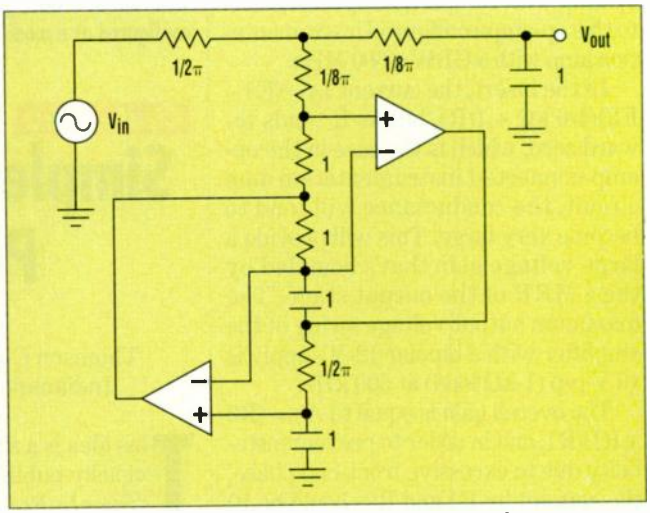
1. This normalized passive π filter, which is a Cauer or Elliptic type, has a source impedance of zero.



2. The normalized frequency response for the Figure 1 filter demonstrates the flat passband response and notch at exactly f_{ref}.



3. The transformed version of the filter shown in Figure 1 has all components multiplied by 1/s.



4. In the final filter setup, component values and corner frequency are scaled in the normal fashion.

Circle 521

Instrumentation Amp Turns Into 600-MHz Gain-Bandwidth Op Amp

KLAUS ACHLEITNER
University of Cape Town, Dept. of Chemistry, Rondebosch 7700, Cape Town, South Africa; phone: +27-21-650-2525; fax +27-21-689-7499; e-mail: klaus@psipsy.uct.ac.za.

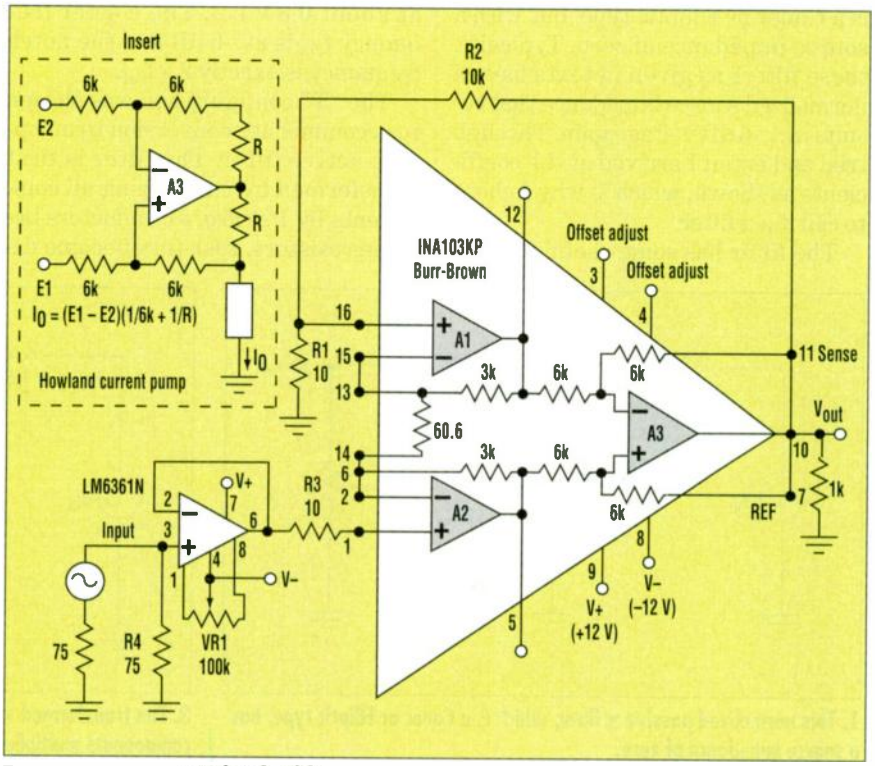
An interesting but brief mention is made in Analog Devices' AN-245 application note (by Scott Wurcer and Walt Jung) that instrumentation amplifiers can be configured as op amps with very high gain-bandwidth (GBW) products. In applications that use wide-band transducers, it's necessary to use high-GBW-product amplifiers.

Presented here is an instrumentation amp that's configured as an op amp with a GBW = 600 MHz (gain of 800 and a –3-dB bandwidth of 750 kHz) *(see the figure)*. To achieve such a large GBW, the output stage of the instrumentation amp is configured as a modified Howland-current pump *(see the figure, insert)*, giving it high conductance and large gain. The overall open-loop gain of the composite amplifier is approximately 90 dB at 100 Hz. The inherently high GBW = 100 MHz of the INA103 makes it an ideal candidate for this unusual application of using this device as an op amp. It's difficult to find a low-cost op amp with comparable specifications to this op-amp-configured instrumentation amp with a GBW = 600 MHz.

In the insert, the current $I_O = (E1 - E2)(1/6\ k\Omega + 1/R)$, but as R tends toward zero, which is the case in the op-amp-connected instrumentation amp circuit, the conductance will tend to become very large. This will provide a large voltage gain that's bounded by the CMRR of the output stage. The maximum output voltage swing of the amplifier with a bipolar 12-V supply is 16 V p-p (1-kΩ load) at 500 kHz.

The overall gain is equal to $A_V = (R2 + R1)/R1$, and in order to prevent instability due to excessive front-end phase, the gain set by R1 and R2 should be 10 times greater than the front-end gain, which in this case is strapped to 100. The front-end phase makes the op-amp-connected instrumentation amp only viable with large closed-loop gain settings.

Resistor R3 ensures that the source resistances presented to the instrumentation-amp inputs are equal. The dc offset at the output V_{out} can be nulled by adjusting RV1. The LM6361N high-speed op amp, which has a GBW = 50 MHz, can be used as a buffer amplifier or to provide additional gain. The LM 6361N should be replaced with a wide-band JFET type if the source impedance of the transducer used is high.



To attain 600-MHz gain-bandwidth, the output stage of the instrumentation amplifier is configured as a modified Howland-current pump.

Circle 522

Simple Gain Stage Swings Gain Positive Or Negative

DAVID L. ALBEAN
Thomson Consumer Electronics, CIR, P.O. Box 6139, M/S INH 700, Indianapolis, IN 46206-6139; (317) 587-4950; fax (317) 587-6779.

This idea is a simplification of a previously published design idea *(see "Single Pot Swings Amplifier Gain Positive Or Negative,"* ELECTRONIC DESIGN, *Jan. 20, p. 153)*. By using another previous design idea *(see "One Transistor Differential Amp,"* ELECTRONIC DESIGN, *March 21, 1994, p. 104)*, the circuit can be built with just one transistor—no op amps are

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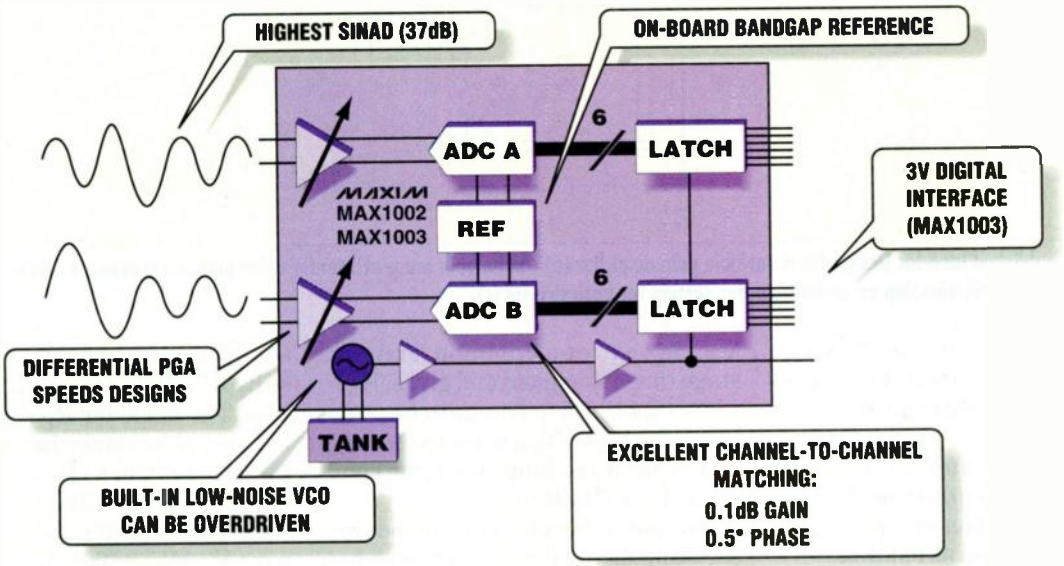

Ideal for such applications as digital set-top boxes, I/Q demodulators, and instrumentation, Maxim's new 6-bit dual ADCs offer the highest performance for the price. Both the 90Msps MAX1003 and the 60Msps MAX1002 are available in space-saving 36-pin SSOP packages.

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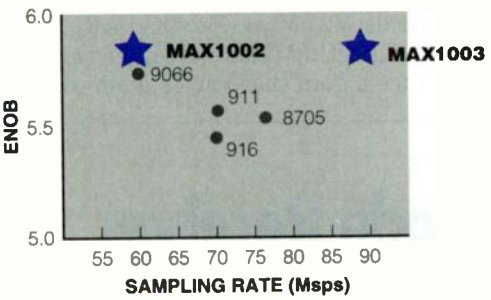

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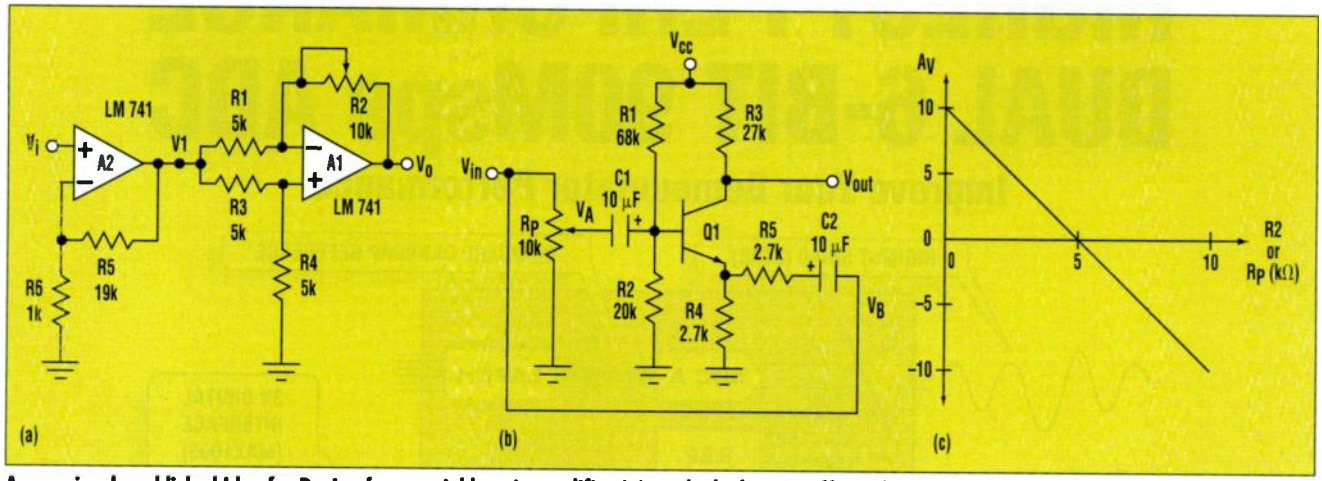

An previously published Idea for Design for a variable gain amplifier (a) can be built more efficiently using just one transistor and no op amps (b). Also given is the gain relationship vs. potentiometer setting for both circuits (c).

required. Thus, a gain which swings from positive to negative can be achieved with just one transistor.

This circuit *(see the figure, b)* operates exactly the same as the more complex (two op amp) circuit *(see the figure, a)*. The simpler circuit *(see the figure, b)* is analyzed as follows:

By superposition, the output voltage of the circuit takes the form: $V_{out} = K_A \times V_A + K_B \times V_B$, where K_A and K_B are constants determined by resistor ratios. Note that V_A and V_B only differ by the scale factor introduced via R_P. That is, $V_A = K_P \times V_{in}$ and $V_B = V_{in}$.

The gain experienced by V_A to V_{out} is that of a common-emitter stage (inverting gain) and gives: $K_A = -R3/(R4 \,||\, R5)$. The gain experienced by V_B to V_{out} is that of a common base stage (non-inverting) and gives: $K_B = (R3/R5)$.

The potentiometer (R_P) introduces the scale factor K_P, which varies between 0 (wiper at bottom) to 1 (wiper at top) and scales the V_A contribution to V_{out}. The wiper at the bottom setting results in a gain of +10, while the wiper at the top results in a gain of –10. Combining the above relations yields: $V_{out}/V_{in} = (K_P \times K_A) + K_B$.

Selecting resistor values to produce a gain that varies from –10 to +10 gives: $K_A = 20$, $K_B = 10$. As a result, R3= 27k, R4 = 2.7k, and R5 = 2.7k. The value for R_P is non-critical, but should be somewhat smaller than the bias network (R1 and R2) to reduce the loading effect of the base circuit. The overall gain expression is now: $V_{out}/V_{in} = -20 \times K_P + 10$. R1 and R2 are selected to set the desired bias current in Q1.

Any other arbitrary gain range can be implemented by properly choosing the various resistors and ratios to set K_A and K_B as desired. R4 may be acbypassed with an appropriate resistor if the biasing and ac gain requirements necessitate doing so.

Circle 523

Small Photodiode Receiver Handles Fiber-Optic Data Rates To 800 kbits/s

ROGER KENYON
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

A photodiode combined with two op amps and a comparator helps form a fiber-optic receiver capable of data rates to 800 kbits/s *(Fig. 1)*. Small packages (SOT23-5 for the op amps; µMAX-8 for the comparator) minimize the required real estate on a pc board or hybrid substrate.

The photodiode operates in the photoconductive mode, producing a signal voltage at IC1 with a transimpedance gain that's equal to the value of R1 (4.7 kΩ in this case). The op amps (IC1 and IC2) are configured as noninverting amplifiers with gains of approximately 25 V/V each, so the circuit's overall transimpedance gain is just under 3 MΩ: 4700 Ω × 25 × 25 = 2.99 MΩ. The op amps' gain-bandwidth capability sets the maximum practical data rate at 800 kbits/s.

Capacitive coupling between IC1 an IC2 negates the amplification of IC1's offset voltage. To achieve an optimum signal amplitude and symmetry, the R6/R11 divider sets IC2's

IDEAS WANTED

Submissions to this section should be about one type-written page of text, with 1-2 diagrams. They should be the author's original work, be tested, and not have been published previously.

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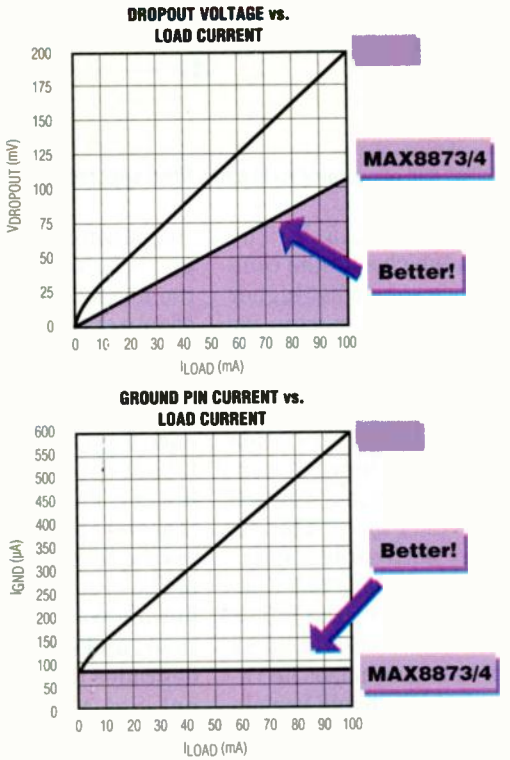

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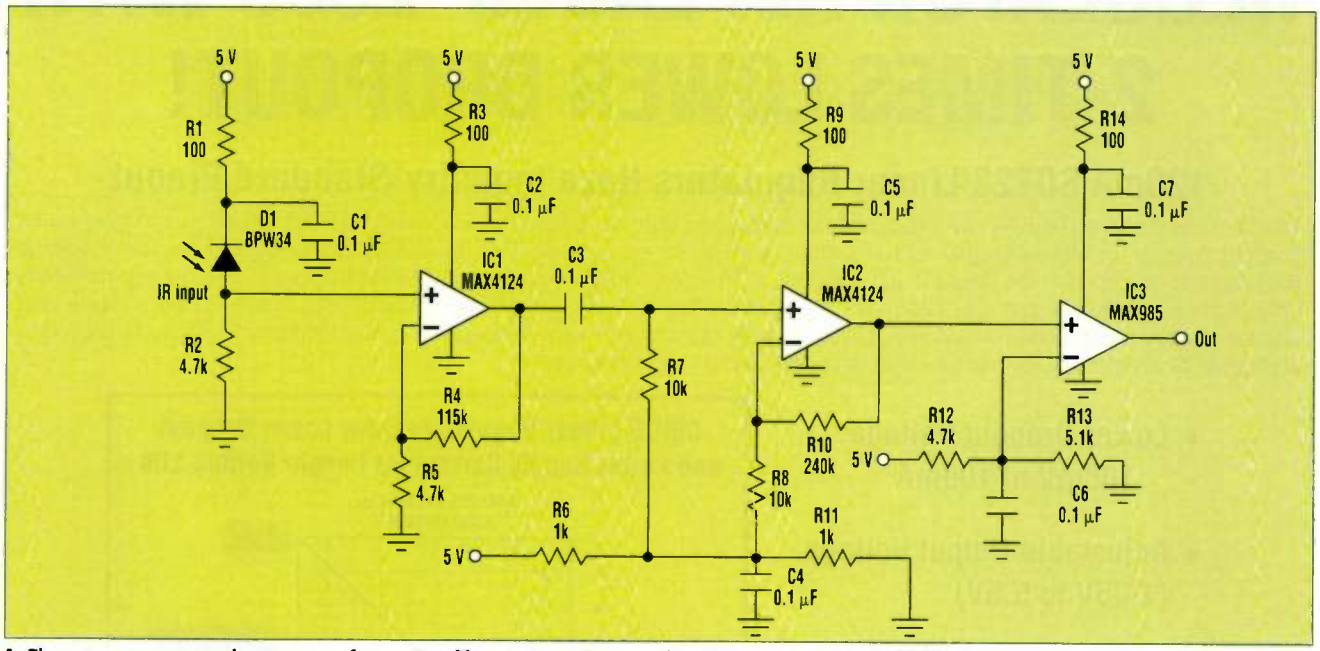


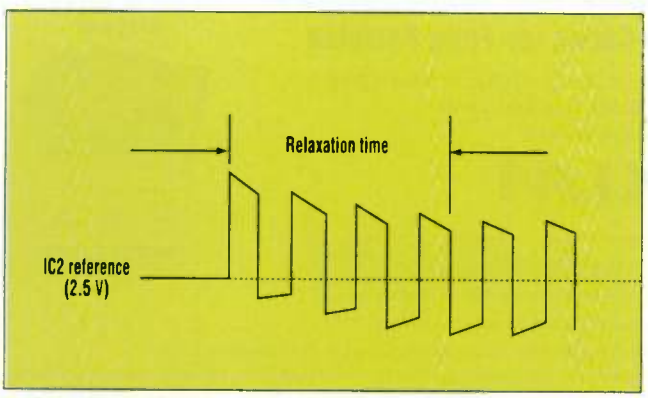
1. These two op amps and comparator form a tiny fiber-optic receiver capable of data rates up to 800 kbits/s.

reference voltage at 2.5 V. The R12/R13 divider, which sets the comparator's reference somewhat higher (2.6 V), provides a noise margin for the system and ensures that the comparator output remains low during a "no signal" condition.

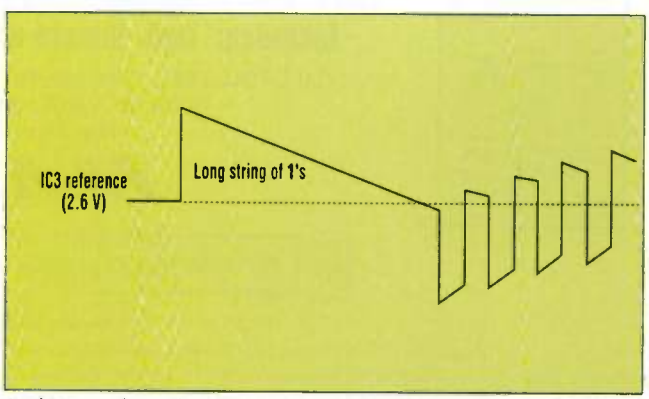
Capacitive coupling can't maintain a dc signal; instead, it allows dc portions of the signal to "relax" toward the reference level *(Fig. 2)*. This effect, particularly noticeable for signals that appear after a long quiet period, is directly affected by the R7/C3 time constant. R7/C3 should be as large as possible to minimize the relaxation effect, but R7 should remain approximately 10 kΩ (to minimize offset voltage by matching the inverting-input source resistance). The comparator can't switch when its input is below the reference level, so too much relaxation can cause a loss of data at the end of a long string of 1's or 0's *(Fig. 3)*.

Again, the IC3 reference should be slightly higher than the IC2 reference for a logic-low no-signal output (otherwise, set the IC3 reference lower). This ΔV_{REF} provides a system noise margin that you can adjust via the R12/R13 divider, but be aware of the trade-off. Setting ΔV_{REF} too low allows erroneous output transitions, and setting the value too high degrades timing of the received signal. Set ΔV_{REF} as low as possible without causing erroneous transitions, making allowance for the offset voltage in IC2 and IC3.

The system is designed for 5-V operation, but with a minor degradation in data rate, it can operate at 3.3 V or even 3 V. Lowering the supply voltage increases the photodiode's internal capacitance (inversely proportional to the applied bias voltage), which forms a low-pass pole with R2 that limits the photodiode's frequency response. To a lesser degree, the lower supply voltage also limits response by producing a smaller gain-bandwidth product in the amplifiers. The circuitry is designed to accommodate a change in supply voltage with only one adjustment: ΔV_{REF} changes with supply voltage, so you must adjust the R12/R13 divider as required to reestablish the desired noise margin.



2. Figure 1's coupling capacitor (C3) causes signal "relaxation" in the analog data waveform at IC2's output and the data thresholding comparator's nonninverting input.



3. This waveform (from Figure 1's IC2 output) demonstrates that signal relaxation can cause data loss (the comparator output goes low when the waveform crosses its reference level).

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MAX4016	2	1	+3.3 to +11	150	600	0.02/0.02	0.05 to 4.95	No	8-pin SO/µMAX	1.10
MAX4017[1]	2	2	+3.3 to +11	150	600	0.02/0.02	0.05 to 4.95	No	8-pin SO/µMAX	1.10
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38th Israel Conference on Aerospace Sciences, Feb. 25-26. Tel-Aviv & Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alice@aerodyne.technion.ac.il.

MARCH

Sixth Annual Embebbed Systems Conference East, Mar. 31-Apr. 2. Chicago's Navy Pier Festival Hall, Chicago, IL. Contact Miller Freeman Inc., 600 Harrison Street, San Francisco, California 94107; (415) 905-2354; fax (415) 905-2220; Internet: http://www.embedsyscon.com/.

APRIL

Southeastcon '98, Apr. 10-15. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

MAY

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE(FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

JUNE

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, MD. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, Maryland 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, Louisiana. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JULY

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 11-17. Sheraton Hotel, San Diego, California. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, California 92112; (619) 696-2780; fax (619) 699-5096.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, CA. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, California 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, CA. Contact Jim Schwank, Sandia National Laboratories, P.O. Box 5800, MS-1083, Albuquerque, NM 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST

AUTOTESTCON '98, Aug. 24-27. Salt Palace Convention Center, Salt Lake City, UT. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

OCTOBER

IEEE International Conference on Systems, Man, & Cybernetics, October 12-14. Hyatt Regency La Jolla, La Jolla, California. Contact M.A. Jafari, Dept. of Industrial Engineering, Rutgers University, Post Office Box 909, Piscataway, New Jersey 08855; (908) 445-3627; (908) 445-5467; e-mail: jafari@gandalf.rutgers.edu.

NOVEMBER

Photonics East & Electronic Imaging International Exhibition, November. 1-6. Boston, Massachusetts. Contact SPIE Exhibits Dept., Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Voice, Video & Data Communications Conference & Exhibition, November. 1-6. Boston, MA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhbits@spie.org.

IEEE Global Telecommunications Conference (Globecom '98), Nov. 9-13. Sydney, Australia. Contact Sam Reisenfeld, School of Electrical Engineering, University of Technology, Sydney, P.O. Box 123; Broadway, NSW 2007, Australia; +61 2-330-2435; e-mail: samr@trnasmit.ee.uts.edu.au.

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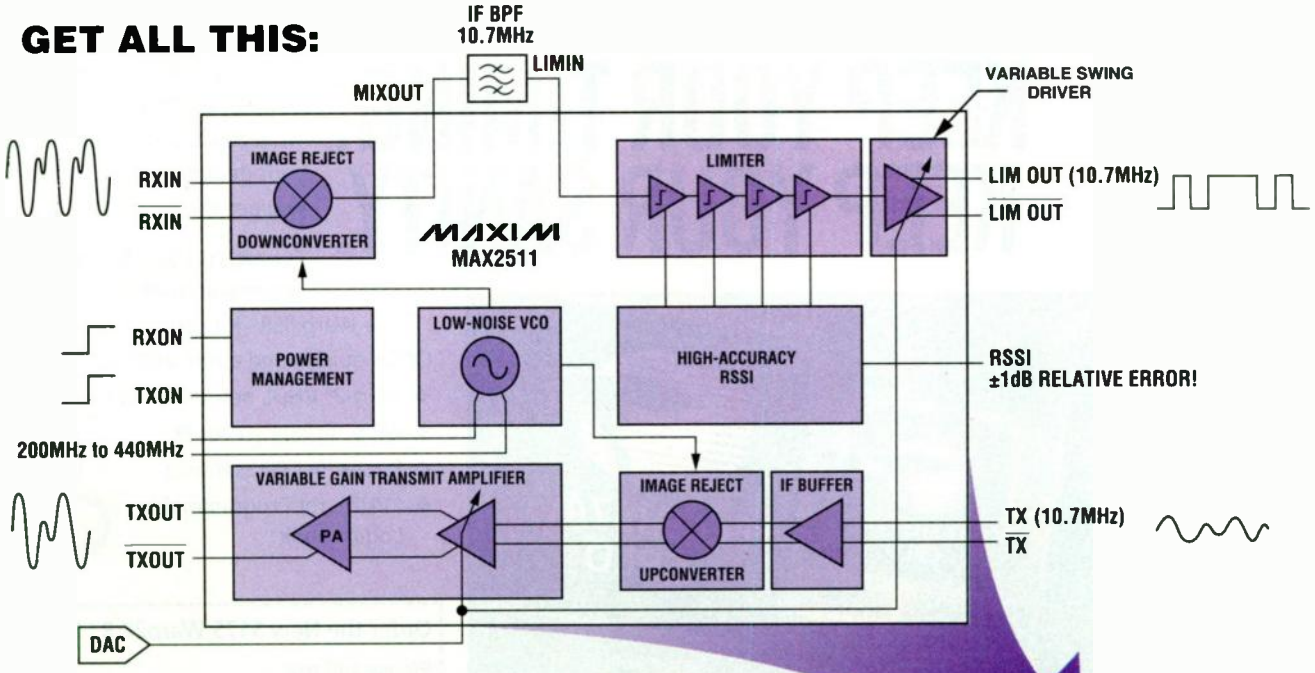

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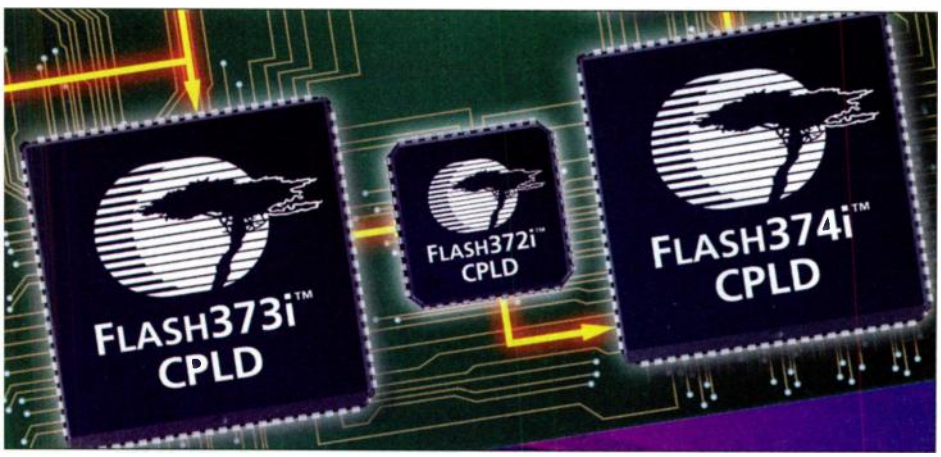

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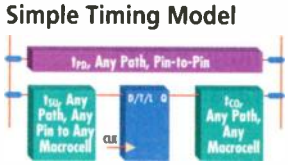

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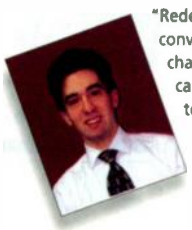

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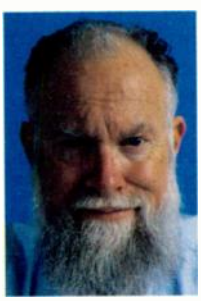
What's All This Scrooge Stuff, Anyhow?

More than 30 years ago, I began playing this different version of Solitaire. Where did I learn it? At Gardner Perry's house in Acton, Mass. Not just a quiet, thoughtful version, but a breakneck version. I'll write it down here. It's a unique kind of card game, because looking at any card is not cheating—it is permitted. Think about it.

First of all, I will mention that I have always refused to learn to play Bridge—and for a reason: First of all, the rules are quite artificial, and arbitrary, with many kinds of communication forbidden. Second of all: I know a number of guys who flunked out of M.I.T. because they could not resist the call, "We need a fourth! Who will join us to make a game of bridge? Hey, Joe, I don't care if you need to study, we *need* a Fourth!" Since a game of Bridge needs 4 players, then a person who knows how to play could be considered antisocial if he refused to join in. That's the main reason why I refused to learn to play. I should mention that the Game of SCROOGE can be played by any number of players, from 2 or 3 to 4, 5, 6, 7, or more. Seriously, I must admit, a game with 3 players is just *so-so* but 5 is much busier than 4, and 6 or 7 becomes mind-boggling....



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

The Game of SCROOGE

Written down by R. A. Pease, 1985, and updated in 1997.

First Description: The game of SCROOGE is a competitive form of double- or multiple-solitaire *(see "Conventional Solitaire Play," p. 138).*

Object Of The Game: To get rid of all the cards in your SCROOGE pile as fast as possible, while putting as many of your cards as you can out on the Aces in the center of the table.

Philosophy Of The Game: Within certain guidelines listed below, you play as fast as you can, to move cards (legally) out of your SCROOGE pile, and onto the Aces. Also, you play the cards in your HAND to help get cards onto the Aces and out of your SCROOGE pile. Anybody can look at any card at any time. Thus, there is no harm to have cards that are well worn, even ones that are too tattered or bent for any other card game!

Number Of Players: A game of 2 is occasionally boring. A game of 3 is boring, not often. A game with 4 players is very RARELY slow or boring. A game with 5 or 6 or more players is almost never boring, and usually frantic or insane. It may tend to turn into a riot. Generally, quite challenging.

Still, this is not bad as Bridge, where there is only one number (4) that is permitted to play.

Equipment Needed: At least 1 deck of cards for each player, with different CONTRASTING back-patterns or colors; pencil and paper for keeping score; and a big, well-lit table, preferably 40 inches in diameter. (A card-table such as 30-in. square is rather too small for 4 people.)

Types Of Skill Involved: Setting and changing priorities. Watching 15 or 20 things at once (literally). Manipulating variables. Avoiding getting seriously angry, even when sorely provoked. (A nontrivial statement.)

Skill And Practice Level: One of the best aspects of the game of SCROOGE is that kids, young people, and beginners can play. It is a good, challenging game, and not hopelessly discouraging for kids of all ages, and adults, too.

The SCROOGE PILE: This is a handicap pile. Each player places his SCROOGE PILE at his left, face up, overlapping so he can just see what each card is. (Everybody else can see them, too, and can see what each player's priority is—and how many cards are left.)

The normal SCROOGE PILE is 13 cards. Experts should play with more than 13 cards. Kids who are learning to play can take as low as 10. I know kids who started out at 10, worked their way up to 13, and are now playing at 15. I played at 13, 14, 15, and 16 for a while, but I am now working at 15. That's a fair handicap.

The general rule is, don't set a SCROOGE PILE so large that a kid or beginner can not ever win. Everybody should win a hand—and a game—on occasion. But if a person wins too often, he should get his SCROOGE PILE adjusted up....

Scoring: At the end of each HAND of play, after somebody has hollered "SCROOGE," the cards left in your SCROOGE PILE (that you could not get rid of) each count 2 points AGAINST you. Each of the cards played in the center (Aces, or on the Aces) counts one point FOR you.

At the end of each HAND, save your SCROOGE PILE, remember the number of cards in your SCROOGE PILE, and multiply by –2, and add that to the number of cards you played onto the center of the table. Hopefully, the result will be positive in most hands!! The scoring is listed here, so you can begin to see the PRIORITIES.

The SHUFFLE: Each player takes a standard deck of cards (52 cards, 4 suits, each with Ace and 2 up to KING). Shuffle them very well, at least 7 or 8 times, and pass them face-down to the person on your LEFT.* (*As soon as one person has reached a score of 75, the cards are passed instead to the RIGHT.) When you get your well-shuffled cards, CUT the deck by taking perhaps the top half of the deck, and moving it below the rest of the cards.

The LAYOUT: After you have CUT,

BOB PEASE

take the top 13** cards off the top of your new deck, one by one, and lay them down, one by one, face up, on the table, on the left side of the table in front of you. That is your SCROOGE PILE. (** 13—or as agreed upon.) Then lay the next 4 cards, side by side, in front of you. These are the BUILDING PILES. Hold all the other cards in your left hand and prepare to play. When every player has laid down their SCROOGE PILE and all 4 cards for the BUILDING PILES, play can begin. (If you want play to NOT start, do not put all your cards out.) Leave plenty of room below your 4 BUILDING PILES for building down, and for your DISCARD PILE. About 8 or 10 inches is good, from the 4 BUILDING cards to the edge of the table.

The PLAY: There are several things you can do. The PRIMARY objective is to get the cards off your SCROOGE PILE, and play them legally onto the 4 BUILDING PILES, or onto the Aces in the center *(see "Play On Aces").*

The NEXT priority is to play a lot of cards onto the center. To help you do this, you go through your HAND, 3 cards at a time. This may help BUILD your piles, or lead to combinations that can spring loose some of your SCROOGE PILE.

For example, let's say you have a 7 of Diamonds and a 5 of Hearts as 2 of your 4 BUILDING PILES, and a 3 of Diamonds on top of your SCROOGE PILE. What cards would you like to see? A black 4 would let you put the 4 on the 5, and the 3 on the 4. Similarly, a black 6 would let you put the 5 on the 6 on the 7—and this would have the further advantage of getting the number of your BUILDING PILES down to 3. See below:

Conventional Solitaire Play: On your 4 BUILDING PILES, the standard solitaire play is alternating colors and descending order. You can put any black 9 on any red 10, and then a red 8 on top of that, and then a black 7, and so on. Only those choices.

When you move a card to empty one BUILDING PILE, you can leave one of the 4 piles empty. Or you could fill it with one card from your SCROOGE PILE. If a second pile gets empty, you will usually fill it with a card from the SCROOGE PILE. You *could* take a card from your DISCARD PILE, if that causes a great advantage. This might occur if you were nearly stuck.

Play On Aces: After play has started, any time you have an Ace, you can put it in the center of the table. Any time an Ace is out there, any player can put a 2 of the SAME suit on the Ace, and this continues, putting the 3 on the 2, etc., and the Jack on the 10, the Queen on that, and the King on top. After the King has been placed on the Queen, no other play in that suit can occur, and the stack may be ignored, or set aside. Often there are 10 or more piles building in the center of the table. This can be very hectic, and hard to keep track of.

Play From Your HAND: Take the first 3 cards off the top of your HAND, turn them over, and lay them down face-up in front of you, to make a DISCARD PILE. You can play the top card, if you can, onto the Aces, or onto the 4 BUILDING PILES. If you move that top card, then of course you could play the card under it—the new top card on the DISCARD PILE. If you cannot move or play the top card, then set down the NEXT 3 cards from your HAND onto the DISCARD PILE, and try to play the next one on top.

Go all the way through the HAND. At the end of this HAND, put down the last 1, 2, or 3 cards on the DISCARD PILE. Then you can pick up the entire DISCARD PILE, turn it over intact to be all facedown, and start all over with this as your new HAND.

Usually you go through your HAND fairly quickly, and only slow down when there is some other interesting move to be made. (Strategy: If you can play *one card* from your hand, then the next time you go through your HAND, you will see different cards. If you *don't*, you *won't*.) If you played 3 cards, you would tend to see mostly the same cards again, which may be considered disadvantageous.

SHORTCUT: At any time, you can always lay all your cards down and get at the last card. Thus, you can always grab the last card off the bottom of your HAND. Thus, it is useful to KNOW what the last card is—the card on the BOTTOM of your hand so you can grab it and play it as soon as it useful. So as soon as you have laid out your SCROOGE PILE, you can check the card on the BOTTOM of your HAND and know what it is.

Be alert for amazing places to put it in play. It is NOT required to literally lay down your whole HAND to do this. You can just grab the last card. Then you can peek and see, what is the NEXT last card. (Reminder: At any time, you can peek at any card in your hand, to see what it is. Usually there is not much advantage to do this. But, if you lay down your 3 cards so you can see each of the three, you might find something amazing. Sometimes it may be advantageous to make a DUMB play on the top card of your DISCARD PILE, if there is a great advantage in getting at the card under it.)

Play Onto The BUILDING PILES: As soon as play has started, you can take a card off the top of your DISCARD PILE, and put it on a legal place ON TOP OF one of the 4 BUILDING piles. If you have 3 BUILDING PILES, you can ALSO take a card off your DISCARD PILE or off the SCROOGE pile, and put it UNDER one of the working piles.

For example, if you have a red 7, you can grab a black 8 off your SCROOGE PILE and slide it UNDER the red 7, because that is equivalent to laying down the black 8 on an empty slot in the BUILDING PILES, and moving the red 7 on top of it.

But you don't have to move that way; just shove it under the 7. This is neater if the red 7 has a lot of cards on top of it. BUT, you can only do this if there 3 or fewer piles. Likewise, if you are in 3 piles, you could grab that 8 of Clubs, and put it on a 7 of Clubs in the middle. It's a perfectly legal shortcut.

Similarly, you could take a card out of the middle of a run of cards in a BUILDING PILE, by moving part of the pile to an empty place, if there is a big advantage to get that middle card. For example, if you have 3 piles, and you want to grab the 8 of diamonds from between a black 7 and 9 in a BUILDING PILE, to spring loose the 9 of Diamonds on your SCROOGE PILE, and you have an 8 of hearts on your DISCARD, you can just swap it in. If you are stuck in 4

BOB PEASE

piles, you can't do that swap.

So, you can see that there are many advantages in staying in 3 piles. Sometimes you can be stuck in 4 piles for many minutes, and this can be a real DRAG. Sometimes, when you are in 3 piles, you decide to make some moves to get into 4 piles for a short time, in hopes of getting back into 3 shortly. If that doesn't work, you might be stuck in 4.

As you continue play, your priorities may change. Early on, building may be important to build up to a place where you can remove cards from your SCROOGE PILE. Later, there may be times when a specific combination can be built to help move things. If a long lost Ace shows up in the middle, you may build a lot of cards on THAT, to reduce clutter on your BUILDING PILES (and make a lot of points). Priorities usually vary 2 or 3 times per minute.

End Of The HAND: When one person empties his SCROOGE PILE down to zero, he can holler "SCROOGE!" That is supposed to end play. If another player has a card coming DOWN onto the table, that is OK, but if he is just picking a card UP to play it, and it is not yet coming DOWN, he should put it back.

House Rule: At our house, if a person has 3 BUILDING PILES, even after play has "stopped," he can move over a card from his SCROOGE PILE to fill in EMPTY slots to get the number of BUILDING PILES up to 4.

At this point, every player counts and saves and remembers the number of cards left in his SCROOGE PILE. Then all cards in your HAND and in your DISCARD PILE and in your BUILDING PILES are scooped together, and are not counted.

Note: The first player to empty his SCROOGE PILE is not REQUIRED to say that awful word; he can keep on playing if he sees any advantage.

One or two players usually merge all the Aces and the cards ON the Aces, ALL the cards in the center, and turn them over, and sort them by the backing, so each player will get his cards that he put into the center. Then each player counts those cards. His score for that hand is the number of Aces and cards on Aces, minus 2 points for each card left in the SCROOGE PILE. This total can be plus *or* minus. After each hand is played, each player's score is added up. Keep score on paper. When one player has gotten his total up to 75 points, that requires the shuffled cards to be passed the opposite way.

End Of Game: When one player has gotten to 150 points, that ends the game, and the player ahead at the end of the round is the winner.

ONE HAND? Yes, you can only use one hand to put out 1 card at a time, on the Aces. (The exception is, you can use more than one hand, to put out 2 or more Aces.)

BACK UP? Normally you can not put a card BACK ON your SCROOGE PILE, or in your HAND, but if you picked it up to put it in a legal place in the center, and somebody beats you to it, then you have to put it back where it was.

STUCK? What if no player can make any legal move? This happens rarely with 4 players, but occasionally with 3 (often with 2). If that occurs, the players agree to stop play, and all the SCROOGE PILES are counted, and subtracted, etc.

STOP PLAY? If there is something important to do—answer the phone, or pick up something spilled, etc., all play can be stopped by request. No harm. Play is often stopped to permit large, messy stacks to be straightened up, or removed from the center when they are filled up to King....

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SCROOGE!

All for now. / Comments invited!

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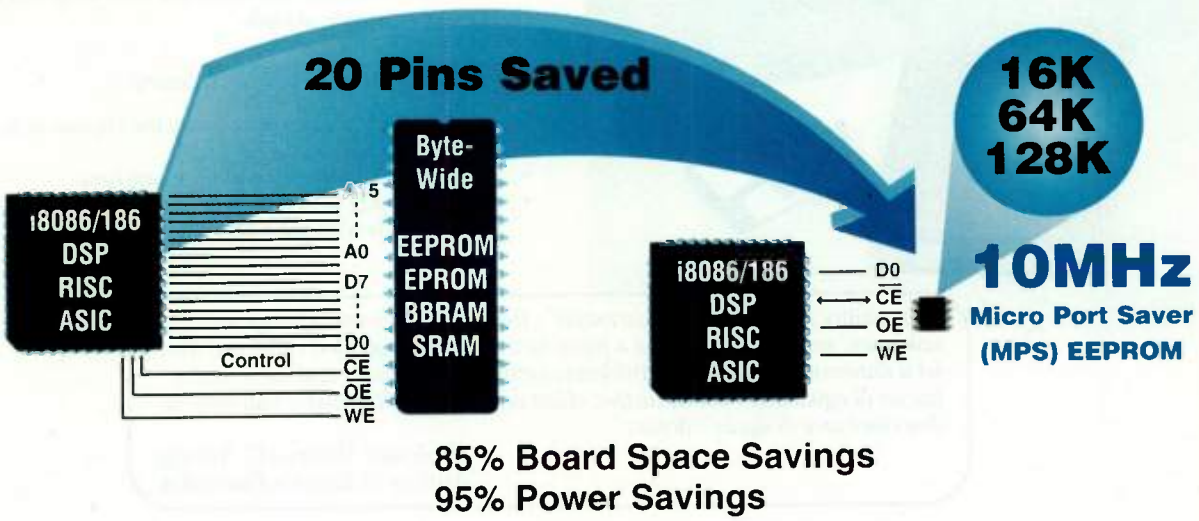

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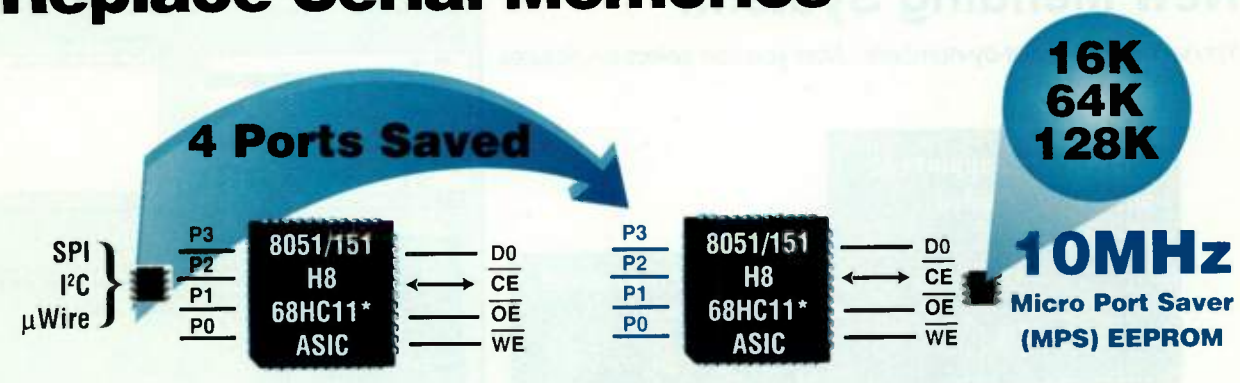

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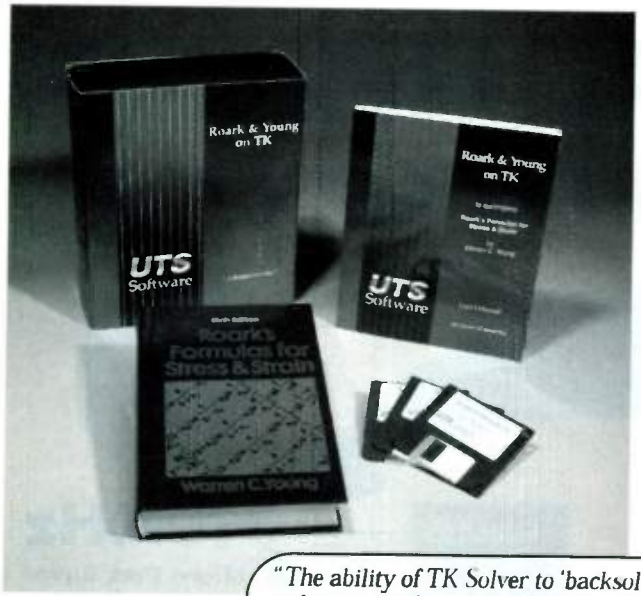

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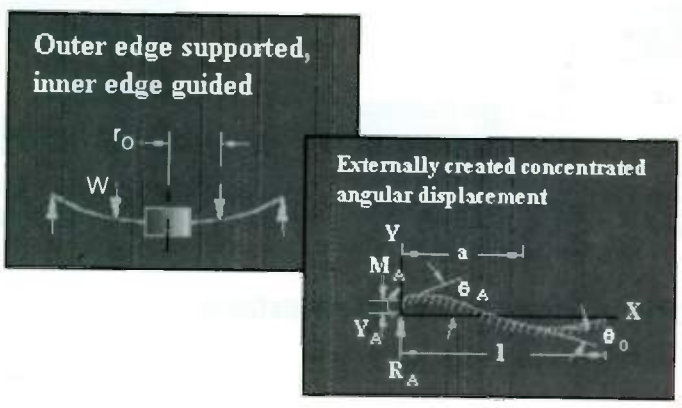

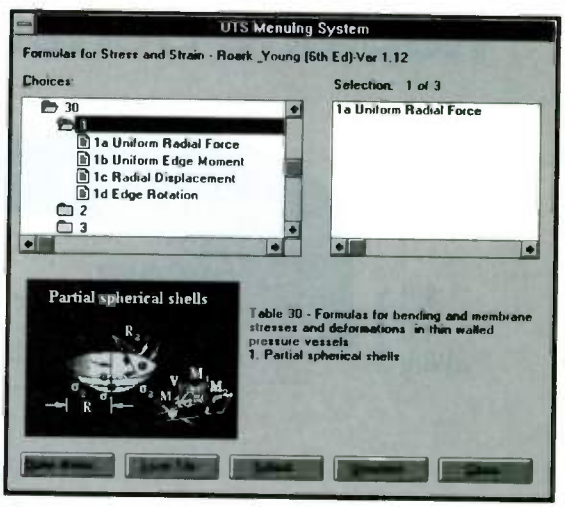

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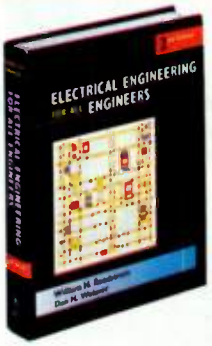

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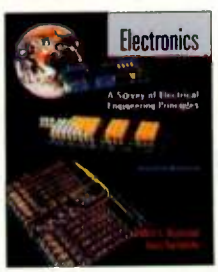

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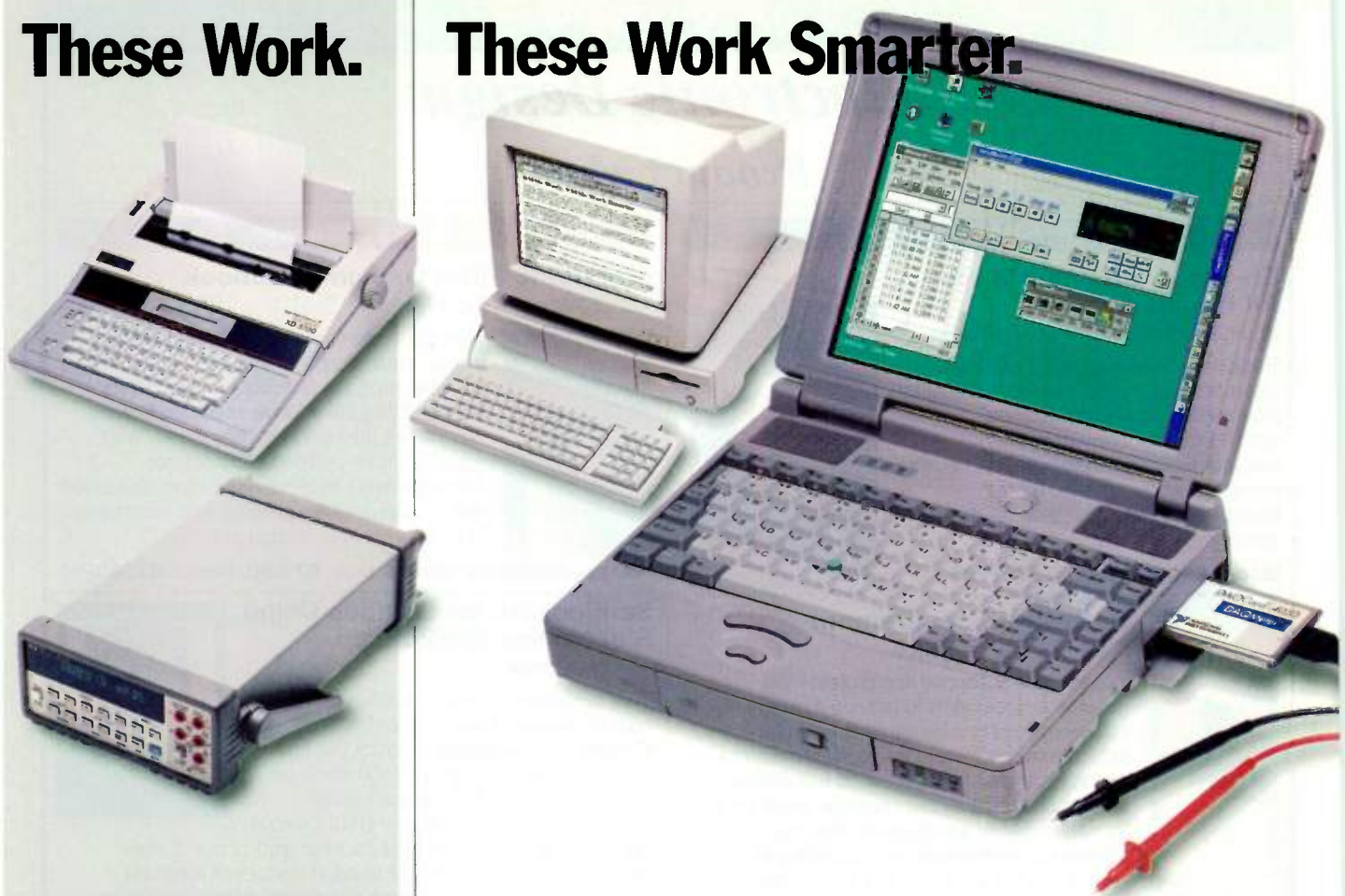

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Book Reviews:

A Collage of EE-Interest Books.

This time around we take a look at a variety of EE-interest books, both of an analog design as well as computer-related nature. This book listing doesn't follow the classical form of book review, which looks at recent titles in high detail. Instead, it is more of an overview of still-current or fairly recent works that have continuing interest.

Analog design books: *The Art and Science of Analog Circuit Design*, edited by Jim Williams; ISBN: 0-7506-9505-6, $49.95, 398 pages with index, is a book available from Butterworth-Heinemann, (800) 366-2665. This one, like its predecessor volume of a similar size, *Analog Circuit Design: Art, Science, and Personalities*, ($31.95 in paperback from the same publisher) is a collection of analog design perspective essays by various expert designers. In both of these books Williams has assembled some unusual writings, doing so in a style and format simply not found at all in conventional engineering handbooks with diverse author sources.

Jim Williams is well known for his many articles in *Electronic Design* and other electronic industry design publications, and has an analog career that includes experience at MIT, National Semiconductor, and Linear Technology Corporation, where he is currently a staff scientist. I got to know Jim while I was with Linear Technology a few years back, and he is always colorful in terms of personality as well as his writings. His writing style invariably reflects unusual insight into a wide array of analog designs. But, in defining and editing these books, he also has shown a quality of vision and selection of what makes good, analog-oriented reading from a multitude of individual authors. Since we all know that analog designers by nature tend to be mavericks, this last accomplishment by itself is no mean feat.

Some insight of what these books are about can be gleaned from the preface: "*...What we concluded went something like this: everyone would go off and write about anything that could remotely be construed as relevant to analog design. Additionally, no author would tell any other author what they were writing about. The hope was that the reader would see many different styles and approaches to analog design, along with some commonalities...*"

Although to some this might sound like a recipe for disaster, in the end, the results for both books speak for themselves. It works, and it's fun! In "*Art and Science*," 16 contributors offer 20 separate chapters on various analog-related topics, not all purely design-related—sections on marketing and careers also are included. A sampling of just some of the more interesting chapters includes the following:

Editor/author Williams contributes three chapters: "*The Importance of Fixing*," focusing on the educational and self-growth aspects of same; "*Tripping The Light Fantastic*," a fascinating treatise on Royer and other high-voltage display converters; and "*There's No Place Like Home*," on setting up your own home lab.

James Bryant has a chapter on "*Analog Breadboarding*," which discusses the physical and mechanical issues of proving your electronic design in hardware. Sprinkled with a multitude of analog design rule capsules, this section should be required reading for those accustomed to designing solely with simulators.

Steve Roach has an engaging chapter, "*Signal Conditioning in Oscilloscopes and the Spirit of Invention.*" This chapter explores scope front-end design, including compensated switched attenuators, and active buffer stages, useful up through 500 MHz.

Carl Battjes contributes a noteworthy chapter, "*Who Wakes the Bugler?*" which describes the design and use of "T-coils" in oscilloscope amplifiers, including a historical sidebar on distributed amplifier technology.

Finally, a perfect example of the book's freeform style is the chapter "*Analog Circuit Design*" by John Willison, written up simply as a list of 57 important analog rules. Take # 8 as a for-instance: "*The impedance looking into the emitter of a transistor at room temperature is 26 (divided by the emitter current in mA).*" After listing 37 such useful gems, Willison invites readers to find the other 20!

TIP: All-in-all, this book and its predecessor are recommended to anyone seriously interested in analog design. They are not handbooks, nor are they design manuals per se. Nevertheless, they do give the reader a broad perspective on various design practices, and some useful insights of keen analog minds. The two books do accomplish the editor's goals, and taken together, should serve you well for some time.

WALT JUNG

Computer-related books: It seems that the quality of computer books can (sometimes) take on the characteristics of an epiphany, or (more often) a dirge. Quite simply, there are just way too many from which to choose, with many in the mediocre category. However, with careful selection, some pearls can be harvested from this sea of information sources. My recommendation: spend some time browsing the computer section shelves of your bookstore, and compare multiple samples of a given genre. That found me two of the books listed here.

The Complete Idiot's Guide to the Internet, Third Edition, by Peter Kent; ISBN: 0-7897-0862-0, $24.99, 394 pages with index, is available from QUE, a division of Macmillan Computer Publishing, (800) 428-5331.This book provides a breezy and comfortable, yet broad-ranging view of what the Internet is all about. In the revised edition there is expanded coverage of the World Wide Web and limited information on on-line services, such as AOL, CompuServe, and MSN.

In my opinion, the real strength of this book lies in the variety of Internet topics that it does cover in some degree of detail, but yet without becoming overly technical. These headings include e-mail, web browsers, web pages, newsgroups, mailing lists,

WALT JUNG

chat, telnet, search engines, FAQ and other info sources, and finally, some basics of selecting an ISP. The book also comes with a CD, which includes Internet access software good for up to 60 days. If you are looking for a single book which gets you going on the 'Net with minimum hassle, this could well be a candidate.

Internet Starter Kit for Windows 95, by Adam C. Engst, Corwin S. Low, and Stanley K. Orchard; ISBN: 1-56830-260-6, $35.00, 514 pages with index, is available from Hayden Books, a division of Macmillan Computer Publishing, (800) 428-5331. This book could ostensibly be seen to duplicate the "*Idiot's Guide*" above, yet it really doesn't, for good reasons. While overlap is inevitable, "*Starter Kit*" is purely for Windows 95 hardware, and emphasizes this with a CD full of software expressly for Windows 95. It also is more detailed and on a higher technical level than "*Idiot's Guide*," and thus will serve to answer many questions not addressed therein.

While the topical coverage of this book generally parallels "*Idiot's Guide*," the main differences lie in details and degrees. For example, "*Starter Kit*" covers choosing an ISP in quite some detail, covering both business and technical issues. Details of your network connection also are covered in some detail, allied to the Windows 95 dial-up networking function. The CD supplied with the book offers basic Internet software such as browser, e-mail, FTP, newsreader, and a webpage editor.

Given the rapidly changing nature of the Internet, some aspects of these two books will inevitably be obsolete very quickly. Nevertheless, the key fundamental points are well covered, so look for future editions of these two books to track 'Net updates.

Using Windows 95 Platinum Edition, by Ron Person, et al; ISBN: 0-7897-0797-7, $60.00, 1360 pages with index, is available from QUE, a division of Macmillan Computer Publishing, (800) 428-5331.

This one is the sort of book that you buy strictly for reference uses, as opposed to the fun aspects of using a book like "*Idiot's Guide.*" And, since Windows 95 doesn't come with documentation, there is an inherent (and pressing) need for just this type of book. In fact, everyone who uses Windows 95 can potentially use a book such as this. Putting "*Using Windows 95*" to work a few times will likely make its relatively high price (for a paperback) seem worthwhile.

The book includes 41 chapters and 5 appendices, plus two CDs of software. Some of the major subheadings and chapters of the book could actually be smaller books in and of themselves. There are, for example, 13 chapters and 370-odd pages covered just in the "*Networking*" and "*Internet/On-line Services*" series of chapters. Other major headings are configuring and optimizing (Windows 95), customizing, working with applications, sharing data, disk drives and backups, and multimedia.

Since first buying this book at the time of a Windows 95 upgrade, I have used it on several occasions. I actually found it indispensable as a resource, leading me through the vagaries of dial-up networking a few times, and later on in adding CompuServe mail access to Microsoft Exchange.

Looking at the bigger picture, it seems truly incomprehensible to me that an operating system as varied and powerful as Windows 95 lacks documentation, but yet this is so. This absurdity serves no one at all, and in the final analysis, goes right back to the theme of support. With that comes the questions of who does it, who helps, who pays for it, and so on, ad infinitum. Stay tuned for more on this timeless topic in a not-to-distant future column.

TIP: Books like "*Using Windows 95*" obviously fulfill a real user need. I can recommend this book, the only caveat being that Windows 98 may soon be with us. Assuming the current '95 version is updated along the same lines into "*Using Windows 98.*" that should also be a very useful work.

So that is it for this set of book reviews. Some upcoming reviews will focus on more analog topics. My thanks to all of those who have taken time to write in. Keep those cards and letters coming!

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A longtime contributor to Electronic Design, he can be reached via e-mail at Walter.Jung@Analog.com.

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READER SERVICE 95

ANSI-Compliant ADSL Chip Set Has Enhanced Spectral Ability

The MTK 20122 chip set for ADSL (Asynchronous Digital Subscriber Line) offers higher performance and an improved spectral performance compared to its predecessor MTK 20120. The new chip set, which features 0.35-µm geometries in the digital section and 0.5 µm in the mixed analog/digital section, consists of a dual chip data pump complemented by a special ATM framer, thus fulfilling the ANSI specifications for ADSL. This allows direct connection to other system elements via a Utopia ATM interface. MTK 20122 makes it possible to implement digital subscriber lines with adaptive data rates, where the data rate can be adapted in increments of 32 kbits/s over the entire transmission range. This data-rate adaption is performed in the physical as well as in the transport layer, which allows for more effective usage of the data stream at the system level. While the downstream performance may be up to 7.5 Mbits/s, upstream performance is limited to a maximum of 640 kbits/s with cable lengths of more than 5 km (using AWG-26 cables). AV

Alcatel-Mietec, *Raketstraat 62, 1130 Brussels, Belgium; phone: +32-2/728 18 11; fax:+32-2/726 42 15.*
CIRCLE 595

Single-Chip "Voice Engine" Meets Voice-Application Needs

Voice Engine is the nickname given to a new single-chip solution for voice recognition, voice storage, and sound effects. It combines a 1-Mbit embedded DRAM, a DSP, 8 kbits of SRAM, 256 kbits of ROM, parallel and serial interfaces, an audio interface, and random logic. The device, otherwise known as SDB 7000, requires a 3-V supply and is packaged in a 44 pin P-MQFP. It comes as the result of efforts to utilize the 16-Mbit DRAM 0.35-µm manufacturing process for logic functionality. Following embedded DRAM solutions in 1- and 4-Mbit DRAM technology, this is the third embedded DRAM generation with trench cells. The fourth generation of embedded DRAM will follow in 1998 using a 0.25-µm process. The process is based on the trench-capacitor DRAM process with up to four metal layers, which is used to produce 256-Mbit DRAMs. These memory blocks can be combined in 256-kbit blocks to sizes of up to 20 Mbits. The internal interface bus width can be up to 512 bits with a configurable pipeline depth of up to three stages allowing data transfer rates of more than 5 Gbit/s. When produced in an 0.35-µm technology, a 2-Mbit memory module consumes a chip area of 8.8 mm^2, including a 128 bit interface and the test controller. AV

Siemens Semiconductors, *P. O. Box 80 17 09; 81617 Munich, Germany; phone: +49 89 4144-0; fax: +49 89 4144-8482.* **CIRCLE 596**

Pentium-Based Computer First In CompactPCI Product Family

The first board to arrive from a new series of CompactPCI (CPCI) products developed by PEP Modular Computers—the CP-310—is a single-board computer based on a Pentium processor. In contrast to already existing CPCI solutions, this board integrates a new generation of Pentium support chips as well as mass storage interfaces for Flash disk drives. The board supports all Pentium CPUs with a PGA socket; if a K5 processor from Advanced Micro Devices is used, the temperature range can be extended. For lower power consumption, the 32- and 64-Mbyte DRAMs are all implemented in 3.3-V technology. Industrial connectors at the front panel allow for cable adaptions. Starting with the basic version, the board is equipped with 256 kbytes of level 2 cache memory. AV

PEP Modular Computers GmbH, *Apfeltranger Str. 16, 87600 Kaufbeuren,Germany, phone: +49-8341/803-0; fax: +49-8341/803-499.* **CIRCLE 597**

Preamplifier For MR Heads Claimed As First At 300 Mbits/s

According to its manufacturer ,the TDA5357 is the first 10-channel preamplifier for single-stripe magnetoresistive (MR) read/inductive write heads to perform at 300 Mbits/s. The new device offers a noise rejection of 65 dB at 100 MHz for both common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR). Thermal asperity detection and recovery (FAST mode) functionality equips the preamp to detect and correct potentially damaging particles on the disk. The TDA5357 incorporates a serial interface for adaption and monitoring as well as to reduce pins and lines formerly used. As filtering and dc blocking capacitors are integrated, the new IC only requires a single external resistor.

The TDA5357's programmable features include a programmable mode (read/write, standby, sleep), programmable head selection, programmable MR bias and write currents, programmable gain, programmable high-frequency zero/pole gain boost and gain attenuator, programmable write driver compensation capacitance, programmable write current inhibit, and programmable servo write head selection. The TDA5357 incorporates read and write amplifiers, digital-to-analog converters, as well as reference and control circuits that operate on dual supply voltages of +5.0 V and –4.7 V. In quantities of 1000-unit lots, it's priced at $8.50 each (U.S.). AV

Philips Semiconductors, *P. O. Box 218, 5600 MD, Eindhoven, The Netherlands; phone: +31 40 272 20 91, fax: +31 40 272 48 25.* **CIRCLE 598**

Edited by Roger Engelke

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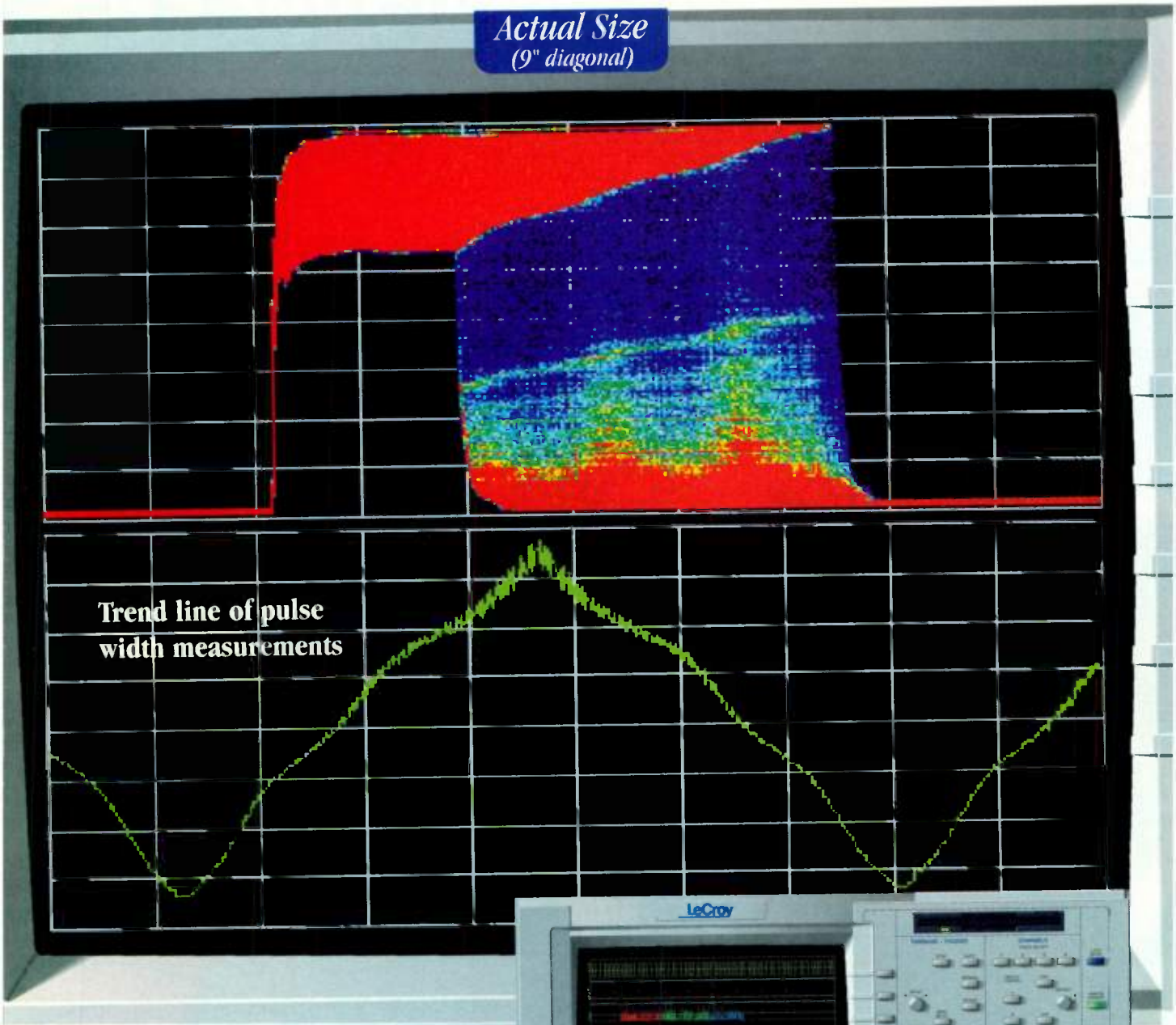

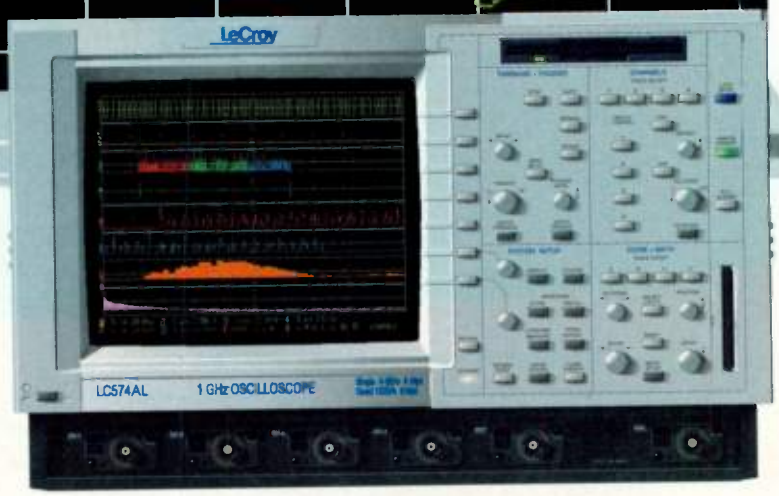

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Programmable Crosspoint Switches Deliver Up To 160 I/O Lines

Four generic digital crosspoint switches featuring 64, 80, 120, and 160 programmable I/O lines comprise the first four members of the ispGDX series of crosspoint switches. The devices are optimized for digital-signal-interface and routing applications, and consist of an array of special-purpose programmable I/O cells that surround an EECMOS-based global routing pool that determines the routing from I/O cell to I/O cell.

Input-to-output delays are less than 5 ns, clock-to-output delays are less than 5 ns, and the crosspoint has a maximum operating frequency of 111 MHz. The chips will be available in TQFP, PQFP, and PLCC packages, and all include an IEEE 1149.1-compliant boundary-scan test port and PCI-compatible outputs. Signals from an I/O pin enter the global routing pool and can be routed to any of the other I/O pins. The EECMOS configuration elements have a 10,000-cycle program/erase endurance and can retain data for a minimum of 20 years.

Each output has individually programmable I/O three-state control, an output latch clock, programmable polarity, a programmable open-drain option, and two multiplex select inputs that control a fast 4:1 multiplexer, which allows the dynamic selection of up to four signal sources for a given output. Inputs or outputs can be combinatorial, latched, or registered. Through in-system programming the pins of the ispGDX devices can be driven to High or Low levels to emulate traditional device outputs.

The crosspoint chips are supported by the company's ispGDX Development System, Version 1.0 that can run on a Windows 3.x, Windows 95, and Windows NT system, and includes a language-based design tool, a GUI-based design manager, on-line help, and interfaces to third-party timing simulators. The design language syntax is used to describe pin-to-pin connections, I/O functions, and user-specified pin assignments.

The ispGDX 160 will initially be housed in a 208-lead PQFP and sells for $27 apiece in lots of 1000 units. A slightly slower 7-ns version sells for $18 apiece in similar quantities. The 64, 80 and 120-I/O devices will be housed in 84-lead PLCC, 100-lead TQFP, and 176-lead TQFP packages, respectively, and will sell for proportionally less.

Lattice Semiconductor Corp.,
5555 Northeast Moore Court, Hillsboro, OR 97124-6421; Steve Stark, (503) 681-0118; or on the web at http://www.latticesemi.com.
CIRCLE 493
DAVE BURSKY

Reduced-Cost FLEX Field-Programmable Gate Arrays Provide 10 to 24 Kgates

With chip areas comparable to those of similar capacity gate arrays, the FLEX 6000 family of SRAM-based FPGAs will deliver 10,000 to 24,000 gates and costs similar to those of comparable-density gate arrays. To do that, Altera will move the current 0.5-µm triple-metal design rules to a 0.35-µm design-rule suite, which will reduce the chip area and also improve circuit performance. Size reduction also is made possible thanks to the company's OptiFLEX architecture, which combines advanced bond-pad technology for high density I/Os, an interleaved logic array block architecture, and an improved I/O structure for better logic efficiency.

Every feature in the OptiFLEX architecture focuses on maximizing the chip efficiency and improving performance. The logic-array block interleaving, for example, allows an LAB to communicate directly with an adjacent LAB through a local interconnect, thus optimizing the global row and column resource utilization. The FastFLEX I/O structures provide a direct path from the logic elements in the LABs to the I/O pins for fast clock-to-output timing, and a tight bond-pad pitch of just 3.2 mils minimizes size of the pad ring. As a result, a 16-kgate FLEX 6000 chip with 240 pads will be only 6% larger than a gate array die with the same pin count.

The improved efficiency also comes with a performance benefit, not a performance loss. For example, a 16-bit loadable counter can run at 135 MHz in a FLEX 6000—more than twice as fast as most other FPGAs. Family members also will include the company's patented MultiVolt feature that allows I/O lines to support preceding-, current-, and future-generation interface-voltage levels.

The EPF6010, a 10-kgate FLEX 6000 chip, will sell for just $6.00 each in volume by mid 1998 (when housed in a 144-lead PQFP). The EPF6016 with 16 kgates and the EPF6024A with 24 kgates are available this quarter, while the rest of the FLEX 6000 family members will be available in the first half of 1998. By mid-1998, the price for the 5-V EPF6016 will be about $7.50 each in lots of 50,000 units, while the 3.3-V version will sell for about $7.00 in similar quantities. The EPF6024A 3.3-V chip will sell for about $10.00 apiece, also in lots of 50,000 units.

Altera Corp.
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http://www.altera.com
CIRCLE 494
DAVE BURSKY

FPGA Reductions To Drop Some Prices To Less Than $3.00

Smaller feature sizes and an improved layout will bring the chip size of the XC5200XL FPGA family into parity with gate arrays, enabling the smaller devices in the family to be sold for less than $3 per chip. The cost-reduced versions of the family will be manufactured with 0.35-µm design rules, are designed for 3.3-V operation, and will be sampled in the late fourth quarter. The smaller features also will allow the XC5200XL family to offer a 30% performance increase while reducing prices overall by 25 to 70%, depending on the device.

Thanks to the lower cost of these arrays, they will be able to compete with gate-array-based designs. That's be-
(continued on page 152)

(continued from page 151)
cause there are no recurring engineering charges and no prefabricated inventory that must be scrapped if the design changes. In large quantities, the 256 logic cell XC5202XL will sell for just $2.95 each. The largest array, the XC5215 XL (which packs 1936 logic cells), will sell for just $9.90 each. Prices are estimated for orders placed in mid-1998. DB

***Xilinx Inc.**, 2100 Logic Dr., San Jose, CA 95124-3400; Kapil Shankar, (408) 559-7778; http://www.xilinx.com.*
CIRCLE 495

Serial EEPROMs Store FPGA Configuration Data

A family of 3.3- or 5-V in-system programmable serial EEPROMs provide designers with simple storage devices to complement SRAM-based FPGAs, which must load in their configuration data from external storage. Unlike the simple serial EEPROMs that operate at data rates of a few hundred kilohertz, the AT17Lxxx family will be able to clock at rates of up to 10 MHz. As a result, the logic configuration information can be loaded into the FPGA very quickly.

Available in densities of 65, 128, and 256 kbits, and in either commercial or industrial temperature ranges, the AT17LVxxx EEPROMs draw just 50 µA during standby and only 5 mA when operating at 10 MHz. Versions of the memories are available for most FPGA families—the AT6000 from Atmel; the Xilinx XC3000, 4000, or 5200; the Altera EPF8000; and the Lucent ORC2Cxx series. Multiple memories can be cascaded to support the larger FPGAs. Furthermore, if configuration requirements change, the EEPROMs can be reprogrammed in the system as many as 10,000 times using a standard two-wire programming protocol. Or they can be programmed prior to system insertion using standard programmers from Data I/O, BP Microsystems, Logical Devices, Stag, and others. Data retention is guaranteed for 100 years.

In lots of 1000s, the AT17LV256 sells for $17.28 each. It is available immediately. The AT17LV65 and LV128 are also available in sample quantities. *DB*

***Atmel Corp.**, 2325 Orchard Pkwy., San Jose, CA 95131; Joel Rosenberg, (408) 441-0311; or on the web at http://www.atmel.com.* **CIRCLE 496**

Design Service Company Supports PLDs And ASICs

The increased usage of programmable logic and ASICs to solve system design issues has opened the door for Wyle Design Services to set up design support. As a result, it now can play more than just a components distribution role in the customer design/manufacturing cycle.

The organization has been set up to provide technical support for customers that use programmable devices from Altera Corp., and to execute ASIC designs with LSI Logic. The expertise put in place provides design and consulting resources—from product synthesis through turnkey design solutions—to companies that desire additional support to meet the ever-shortening time-to-market windows.

Wyle currently has ASIC design centers in Los Angeles, Santa Clara, Baltimore, Boston, Chicago, and Dallas. Two more cities—Tampa and Dallas—will get design centers later this year. Staffing those centers will be over 75 supplier-certified application engineers and designers. Contact the nearest design center to determine fees and resources available to meet specific project needs. DB

***Wyle Design Services Div. of Wyle Electronics**, 15470 Barrance Pkwy., Irvine, CA 92618-2215; Rick Timmins, (714) 753-9953, or on the web at http://www.wyle.com.* **CIRCLE 497**

Logic Synthesis Tool Targets Altera Flex 6000

Fully supporting the Altera FLEX 6000 FPGA family, the Synplify logic synthesis tool can provide a design solution that, according to Synplicity, benchmarks 10 to 100 times faster than competitive synthesis tools. Furthermore, the company expects the tools will produce designs with better performance and more efficient logic utilization than other synthesis tools.

The Synplify tool incorporates a direct synthesis technology approach. This enables designs to be compiled directly to the base cells and architectural features of the target programmable devices, improving both performance and utilization. The Synplify synthesis tool accepts standard Verilog and VHDL circuit descriptions and produces the optimized implementations for the logic devices.

A finite-state-machine compiler allows the tool to provide fully-automatic recognition and re-encoding of finite state machines. The compiler also performs reachability analysis and eliminates unreachable states. The Synplify 3.0 node-locked Windows platform version sells for $12,000, and floating licenses for Unix or Windows are $24,000. Existing Synplify users with maintenance contracts get the FLEX 6000 support at no additional cost. DB

***Synplicity Inc.**, 624 Evelyn Ave., Sunnyvale, CA 94086; Andy Haines, (408) 617-6000; http://www.synplicity.com.*
CIRCLE 498

FPGA Tool Suite Targets HDL-Based Designs

Version 3.1.1 of the Designer Series of FPGA development tools will include an integrated high-level design tool suite and web-based design tools. Since about 25% of all FPGA designs are HDL-based, the revamped tools help meet the needs of the designers currently using HDL design capture, and should provide a smooth and low-cost transition to designers who are planning to move to HDL-based design approaches.

The first revamped part of the package will be the Designer 3.1 tool, which incorporates all of the latest devices, speed grades, and package options released by the company. The software also will offer an easier to use installation and startup path thanks to an improved database management package. Design support for the ACT1020RH RadHard FPGAs, the 32100DX, and other family members includes features that make it possible to use the -F, -2, and -3 speed grades.

The enhanced tools yield better circuit performance—about 15% improvement in circuit performance can be achieved thanks to more efficient synthesis, placement, and routing. Also included in the suite are the ACTgen macrobuilder and PinEdit, a signal placement utility. The software runs on either PC or Unix platforms and will sell for about 60% less than the price of the previous version. DB

***Actel Corp.**, 965 E. Arques Ave., Sunnyvale, CA 94086; Michael Saniei, (408) 739-1010, or on the Web at http://www.actel.com.* **CIRCLE 499**

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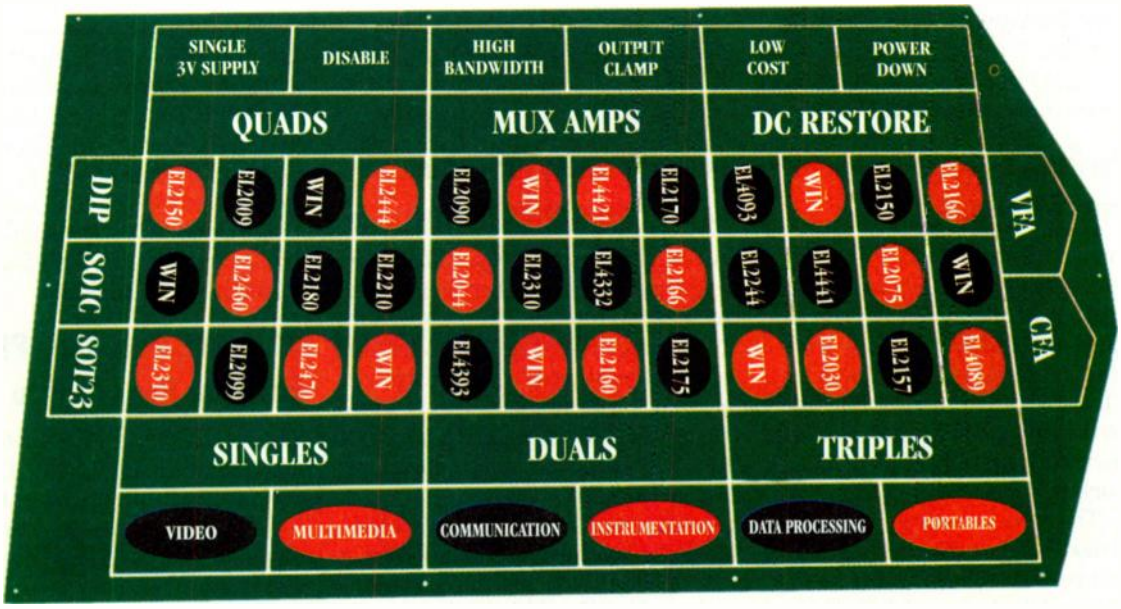

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READER SERVICE 104

Dynamic Signal Analyzer Has 50-kHz Analysis Bandwidth

The DSPT SigLab 50-21 is a modular dynamic signal analyzer with two input and one output channels. It offers a 50-kHz analysis bandwidth, greater than 95-dB spurious free dynamic range, and more than 90-dB alias protection at all analysis bandwidths. For higher channel counts, users can connect up to four instruments. Users setup and control measurements with a host PC using point-and-click GUIs coded in the MATLAB technical computing environment from The MathWorks. A number of ready-to-run instrument applications come with the hardware, including function generator with arbitrary waveforms, oscilloscope, spectrum analyzer (FFT), broadband network analyzer, swept-sine network analyzer, and system identification. The system comes in a notebook computer-size enclosure. The SigLab 50-21 costs under $8000. JN

***DSP Technology Inc.**, 48500 Kato Road, Fremont, CA 94538-7385; (510) 657-7555; (510) 657-7576; Internet: http://www.dspt.com.* **CIRCLE 500**

Tool Verifies, Debugs Test Patterns Without ATE

An automated test-productivity tool offers engineers a way to verify and debug IC test patterns and timing on engineering workstations rather than costly automated test equipment (ATE). Digital VirtualTester is a result of technology based on the company's Dantes Test development Automation System and a close working relationship with ATE vendors. The product incorporates a behavioral model of the target ATE that includes representations of tester memory, timing architecture, and digital pins. Test patterns can be generated by the company's TestDirect, TSSI's TDS, or customer-developed test pattern translation tools. The process also can be used on mixed-signal devices if test patterns for their digital pins and a standalone Verilog model of their digital functions are available. Prices for the tool start at $50,000. JN

***Integrated Measurement Systems Inc.**, 9525 S.W. Gemini Dr., Beaverton, OR 97008; (800) 879-7117 or (503) 626-7117; fax (503) 644-6969; Internet: http://www.virtualtest.com.*
CIRCLE 501

Tester Cycles 640 Flash Memories At Once

A flash memory cycling test system, the MS1201, can handle up to 640 devices simultaneously within its temperature chamber. The tester supports memories of up to 2 Gbits, with X4, X8, X16, and X32 organizations. Users can cycle and test the devices with traditional methods, the devices' embedded algorithm, or the internal test modes.

A distributed architecture allows simultaneous cycling and test of different flash devices in groups of 64. Other features include bit-map viewing and analysis of a device's physical features by column, row, block, address, and pattern. The unit is ideal for endurance characterization, measuring time and margin degradation, and stress testing, as well as infant mortality screening. Call the company for price and availability information. JN

***MOSAID Systems Inc.**, 3375 Scott Boulevard, No. 206, Santa Clara, CA 95054; (408) 727-7199; fax (408) 727-0479.*
CIRCLE 502

Software Analyzer Option Makes Integration Easier

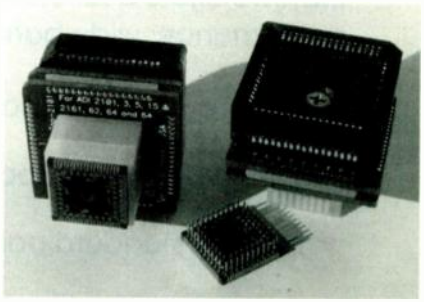
The SWAT Software Analysis Tool shows design engineers whether their code is executing as intended. Configured for code coverage, SWAT helps automate the task of gathering code coverage information. No instrumentation—that is, added code for "hooks"—is needed so the code doesn't have to be recompiled, linked, and downloaded again.

Configured for performance analysis, SWAT displays function execution times in the application. Engineers can use the results to identify which portions of code need better performance. Because SWAT is used during development, the code delivered to the system integration stage will have a higher likelihood of meeting expectations. SWAT can be ordered as a option for PowerPack emulators for 386, 486, and Pentium processors. Prices for the software analysis tool start at $8995. JN

***Microtek International**, 3300 N.W. 211th Ter., Hillsboro, OR 97124-7136; (800) 886-7333; (503) 645-7333; e-mail: info@micrtotekintl.com; Internet address: http://www.microtekintl.com.*
CIRCLE 503

Emulator Adapters Handle Digital Signal Processors

A line of emulator adapters provide interfaces between a PGA or a PLCC plug on the emulator and a target board with pads for a QFP package. The adapters are transparent to the emulator and are wired for Analog Devices' 21xx series digital signal processors and all devices



that are pin-compatible with them. The base of the adapter has a male connector and is soldered to the pads in place of the package. A second part, the emulator attachment with a 500-mil-high female connector, attaches to the emulator plug. The 69PG/80QFS26-SD-2101 accepts a 69-pin PGA emulator plug. Both cost $293 and are available from stock. Additional bases (80QFS26-SD) cost $122. JN

***EDI Corp.**, 2611 Highland Dr., Las Vegas, NV 89109; (702) 735-4997; (702) 735-8339.* **CIRCLE 504**

PC-Based Real-Time PIC16/17 Emulator Runs At 3 to 5 V

The RICE17A, a PC-based in-circuit emulator for PIC16Cxx and PIC17Cxx 8-bit microcontrollers, operates in the 3- to 5-V range, provides instant updates on all output ports, and comes with a self-diagnostic tester board. Standard features include a 32k program memory (expandable to 64k for the PIC17C4x), an 8k real-time trace memory, a 12-clip external probe, a DOS debugger, Windows 95 integrated debugging environment software, MPASM assembler, power adapter, and communication cables. The RICE17A emulator base costs $550. Emulator-specific probes range from $225 to $325. Both are available for immediate delivery. JN

***Advanced Transdata Corp.**, 14330 Midway Rd., Suite 128, Dallas, TX 75244; (214) 980-2960; fax (214) 980-2937; e-mail: atc@ix.netcom.com.*
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READER SERVICE 136

DIGITAL ICs

Serial 32-Kbit EEPROM Clocks At 5 Mbits/s

The X25330 high-speed 32-kbit EEPROM, which features a 5-Mbit/s serial peripheral interface (SPI), can transfer data 67% faster than other 32-kbit SPI memories. Two memory protection modes reduce the chip count in system designs by eliminating the need for an extra EPROM or ROM for sensitive read-only data. By transferring data faster, system operation can be greatly improved, since the low-speed access often is the performance-limiting factor in many systems.

This latest device fills out the company's serial EEPROM family, which ranges in density from 4 to 64 kbits, and offers endurance levels of 100,000 cycles. The protection modes include a Block Lock mode and an in-circuit programmable ROM mode. With the Block Lock mode, certain memory segments can be write-locked to protect the data from inadvertent writes that could corrupt sensitive information (e.g., billing information or serial numbers). The in-circuit programmable ROM mode allows designers to permanently lock certain portions of data as read-only during the manufacturing process. This is an important option for applications that must store critical system information such as calibration data.

Targeted at portable applications, the memory has a standby current of just 1 µA (maximum) and operates at voltages ranging from 5- down to 2.5-V. The memory comes in either a 14-lead TSSOP or 8-lead SOIC package and is available in production quantities. The same price applies for the serial EEPROM in either package—$1.46 each in 10,000-unit quantities. DB

Xicor Inc., 1511 Buckeye Dr., Milpitas, CA 95035; Bob Anderson, (408) 432-8888; http://www.xicor.com. **CIRCLE 506**

Link-Layer Controller Moves MPEG Over 1394

Intended for use in set-top boxes, digital televisions, and digital audio/video recording equipment, a link-layer controller chip is the first to assemble MPEG-2 packets on chip. This offloads the task from the host system's microprocessor or microcontroller. Thus, the chip can configure MPEG-2 or digital-satellite-system (DSS) data for transport over 1394/Firewire interfaces at speeds of up to 200 Mbits/s.

The TSB12LV41, also referred to as the MPEG2Lynx, includes a multimode 8- or 16-bit host interface. When the chip accepts decoded MPEG-2 data from the system processor, it automatically inserts the required time stamp and packet header, and assembles the 1394 packets in conformance with the proposed International Electrotechnical Commission's (IEC) 61883 standard.

A large on-chip FIFO (8 kbytes) can be logically partitioned as transmit and receive FIFO buffers of various sizes, depending on the application requirements. Furthermore, the chip's internal memory is large enough to support bidirectional transmission of MPEG-2/DSS asynchronous and isochronous traffic. To aid in system development a daughtercard contain-

(continued on page 159)

EDA
Marketing Tool!

The 1996 Electronic Design Automation (EDA) Study sponsored by *Electronic Design* magazine, provides critical survey information with a focus on EDA marketing executives and user/engineers. Conducted by the market research firm, EDA Today, L.C., results have been compared, compiled, and studied to serve as strategic marketing opportunities for suppliers.

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(continued from page 156)
ing the TSB12LV41 is available, and it can be attached to the company's already available AV7000 evaluation module. In lots of 1000 units, the link-layer controller sells for $13.94 each. Samples are immediately available. DB

Texas Instruments Inc., *Semiconductor Group, SC-97042, Literature Response Center, P.O. Box 172228, Denver, CO 80217; Steven Schnier, (972) 480-3401; or on the web at http://www.ti.com/sc/1394.* **CIRCLE 507**

Commercial Rad-Hard ICs Tolerate 100 Krad (Si)

In a partnering agreement, American Microsystems will manufacture radiation-hard ICs on its 0.6-µm commercial foundry process thanks to a process-module addition developed by United Microelectronics Systems Inc. The minimally invasive processing module, combined with circuit design techniques developed by UTMC to provide single-event-upset protection, allows the commercial process to achieve a radiation tolerance of 100 krads (Si). Such production capabilities will give commercial satellite manufacturers ICs at a cost significantly lower than traditional radiation-hardened circuitry. The manufacturing line also can satisfy many of the design requirements for military hardware that's built using the commercial off-the-shelf (COTS) directives. Contact AMI directly to discuss cost and availability. DB

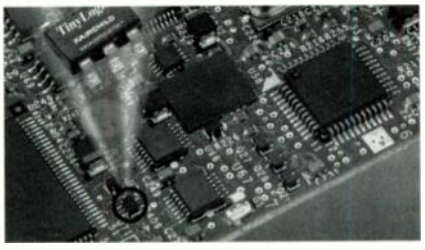
American Microsystems Inc., *2300 Buckskin Road, Pocatello, ID 93201; (208) 234-6890, or on the web at http://www.amis.com.* **CIRCLE 508**

United Microelectronic Systems Inc., *4350 Centennial Blvd., Colorado Springs, CO 80907; (719) 594-8000, or on the web at http://www.utmc.com.*
CIRCLE 509

Single-Gate Logic Chips Reduce Board Space

The TinyLogic family of single-gate general-purpose logic circuits, which come housed in 5-lead small-outline transistor-style packages (SOT-23), provides designers with a reduced area solution when just a single logic gate is needed on a board. Reducing board space requirements by as much as 75% over the conventional multigate small-outline packages, the TinyLogic family includes logic devices from the UHS, HS, and HST high-speed logic series.

The UHS devices have an operating voltage range of 1.8 to 5.5 V, and can interface with 5-V components



while operating from a 3-V supply. When operating from a 5-V supply, they have a typical propagation delay of 2.4 ns or when operating at 3 V, can drive loads of up to 24 mA.

The HS devices are targeted at 5-V systems and have a propagation delay of 4 ns. However, they can operate over a 2- to 6-V range. Lastly, the HST circuits offer translation of TTL levels to CMOS levels and they're targeted at 5-V systems, offering propagation delays of 7 ns. Prices for the UHS series TinyLogic chips start at $0.24 each in lots of 10,000 units, while HS and HSTseries devices start at $0.20 each, also in 10,000 unit lots. DB

Fairchild Semiconductor Corp., *333 Western Ave., MS 01-07, South Portland, ME 04106; (207) 775-8775; http://www.fairchildsemi.com.*
CIRCLE 510

Glint TX Gold Graphics ICs Up 3D Performance

With increased polygon performance by 33% over the previous Glint processors, the Glint TX Gold processor set offers a speed-enhanced "bundle" of the Glint 500TX and the Glint Delta processors at a reduced combination price. The chips are sold along with a new release of the company's Windows NT and OpenGL drivers for Microsoft Windows and the Silicon Graphics Graphics Language software.

With the enhanced silicon and new drivers, boards can deliver graphics throughputs of over 800k polygons/s with over 60 true-color Business Winmarks under Windows NT. Such a board also can deliver a Viewperf score of over 30 for the CDRS-03 data set, and a score of 6.5 for the Data Explorer Viewperf data set (on a Pentium II, 266-MHz platform). Boards based on the Glint TX Gold can support 24-bit, true-color, double-buffered high-resolution displays with true 8-bit overlay support for applications such as Softimage 3D and I-deas.

Additional features supported include full high-precision 24- or 32-bit Z buffering, four-stencil planes, advanced per-pixel clipping, and 4-by-4 subpixel antialiasing. Boards based on the Gold chip set start at about $2495 and include 32 Mbytes of graphics memory and support for higher resolutions such as HDTV. DB

3Dlabs Inc., *181 Metro Dr., Ste. 520, San Jose, CA 95110; Neil Trevett, (408) 436-3455; or on the web at http://www.3dlabs.com.* **CIRCLE 511**

Serial EEPROM Delivers 4 Kbits Over SPI Port

Operating at clock frequencies of up to 3 MHz, the 25C040 provides 512 bytes of EEPROM storage in an 8-lead DIP or SOIC package, or in a 14-lead TSSOP. The circuit can interface directly to the popular serial peripheral interface (SPI) port included on many microcontrollers, such as those from Microchip, Motorola, and others. The 25C040 also offers several security features, including user-selectable write protection. The chip has a guaranteed data-retention time of more than 200 years and an endurance of 10 million erase/write cycles.

Versions of the serial memory are available in 5-V and lower-voltage options that operate at levels below 3-V—the 25LC040 and the 25AA040. The 4-kbit chip adds a lower-density option to the previously released 8-, 16-, and 32-kbit family members. Supporting the EEPROM is a special Designer's Kit. This development tool helps reduce the time required for system integration and hardware/software debugging. Included in the kit are a Total Endurance software model (version 2.2), and the SEEVAL, a serial EEPROM evaluation and programming system. Price for the 25C040 starts at $0.71 each in 1000s for the commercial-temperature-range, PDIP version. DB

Microchip Technology Inc., *2355 West Chandler Blvd., Chandler, AZ 85224-6199; Keith Pazul, (602) 786-7668; http://www.microchip.com.*
CIRCLE 512

Full-Duplex Digital Radio Chip Set For WLAN, WLL, PCS

Originally developed for wireless LAN applications, the new full-duplex version of the PRISM radio chip set also is suitable for many other tasks. These include wireless local loops, RF-based T1/E1 links, handheld data transceivers, and personal communications systems (PCSs). Capable of operating between 1.7 and 2.7 GHz, the eight-chip set can be used to construct full-duplex digital radios that perform all RF and baseband functions, including amplification, down-conversion, demodulation, and upconversion.

A variety of radio designs can be implemented with this chip set, with carrier frequencies of 2.0 to 2.7 GHz and IFs from 10 to 400 MHz. The PRISM radio's high sensitivity (–11 dBm) and wide AGC range (90 dB) allows it to be used in many high-performance applications, with data rates as high as 4 Mbits/s.

Individual ICs within the PRISM chip set are the HFA3421 LNA (1.7-2.3 GHz), the HFA4324 LNA (2.4-2.5 GHz), the HF3524 dual synthesizer, the HFA3661 RF/IF downconverter, the HFA3761 AGC and quadrature IF demodulator, the HFA3663 upconverter with gain control, the HFA3925 RF power amplifier (2.4 GHz), and the HFA3926 power amplifier (2.0-2.7 GHz). All of the chips can operate on power supplies ranging from 2.7 V to 5.5 V.

Sampling now, with full production quantities available this fall, the PRISM chip set is priced at $65 for 100,000-piece orders. LG

***Harris Corp.**, Semiconductor Sector, P.O. Box 883, Melbourne, FL 32902-0883; (800) 4-HARRIS, ext. 7729.*

CIRCLE 513

10-Bit Gigabit Transceivers For Ethernet And Fibre Channel

A family of gigabit-speed transceivers is now available for both Ethernet and Fibre Channel communications products. The CXB1589R is designed for use in 1.25-Gbit/s gigabit Ethernet systems, while the CXB1586R and the CXB1586AR are intended for1.06-Gbit/s Fibre Channel applications. The family's fourth member, the CXB1584Q, can be used for transporting Fibre Channel or gigabit Ethernet traffic. All parts require only a single 3.3-V supply, except for the CXB1584Q . For TTL/CMOS interface applications, the CXB1584Q may also be run with a +5.0/+3.3-V dual power supply.

The CXB1589R features an on-chip PLL, plus an on-chip byte sync detector and built-in local loopback circuitry. The CXB1584Q is designed for use in both 1.06- and 1.25-Gbit/s applications, and offers a selectable 125-MHz or two-phase 62.5-MHz transmit byte clock. Also included in the transceiver are an on-chip PLL, a byte sync detector, test pattern generator, and local loopback circuitry.

Housed in PQFP packages, all products will be available by August, 1997, except for the CXB1584Q, which will be available in September. Pricing in 1000-piece lots is $15 each for the CXB1586R and CXB1586AR, $20 for the CXB1589R, and $25 for the CXB1584Q. LG

***Sony Semiconductor Of America**, 3300 Zanker Rd., San Jose, CA 95134; (800) 228-SONY or (408) 955-6572; fax (408) 955-5176; www.sony.com/semi.*

CIRCLE 514

RS-232/-485 Transceivers Use 5 V, Have Selectable Slew Rates

The LTC1387 is a single-port RS-232/RS-485 transceiver that operates off a 5-V supply and switches between RS-232 and RS-485 operation under software control. Drawing under 7 mA of current during operation, it can be placed in a standby mode where it draws only 5 µA The device incorporates an on-chip charge pump that requires only four 0.10-µF capacitors to generate the boosted plus/minus voltage supplies required for RS-232 operation.

It can be software configured as a pair of RS-232 drivers and receivers, or as a single RS-485 driver and receiver. Separate driver and receiver enable controls provide the flexibility to operate in full-duplex, half-duplex, or receive-only modes. The LTC1387 also features logic-selectable fast/slow driver skew rates for the RS-485 transceiver, allowing data delivery at 5 Mbits/s, or at 150 Mbits/s for reduced EMI.Pricing is $4.50 each, in 100-piece quantities. LG

***Linear Technology Corp.**, 1630 McCarthy Blvd., Milpitas, CA 95035-7417, (408) 432-1900, fax (408) 434-6441.*

CIRCLE 515

RTOS Has Seamless Links To Comm Protocol Software

The VRTX real-time operating system (RTOS), developed by Microtec, Santa Clara, Calif., has recently announced that it's co-marketing a series of portable communications software packages developed by Trillium Digital Systems, Los Angeles, Calif. Trillium offers a series of software packages that handle the signaling monitoring, and control tasks of most major communications protocols, including ATM, SS7, Frame Relay, ISDN, V5, and X.25. In addition, Trillium is developing a systems service layer that will ease the integration of all of its protocol stacks with Microtec's VRTX, its telecommunications management network (TMN) software, and other applications.

VRTX already supports TCP/IP and other Internet protocols, as well as the OSI protocol stacks. The combined software product offering is expected to greatly accelerate product development time by offering seamless compatibility between the RTOS and its application software. Available by the fourth quarter of this year, pricing varies according to the particular application. LG

***Microtec**, 2350 Mission College Boulevard., Santa Clara, CA 95054; (800) 950-5554 or (408) 980-1300; fax (408) 982-8266; or on the Internet: http://www.mri.com.*

***Trillium Digital Systems Inc.**, (310) 442-9222; http://www.trillium.com.*

CIRCLE 516

Gigabit Ethernet MAC Chip Is Now Available

The SEEQ 8100 Gigabit Ethernet media access controller (MAC) provides a complete full-duplex MAC function for line-interface cards, switches, and other networking devices. Among the first to support the emerging Gigabit standard, the 8100 also contains a Gigabit Physical Coding Sublayer (PCS), which performs packet encoding and decoding.

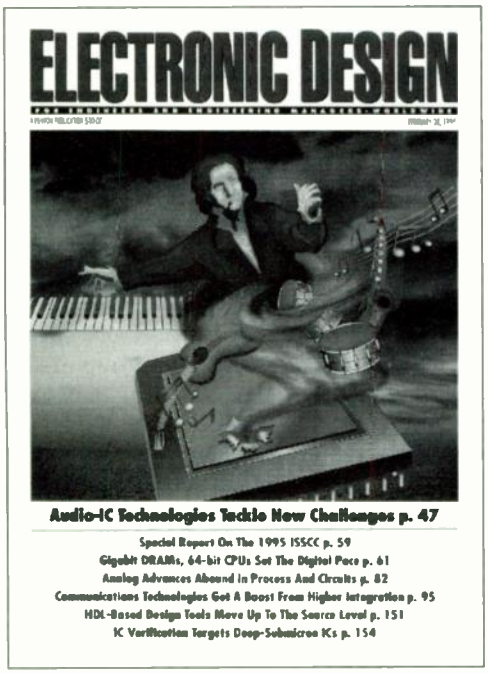
Available now, the SEEQ 8100 is priced at $45 each in 10,000-piece quantities. LG

***SEEQ Technologies Inc.**, 47200 Bayside Pkwy., Fremont, CA 94538; (510) 226-7400; fax (510) 657-2837; or on the Internet: http:// www.seeq.com.*

CIRCLE 517

STRATEGIC PARTNERS WORKING TOGETHER

Information has always been a part of the developmental strategy needed for success in the OEM market. In today's fast-paced, competitive global market environment, technology information has become a priority. Systems designers not only want to know what their strategic supply partners are doing today, but where they're going. Designers and suppliers must now work in tandem to align enabling technology with the customer's system requirements. These strategies demand strong partnerships in the development of competitive products.



A third strategic partner completes this alliance. This partner's mission is to observe and report today's product availability by its editorial staff of respected experts, while constantly probing for the next generation of enabling technology. The constant flow of exclusive and vital information helps to bring systems designers and suppliers together as strategic partners. It also provides engineers and engineering managers with an enhanced ability to bring more competitive products to market, faster.

Electronic Design is that strategic information partner — a partner who provides the information that helps the systems designer make those critical decisions that stay the course of the technology road map.

Your Strategic Information Partner.

ELECTRONIC DESIGN

A · PENTON · PUBLICATION

Bulletin Gives Data On Ferrite Paste Used For Inductors

A new bulletin from EMCA-REMEX Products supplies technical information for a ferromagnetic thick-film paste used in the manufacture of screened printed inductors. The 4920 ferrite paste is used in the construction of inductors of up to several hundred nanohenries in a 0.2-by-0.2-in. area, and for operation into low-gigahertz frequencies. The bulletin gives the paste's electrical properties and various formulation properties. Also discussed are the various design and processing considerations when making printed conductors. To obtain a free copy of the 4920 ferrite paste bulletin, call the comapny at (215) 855-1000; fax (215) 255-8202; or e-mail: *john.wood@nstarch.com*. LM

CIRCLE 485

Catalog Details Board-Interface Systems

The new *F-197 Sudden Solution Guide* features board-interface systems from Samtec Inc., New Albany, Ind., for card-to-board, board-to-board, and off-board applications. New products in the catalog include the company's patented Flex-Card system for socketing pluggable modules, micro-circuit cards, and other on-board integrated systems. Additional products include interconnects on micro and standard pitch, right-angle headers and sockets, and IDC and flex cable systems. For a copy of the new catalog, call Samtec at (800) SAMTEC-9; fax (812) 948-5047; or e-mail: *info@samtec.com*. The company's Internet address is at *http://www.samtec.com*. LM

CIRCLE 486

Product Brochure Puts You In Touch With Operator Interface

Total Control Products Inc., Melrose Park, Ill., has published a color brochure detailing its new OpCenter operator interface. The panel-mount workstation contains a touchscreen interface and features rugged construction, the latest in flat-panel screen technology, and advanced interface software. The MMI software has multimedia and animation-integration capabilities. Product specifications and options are included in the brochure. For a free copy, call (888) THINKOI or fax a request to (708) 345-5670. The company's Internet address is *http://www.total-control.com*. LM

CIRCLE 487

Catalog Has LED Displays That Don't Need Separate Sockets

If you're tired of using right-angle sockets with LED displays, check out a new four-page color catalog from Lumex Opto/Components Inc., Palatine, Ill. The catalog showcases the company's new family of chip-on-board LED numeric displays and 10-bar light arrays that don't require separate right-angle sockets. These sockets often cost more than the display itself. For a free copy, call (800) 278-5666 or (847) 359-2790 and request catalog 2007-3. You can also fax (800) 944-2790 or (847) 359-8904; e-mail: *sales@lumex.com*, or visit the company's Internet address at *http:///www.lumex.com*. LM

CIRCLE 488

Handbook Educates About Self-Locking Fasteners

The *Self-Locking and Self-Sealing Fasteners Handbook* is available free from Long-Lok Fasteners Corp., Cincinnati, Ohio. The handbook, which serves as a quick reference for engineers, covers the basic types of self-locking fasteners and how they work. Also discussed are various applications and torque calculations. And a selection guide helps you find just the right fastener for your needs. For a copy of the handbook, contact the company at (800) LONGLOK, or fax (513) 772-1888. LM

CIRCLE 489

Review A Year of Datel Product Announcements

A 20-page publication from Datel Inc., Mansfield, Mass., reviews the company's 50 new products introduced during the past year. Products are included from all of Datel's four core product lines: switching dc-dc power converters, digital panel voltmeters and instruments, sampling analog-to-digital converters, and analog I/O boards. The brochure introduces Datel's fax-back document-delivery system. For a free copy of the brochure, call (800) 233-2765 or (508) 339-3000; fax (508) 339-6356; or e-mail: *datel-lit@mcimail.com*. LM

CIRCLE 490

Value-Added Assembly Services Described In Brochure

An eight-page brochure details the range of value-added assembly and production services available from Powell Electronics Inc., Philadelphia, Pa., for building electronic subsystems. The range of Powell+Plus services include connector, switch, and battery value-added services; IDC; RF; and discrete cable assemblies and harnesses. The brochure also describes Powell's intermediate-level and turnkey sub- and final-contract manufacturing for simple and complex assemblies. For a free copy of the Powell+Plus brochure, call (215) 365-1900; fax (215) 365-7245; or e-mail: *plus@powell.com*. The company has a web site at *http://www.powell.com*. LM

CIRCLE 491

Catalog Focuses On Data-Conversion Products

A comprehensive new catalog from ILC Data Device Corp. (DDC) covers the company's extensive line of data-conversion products. ADCs, DACs, digital-to-synchro and digital-to-resolver converters, and many others are described. There are also individual data sheets given for each product. To obtain a free copy, call DDC's Customer Service Group at 1 (800) DDC-5757. Or visit the company's web site at: *http://www.ilcddc.com*. RE

CIRCLE 492

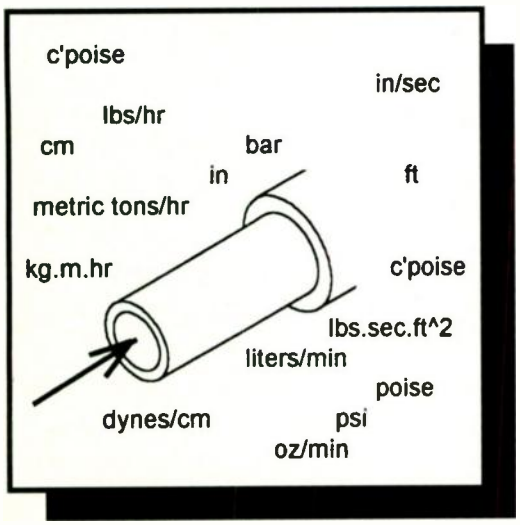
New FLUIDTOOLS with elbows and valves solves pipe and tube flow problems on your PC

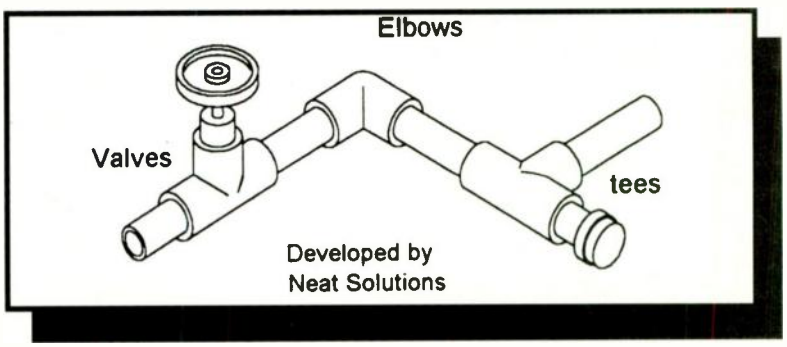
Wouldn't it be nice if you could solve flow problems without having to look up all of your data? With FLUIDTOOLS, you can do just that? It's easy as A-B-C.

- **Just enter your data in whatever units you wish . . .**
- **Request FLUIDTOOLS to return answers in the units you want . . .**
- **Press "calculate" . . .**
  It's that simple!

FLUIDTOOLS solves liquid and gas flow problems including escaping gas problems. It can solve for diameter, length, flow rate, pressure, or viscosity when doing liquids. Gas problems solve for quantity and DPSI.

Program accepts mixed units





Some of the important Features of FLUIDTOOLS . . .

Automatic unit conversion . . . enter data in mixed units and FLUIDTOOLS automatically calculates in the units you want • Friction and expanding gas factors are automatically calculated • All factors can be overridden • Program data base includes elbows, valves, fittings, viscosity, specific gravity and pipe sizes •A wide range of common and uncommon metric and English conversion factors are included and are easily expandable to accept user-defined data • Menus for pipe roughness are provided, or you can key in your own • Program can save all user defined data. All tables can be edited and expanded using the special editor included.

FLUIDTOOLS program disk and user manual $295

System Requirements:

IBM PC line of computers or 100% compatibles
DOS 2.0 or higher
320K minimum memory

SATISFACTION GUARANTEED! Run FLUIDTOOLS on your PC. If the program doesn't perform as described, just return it within 30 days for full credit or refund!

Chargecard users order toll-free 800-223-9150
(In Ohio 216-696-7000) or FAX your purchase order to 216-696-6023

Mail orders to:

Penton Education Division • 1100 Superior Avenue • Cleveland, Ohio 44114

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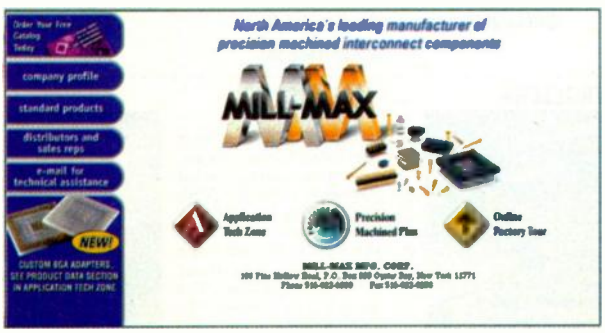
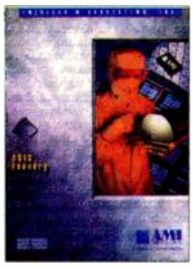


ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

FOUNDRY

American Microsystems, Inc. has offered custom and semicustom foundry expertise for over 30 years. AMI supports o.35µ through >1µ design and will increase its production capacity by 3x with the completion for FAB 10. For more information on AMI's foundry, call (208)233-4690 or visit our home page http://www.amis.com



CIRCLE 250

AMERICAN MICROSYSTEMS INC.

"No-Power" Cholesteric Liquid Crystal Displays

Kent Displays' brochure details the benefits of No-PowerÔ Reflective Cholesteric Liquid Crystal Displays. This technology requires no energy to maintain an image. Displays have wide viewing angels and are flicker free. Call (330) 673-8784.

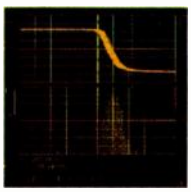
CIRCLE 251

KENT DISPLAYS

FREE T & M PRODUCTS CATALOG

The 1997 catalog from Lecroy offers complete technical information and pricing on our complete line of digital oscilloscopes. Also included are technical application notes covering many topics.

1-800-4LECROY



CIRCLE 252

LECROY

FACTOR PFC

The compact, 200W PFC Series switcher provides a 0.99 power factor corrected input with 2-48V main output. three additional, fully isolated outputs each provide 5,12,15,or 24 VDC. Phone: 800-4-XENTEK.

Fax: 760-471-4021

CIRCLE 253

XENTEK POWER SYSTEMS

V-SYSTEM/VLOG

Model Technology offers simulations for VHDL, Verilog and mixed-HDL on workstation and PC platforms. Model Technology provides technology- leading solutions for all your ASIC and FPGA needs. Model Technology's suite of HDL tools are fully compliant with leading industry standards. For more information, call 503-641-1340 or visit our home page http://www.model.com

CIRCLE 254

MODEL TECHNOLOGY

ADHESIVES AND SEALANTS

Master Bond Inc., Hackensack, NJ manufactures over 3000 grades of adhesives, sealants and coatings. Line cosists of epoxies, anaecobics, cyanoacrylates, silicones and acrylics. One and two part systems are available. Tel 201-343-8983.

CIRCLE 255

MASTER BOND INC.

NEW .100" PITCH SINGLE SIGNAL

Meritec Assemblies accurately control analog & digital signals for applications with 3ns to sub ns edge rates while matching requirements for controlled impedance, high speed & low crosstalk. SSI terminations available in booth single & multiple configurations to mate with .025" backplane pin fields & industry standard harders. Cables with impedances from 50 to 100 ohms available for use in single & differential mode applications.

CIRCLE 321

MERITEC

RELIABILITY PREDICTION

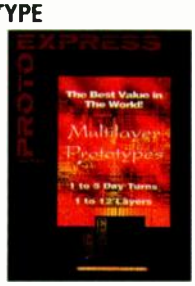
Catalog describes the RelCalc2 software package, which automates Mil-HDBK-217 or Bellcore on your PC, and allows quick and easy reliability analysis of your electronic products. Phone: (818) 991-0057, Fax: (818) 991-1281

CIRCLE 256

T-CUBED SYSTEMS

MULTILAYER PROTOTYPE

Award winning quick turn multilayer prototype manufacture specializing in 24 hour to 5 day turns, for commercial and milspec boards (Milp-55110E) on FR4 and polyimide materials. Our capabilities also include "blind and buried" vias, full body gold, carbon baste, metal core boards, small hole drilling, and net list testing.



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PROTOS IN 12 HOURS...

Keep up with the Global Pace...On Time Every Time, assisting you to stay ahead of the fast moving. Electronics Industry. Single/multi-layer FR4 Prototype P.C. Boards in 12 hours to 5 day turns. Other services include: Surface Mount & Thru Hole Assembly. Prototype & Production. SMOBC & LPI. Gold/Nickel plating. Scored Panels. Single to Multilayers. Electrical Testing. Instant Quotes. UL Approved. Tel: 847-290-9900. Fax: 847-290-9901

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Imagineering specialized in FAST TURNAROUND, High Quality. Multi-layer, FR4 PC Boards. Other Services include SMOBC & LPI, Bare Board Electrical Testing. Gold/Nickel Plating, Scored Panels, Blind & Buried Vias. Complete CAD/DFM Service. UL approved and more.

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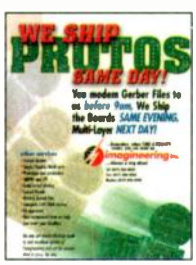

CIRCLE 259

IMAGINEERING

FAST TURNAROUND PROTOTYPES

Accutrace offers the Best Quality along with Excellent Service and Best Turnaround Time. Our capabilities include SAME DAY Prototypes, Instant Quotes, SMOBC & LPI, Scored Panels, Electrical Testing, SMT & Thru Hole, Complete CAD/DFM, Gold/Nickel Plating, Blind & Buried Vias,

UL Approved and more.

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CIRCLE 260

ACCUTRACE INC.

470MHZ ANALOG OSCILLOSCOPE

IWATSU Manufactures 100, 200, 400, 470MHZ analog scopes & accessories. IWATSU is the sole manufacturer of 400MHZ analog scopes & 60KV high voltage probe. Our free 16-page color catalog features product information & applications. Phone: (201) 935-8580

CIRCLE 261

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LOW COST 16-BIT CONTROLLERS

Easy to program in Borland/Microsoft C/C++. Low Cost, High quality, Reliable, Compact, Made in U.S.A. More than 20 controllers with ADC, DAC, solenoid drivers, relay, PC-104, PCMCIA, LCD, DSP motion control, 10 UARTs, 100 I/Os. For industrial control, test, and data acquisition. Customer boards design. Save time and money. Phone: 916-758-0180,

FAX: 916-758-0181

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CIRCLE 262

TERN, INC.

NETRANS™

NETRANST™ and NETRANSplus™ from American Microsystems, Inc. provides proven netlist conversion technology.With over 800 FPGA to ASIC conversions to date, AMI has the most experience and greatest success rate for netlist conversions. For more information on NETRANS products, call (208) 233-4690 or visit our home page http://www.amis.com

CIRCLE 316

AMERICAN MICROSYSTEMS, INC.

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

INDUSTRIAL PC POWER SUPPLY

ICP Acquire Inc. is a manufacture of single Board computers, provide Backplane, rackmount chassis , and Industrial Power supplies. Including: 3-20Slot BP, 386/486/Pentium SBC, 3-20Slot chassis, DC-12V/24V-48V PS and 85-265V AC PS. Contact Allen, phone: 415-967-7168

CIRCLE 263

ICP ACQUIRE, INC.

DEVICE PROGRAMMERS & HANDLERS

The Data I/O® catalog is the direct-order source of affordable tools for users of programmable devices. From design software to device programming and automated handling systems, the Data I/O catalog offers unbeatable values on the high quality tools you need. Call 1-800-332-8246, ext. 806

CIRCLE 264

DATA I/O

80186, 80196, 8051 EMULATION

Signum Systems has released its 1996 catalog of in-circuit emulators. This full line catalog includes Intel processors, Texas Instruments DSP's Zilog controllers, and National Semiconductor HPC family. Call (800) 838-8012 for information. Internet address: ww.signum.com

CIRCLE 265

SIGNUM SYSTEMS

OFF-THE-SHELF-OPTICS

Free 130 page product catalog from Rolyn, largest supplier of off-the-shelf optics. 24 hour delivery of simple or compound lenses, filters, prisms, mirrors, beamsplitters, reticles, objectives, eyepieces & thousands of other stock items. Custom products & coatings also. Phone: (626)915-5707, Fax: (626) 915-1379

CIRCLE 266

ROLYN OPTICS CO.

NEW SWITCHING REGULATORS

Power Trends, Inc. has released a new 80 page full-line catalog for its complete line of Integrated Switching Regulators and DC to DC converters. the catalog introduces significant new products along with extensions to existing product lines. Complete specifications, photos and standard applications are provided for each product along with mechanical configuration options and ordering information.

CIRCLE 267

POWER TRENDS, INC.

VLSI INTERCONNECTION SPECIALISTS

Call for a complete range of Interconnect Solutions including hundreds of Prototyping Adapters, Test Probe Adapters, Programming Adapters and many other interconnect devices. for fully compliant surface mount interconnect test adapters, we offer a wide selection of high quality solutions. We also have quick turn custom design services for unique solutions in packaging.

CIRCLE 268

IRONWOOD ELECTRONICS

CLEANABLE ELECTRONIC AIR FILTERS

Quadrafoam cleanable air filters provide high efficiency and low resistance for electronics applications, including limited space environments. They are custom-dedigned to specification by Universal Air Filter Co., and are Bellcore certified. The filters are designed for electronics, computer, telecommunications, medical and general purpose equipment applications. Phone (800) 541-3478. Fax: (618) 271-8808. www.uaf.com

CIRCLE 320

UNIVERSAL AIR FILTER

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Teltone's 224-page Databook features a wide range of products for network interface applications, including: DTMF Receivers, DTMF Transceivers w/Call Progress Detection, MF Trunk Signaling ICs, Call Progress Tone Detectors, Line Sensing Relays, test tools including Telephone Line Simulators and ISDN Line Simulators, application notes, and more. For your copy call 1-800-426-3926 or 206-487-1515, E-mail at info@teltone.com.

CIRCLE 269

TELTONE

TANNER TOOLS PRO™

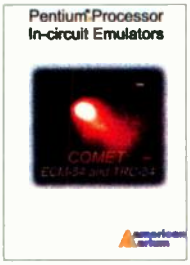
Tanner Research offers powerful, easy to use, PC/MAC/Unix design tools for IC, MCM and MEMS applications. Output CIF & GDSIL. Send for free demo and literature, or download from our web page at www.tanner.com. PH: 818-792-3000, Fax: 818-792-0300, Email:sales@tanner.com

CIRCLE 270

TANNER RESEARCH

COMET IN-CIRCUIT EMULATORS

American Arium has been the primary market supplier of Pentium® processor In-circuit Emulators since 1991. In 1995, the company introduced their Pentium® Pro In-circuit Emulator. Recently, American Arium announced the release of Comet In-Circuit Emulators. These were specifically designed for the embedded software developer, with special attention paid to the 66Mz real-time trace engine and ultra-accurate breakpoints. The Comet ECM-54 is a portable low cost solution which provides processor control through the Intel defined, JTAG debug port. Comet TRC-54 is a full featured In-Circuit Emulator with American Arium Data Capture Technology.



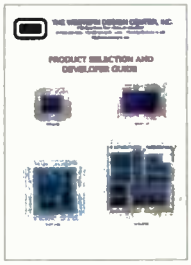
CIRCLE 271

AMERICAN ARIUM

W65C02S - BASED PRODUCTS

Western Design Center's product selection and developer guide describes our 65C02-BASED CMOS low power IC microprocessors. Included is information about our chips, boards and licensable cores.

www.wdesignc.com.



CIRCLE 272

WESTERN DESIGN CENTER

6050 I/O With I/Q

Octagon Systems has introduced a new family of single card industrial computers called the PC Microcontroller Series. The card family combines the industry standard PC architecture with industrial- class I/O and an extensive suite of embedded software in a small 4.5 X 4.9 package rated from - 40° to 85° C.

CIRCLE 273

OCTAGON SYSTEMS

C-PROGRAMMABLE CONTROLLERS

Save time and money.. Our controllers are ideal for control, test or data acquisition applications with a mix of analog/digital/ I/O, relays, RS232/485 serial ports, LCD/keypads, & programmed with Dynamic C™ . From $79, Qty. 1 (916)757-3737, or Fax: (916) 753-5141. For 24 Hr. data, call from YOUR Fax: (916) 753-0618. http://www.zworld.com.

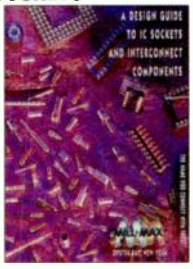
CIRCLE 274

Z-WORLD ENGINEERING

DESIGN GUIDE TO IC SOCKETS

MILL-MAX features its newly expanded family of precision machined interconnect components including PCB pins, wrapost & solder terminals plus a complete line of SIP, DIP & PGA sockets. The guide highlights over 70 new products in pins, surface mount components & large I/O PGA sockets. Phone: 516-922-6000. Fax:516 922-9253.

e-mail:techserv@mill-max.com
online: www.mill-max.com



CIRCLE 275

MILL-MAX

HIGH PERFORMANCE nvSRAMs

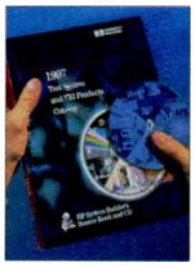
Discover the world's fastest and most economical nonvolatile SRAM's. SRAM read and write speeds to 25ns. All new data saved in a single cycle. Program, data and SRAM in one chip. No batteries or contacts to fail. No data loss from noise or undershoot. No memory block management or erase. No sockets, brackets or "snap on's". SRAM, EEPROM & EPROM pinouts. DIP and small surface mount packages. Commercial, industrial and military. Call 800-637-1667

CIRCLE 326

SIMTEK CORPORATION

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

VXI PRODUCTS



The new HP Systems Builder's source includes comprehensive technical information for the most complete selection of test system components available. Test system and VXI components, HP VEE - the graphical programming language for test engineers, and custom system integration services are detailed for solutions in electronic manufacturing test and data acquisition applications ranging from telecommunications to automotive. For FREE catalog and CD-ROM, call 1-800-452-4844, ext. 1801.

CIRCLE 276

HEWLETT-PACKARD

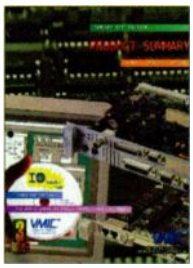
CRYSTALS & OSCILLATORS

The 1997 International source Book offers detailed specifications on Ecliptek's through-hole and surface-mount crystals and oscillators. Visit our internet site at http://www.ecliptek.com. Phone: (714) 433-1200, Fax: (714) 433-1234, or E-mail: ecsales@ecliptek.com.

CIRCLE 277

ECLIPTEK

FREE VMIC PRODUCT CATALOG



VMIC's Product Summary Catalog features the world's widest selection of VMEbus I/O, VMEbus CPU's, Real-Time Networks using VMIC's reflective memory products for VME, PCI, PMC, Multibus, IOWorks component software, and a host of other products designed to provide complete, open solutions from one vendor. Phone: 800-322-3616. http://www.vmic.com

CIRCLE 278

VMIC

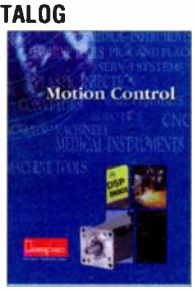
1997 PRODUCT CATALOG

Pentek's new 1997 Product Catalog provides specifications on our VME, VXI, PCI and PMC products. You'll also find tutorials, case studies and applications stories. Get all the information on the broadest line of DSP processors, analog and digital I/O, digital receivers and world-class software tools. Send for your free copy today, or call (201) 818-5900 Ext. 669. www.pentek.com, info@pentek.com

CIRCLE 279

PENTEK, INC.

MOTION CONTROL CATALOG

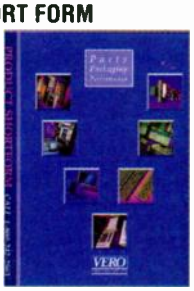


GESPAC' intelligent motion controller uses a 40MHz MC56002 DSP to control 2 or 4 DC, AC or brushless motors. Versions of the board are available for the VME, G-64 and soon for the ISA and Compact-PCI buses. The board comes with a powerful PC based software package that helps you automatically determine the mechanical characteristics of the drive assembly and more.

CIRCLE 280

GESPAC

NEW PACKAGING SHORT FORM



New VERO shortform summarizes industry's broadest range of electronic packaging hardware, including: IMRAK cabinets for electronic component housing and cable management; cardframes; Diplomat desktop enclosures; IBX and Veronex plastic eclosures ; and a full range of blackplanes, microracks and plug-in power supplies. Phone: 800-642-VERO ; Fax: (203) 949-1101.

CIRCLE 281

VERO ELECTRONICS

PLUG-N-PLAY CONTROLLER

Fairchild Semiconductor unveils a versatile Plug-n-Play controller that also supports Non-Plug-n-Play platforms like Windows-NT, DOS, Windows 3.1, UNIX, Novell and others. The NM95MS18 is the first PnP controller to allow several cards to share a single interrupt channel, consistent with the PC' 97 recommendations laid out by Microsoft Corporation. For more information and samples, call 1-800-272-9959

CIRCLE 324

FAIRCHILD SEMICONDUCTOR

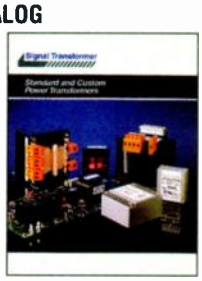
THE SMARTEST PROGRAMMER

The catalog covers our entire product line and includes comprehensive supported device listings, all available options and features, and a complete price list. For information, call Yvon J. Blais Phone: (407) 649-3335, FAX: (407) 649-3310

CIRCLE 282

DATAMAN

TRANSFORMER CATALOG

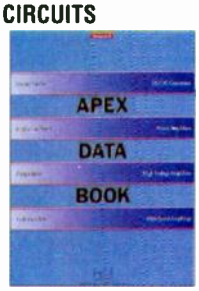


Signal Transformer Co., an operating unit of the Insilo Technologies Group, has just released a new 40-page, 4 color catalog that is an ideal reference source for engineers and buyers. signal Transformer offers the most extensive line of 50/60 Hz transformers available in a power range of 1 VA to 10 KVA.

CIRCLE 283

SIGNAL TRANSFORMER

POWER INTEGRATED CIRCUITS



The 7th edition Apex Power Integrated Circuits data book contains complete product data sheets and applications notes for Apex Microtechnology's power Amplifier PWM Amplifier and DC/DC Converter product lines.

Call: 1-800-862-1021; Fax:1-520-888-3329 Email: Prolit@TeamApex.com

CIRCLE 284

APEX

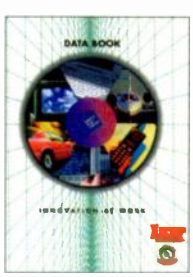
HI PERF CABLE ASSEMBLIES

Brochure for engineers needing to know the current level of advanced capabilities in the integrated design and manufacture of miniature cables and high density terminations.

CIRCLE 285

PRECISION INTERCONNECT

FREE! FREE! FREE!



Xicor's broad line of in-the-system programmable semiconductor integrated circuits retain information even when system power is lost or turned off. In-the-system programmability telecommunications, consumer, computer industrial, automotive and military products to adapt to changing software and operation environments. Call (408) 432-8888 Ext. 3336.

CIRCLE 286

XICOR

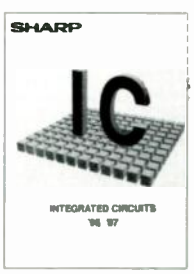
SPECTRA® DEVELOPMENT SYSTEM

Microtec's Spectra development system combines our renowned development tools - including the XRAY debugger and C & C++ compilers - with VRTX, the most proven, robust RTOS in the industry. Spectra's host-based approach addresses the full range of embedded applications from resource constrained devices with no real-time operating system requirements up to the most complex multiprocessor systems. www.microtec.com, 1-800-950-5554.

CIRCLE 287

MICROTEC

SHARP FIFOs

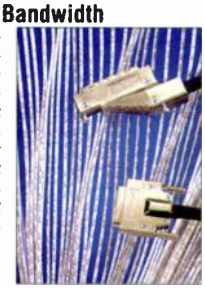


First-in, First-out memories are just the stuff the nonsense design environment of the '90s is meant to build on. Used as data buffers between systems operating at different speeds, FIFOs conserve valuable board space, streamline design tasks and reduce system cost. Sharp's new 1997 IC Short Form Catalog is packed with information about Sharp FIFOs.

CIRCLE 288

SHARP MICROELECTRONICS

SKEWCLEAR™ High Bandwidth



Skewclear™ high bandwidth parallel pair cable assemblies from Amphenol are ideal for a wide range of critical applications, including SCI, Super HIPPI, LVDS, and fiber channel. with faster clock speeds and shrinking skew budgets, SKEWCLEAR™ provides four times less skew than standard cabling. Amphenol's advanced cabling technology, precision termination, and factory skew-testing assures reliability in every cable.

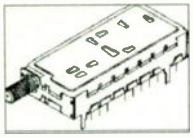
CIRCLE 319

AMPHENOL

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

SINGLE CONVERSION CATV TUNERS

Designed for reception of modulated digital data streams, CASD-series tuners are ideal for consumer set-top or PC add-in receivers. They feature PLL tuning, 62.5 kHz step sizes and low noise, with a return-path low pass filter in some models. F connector and PCP pin inputs available. Call 800-642-0261 for product information. For details via FASTFAX, call 800-833-9437, ext. 3000



CIRCLE 289

SHARP MICROELECTRONICS

MODEL TECHNOLOGY

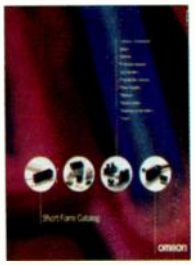
Model Technology offers simulation solutions for VHDL, Verilog and mixed-HDL on Workstation an PC platforms. Model Technology provides technology-leading solutions for all your ASIC and FPGA needs. Model Technology's suite of HDL tools are fully compliant with leading industry standards. For more information, call 503- 641-1340 or visit our home page http://www.model.com

CIRCLE 290

MODEL TECHNOLOGY

NEW SHORT FORM CATALOG

Omron's Control Components Short Form Catalog contains 200-plus pages of relays, switches, photomicrosensors, card readers, photoelectric sensors, power supplies, totalizers, digital displays, temperature controllers and timers. Call 1-800-55-OMRON. E-mail: SFC2_EDLit@omron.com



CIRCLE 291

OMRON ELECTRONICS, INC.

FREE PRODUCT HANDBOOK

Completely updated and expanded. The CDI product handbook provides full electrical and mechanical specifications on hundreds of standard power conversion products, including 230 new models. Also included: a 50 page application guide with in-depth information on power conversion topics including product testing, theory of operation, distributed power systems, thermal characteristics, safety/ reliability approvals. Tel: (508) 559-0880 Fax: (508) 559-9288

CIRCLE 292

CONVERSION DEVICES, INC.

MicroSim® DesignLab™

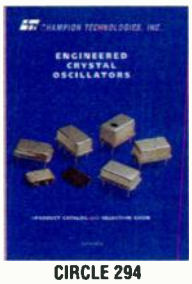
Interface Technologies distributes Version 7.1 of MicroSim DesignLab and MicroSim Pspice A/D with Schematics. Version 7.1 supports long file names in Windows 95 and Windows NT, includes DXF export, enhanced simulation libraries, library browser and search engine, and automated move, select and edit in MicroSim PCBoards. Call 1-800-357-1636 or browse http://www.i-t.com for more information.

CIRCLE 293

INTERFACE TECHNOLOGIES

CRYSTAL OSCILLATOR CATALOG

A new product catalog and selection guide from Champion Technologies features their full line of crystal oscillators. Technocal information, specifications and mechanicals are featured in this catalog for over 60 of Champion's VXCOs, TCXOs, VCTCXOs, data clocks and related products. frequency ranges up to 155.52 MHz for general purpose to high frequency or tight stability applications. Phone: (847) 451-1000



CIRCLE 294

CHAMPION TECHNOLOGIES

GIANT NEW SWITCH CATALOG

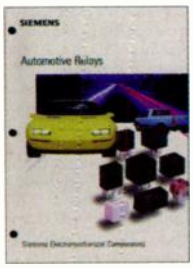
APEM's brand new 420 page full-line catalog is jam packed with their extensive switch offerings. Hundreds of new products have been added, including toggles, rockers, pushbuttons, tacts, keys, industrial controls, DIPs, and more. Many state of the art switch models are described that feature process compatibility, surface mounting technology & electrostatic discharge withstanding.Tel 617-246-1007. Fax 617-245-4531.E-mail: info@APEM.com

CIRCLE 318

APEM COMPONENTS

AUTOMOTIVE RELAYS

Siemens automotive relays, flashers and motor reversing modules are described in this 40-page catalog. Plug-in, bracket mount and PC board models with contact ratings up to 70A. Many termination, contact and enclosure options are offered. Fax: 812-386-2072; e-mail: info@sec.siemens.com



CIRCLE 295

Siemens Electromechanical Components

1998 Flat Panel Display Solutions

1998 Designer's Guide offers the latest color displays ranging from 17.7" to 6.4" and XGA to VGA resolution. Sunlight readable 900-nit. Touchscreens, enclosures, other mounting options, and SBCs including new MMX-Pentium. **Computer Dynamics, Greenville, SC**, voice: (864) 627-8800, fax: (864) 675-0106, email: sales@cdynamics.com, web: www.cdynamics.com.

CIRCLE 296

COMPUTER DYNAMICS

KEY SWITCHES SURVIVE

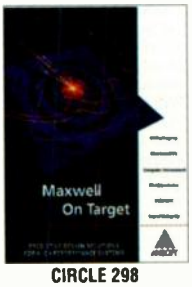
Low-profile tactile key switches with through-hole and surface-mount terminals are sealed to withstand wave-soldering and cleaning processes. Surface-mount models also tolerate reflow, vapor phase, hot-stamp, and laser soldering. The Rafi Racon 8 is approximately 5-mm high by 8-mm square; the Racon 12 is approximately 5-mm high by 12-mm square with an optional plunger to increase the height to 12.5mm.

CIRCLE 297

C&K COMPONENTS INC.

MAXWELL ON TARGET

Electromagnetics based EDA solutions for high speed and high frequency design. 2D/3D RLGC extraction and SPICE model generation for high speed interconnects, IC packages. Signal integrity, ground bounce, and EMI enclosure design rules. S-parameters, antenna parameters including gain, directivity for RF and microwave design.



CIRCLE 298

ANSOFT

PRECISION SWITCH FOR APPLICATIONS

New Catalog 106 has 80 pages featuring new sealed snap-in rockers and toggles with available illuminated indication, plus an in-depth line of precision pushbutton, toggle, rocker, limit and basic switches. Sealed and unsealed construction. Industrial, commercial and military grades. Environment-free sealed. Sub-subminiature, subminiature, miniature and standard sizes.

CIRCLE 299

OTTO Control

PFC POWER SUPPLIES

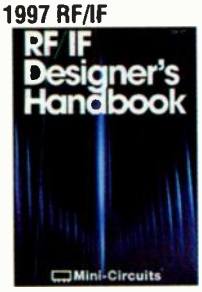
New F Series catalog describes 0.99 power factor corrected switching power supplies from our Moduflex® family of switchers. FT and FS Series models are available in 1 to 7 outputs with power ratings of 400 to 1000 watts. FX Series units feature the 7 outputs required by VXIbus standards. Send for your free copy today or call 800-523-2332.

CIRCLE 314

DELTRON INC.

MINI-CIRCUITS FREE 1997 RF/IF

Mini-Circuits brand new 760 page RF/IF Designer's Handbook is now available for distribution worldwide. The handbook is loaded with fresh design and applications information, such as modern surface mount techniques, practical articles about VCO's, ERA MMIC amplifiers and more, answers to frequently asked questions, definitions of terms, convenient selection guides and handy conversion charts.

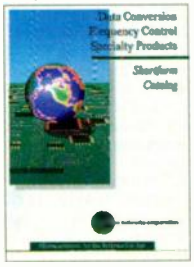


CIRCLE 317

MINI-CIRCUITS

DATA CONVERSION AND CLOCKS

Micro Networks Corp. short form catalog covering standard data converters and frequency control products. Products are designed for commercial, industrial, and military applications in computers, communications and control circuits. Phone: (508) 852-5400



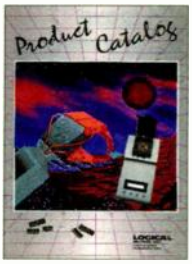
CIRCLE 326

MICRO NETWORKS CORP.

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

Product Literature News Announcement

Our 28 page four color catalog is an excellent buyers guide for design and production engineers shopping for EPROM /FLASH/PLD/FPGA design, programming, erasing and test tools. The catalog offers products for every budget and level and also includes a host of Socket converters and adapters for DIP, PLCC, TSOP, QFP technologies. For more information call Logical Devices at 800-331-7766. web: http://www.logicaldevices.com



CIRCLE 301

LOGICAL DEVICES

A WEALTH OF SWITCH INFORMATION

Grayhill's 320 page catalog provides you with electromechanical switch data, reference material, dimensional drawings and photos. Catalog No. 1 includes information on DIP Switches, Rotary Switches, Keyboards and Keyboard Modules. The detailed information allows the catalog user to select the proper product for their application right down to the part number. Phone: (708) 482-2131, Fax: (708)354-2820

CIRCLE 302

GRAYHILL, INC.

Schematic Capture to PCB Layout $995

ProCAD PowerStation 32 is complete CAD Software for Schematic Capture, PCB Layout, Mechanical drafting & Autorouting. High Performance CAD with true easy to use WIN95 compliance user interface & numerous import/export to other CAD/CAE pkgs. Prices start as low as $995.For data sheet & pricing, visit www.icadsys.com or call 408-970-0852, fax: 408-986-0524.

CIRCLE 303

INTERACTIVE CAD SYSTEMS

Kepco's New Power Supply Catalog

Kepco's new power supply catalog and handbook integrates in one volume digital and analog power supplies that allow for a high degree of control flexibility including VXI. Recently Kepco has introduced many new digital models; they are cataloged here with full specifications. Modular units include p-c card multi-output models, high-density dc-dc converters, and high power plug-in models for N+1 redundancy applications..

CIRCLE 304

KEPCO INC.

SCHEMATIC SOFTWARE

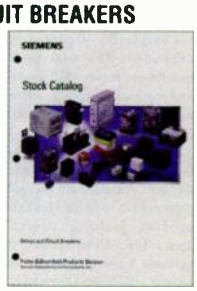
OrCAD Capture Enterprise Edition for windows NT offers an intuitive drawing interface, integrated with a component information system that links with corporate databases. It speeds the entire design process by reducing manual entry and electronically passing physical data to the board designer. For a data sheet and demo CD, visit www.orcad com or call 1-800-671-9505.

CIRCLE 305

OrCAD

P&B RELAYS & CIRCUIT BREAKERS

Newly updated 40-page catalog describes stock relays and circuit breakers from Potter & Brumfield Products Division. Lists electromechanical, solid state and time delay relays, as well as thermal and magnetic circuit breakers. Many rating, termination, mounting and enclosure options. Fax: 812-386-7072; e-mail: info@sec.siemens.com



CIRCLE 306

SIEMENS ELECTROMECHANICAL

IC CATALOG ON CD-ROM

Allegro introduces a new electronic databook with selection guides and datasheets for motor driver ICs, power ICs, Hall-effect sensors, and mixed-signal ASICs. Call (508) ALLEGRO or visit us at www.allegromicro.com

CIRCLE 307

ALLEGRO MICROSYSTEMS

Partnership Innovation Technology

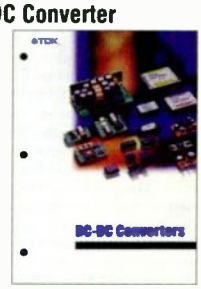
Techron's medical products brochure provides information about the companies capabilities as a supplier of gradient amplifier systems. Two new companion data sheets list specifications for the TEC7782 gradient amplifier and 8700 gradient amplifier systems. For more information visit our web site at www.techron-amps.com, call us at 219-294-8300 or send e-mail to techron@crownintl.com.

CIRCLE 308

TECHRON

TDK Offers New DC-DC Converter

TDK's new 30-page brochure covers their full line of over 600 standard DC-DC Converters. Custom configurations not cataloged are available from TDK. The power conversion products covered in this catalog are now available from stocking distributors throughout North America. Phone: 847-390-4478. Web Site: http://www.tdk.com

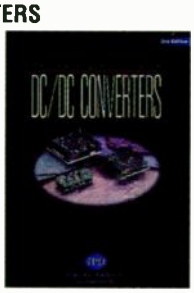


CIRCLE 309

TDK Corp. of America

NEW DC/DC CONVERTERS

IPD's advanced SMT technology delivers the highest DC/DC power densities available. A full line of new products is outlined including single, independent dual, and triple output models. Visit www.ipdconverters.com for specifications.

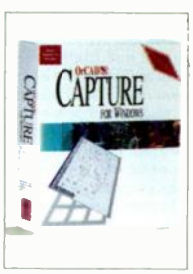


CIRCLE 310

INTERNATIONAL POWER DEVICES

FREE EDA CD-ROM

OrCAD's new Desktop Solutions CD includes product overview, detailed data sheets and working demo versions of OrCAD's 32-bit Windows software- including new OrCAD Express and Capture Enterprise Edition. Order today by calling 1-800-671-9505 or visit our website at www.orcad.com

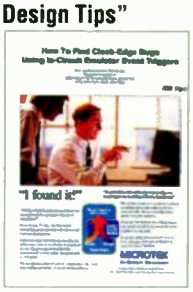


CIRCLE 311

OrCAD

"X86 and 683xx/HC16 Design Tips"

Free application note shows how to use in-circuit emulation to isolate real-time events. Set clock-edge triggers, and then use trace to display system status and the source code leading up to the event. For immediate response: WEB page: www.microtekintl.com Voice: 800-886-7333



CIRCLE 312

MICROTEK INTERNATIONAL

ISDN TRANSFORMERS

The new catalog from ISDN specialist interface manufacturer APC features: Complete range of 'S' and 'U' interface transformers and chokes. ISDN modules incorporating all dual magnetics and IC protection circuit. Approved to EN41003, EN60950, BS6301, BS415, IEC950 safety standards for supplementary and reinforced isolation.

CIRCLE 313

ADVANCED POWER COMPONENTS

2x300kHz DAQ PCMCIA Data Sheet

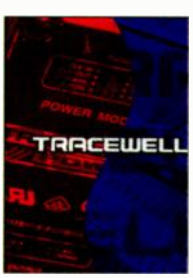
INES, Inc. Englewood, Colorado has released new updated data sheets with technical specifications regarding application interface information, hardware/software configuration, and full Data Acquisition information.

CIRCLE 325

INES, Inc.

POWER SUPPLIES

Tracewell Power Inc. offers a full line of standard and custom power supplies and distributed power products designed specifically for computer, test, and telecom systems.



CIRCLE 315

TRACEWELL POWER

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

COTS VMEbus Systems Catalog

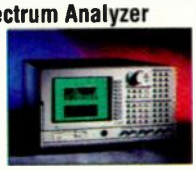
Military and severe environment systems for demanding needs at affordable prices. with more than ten years experience VISTA is committed to customer satisfaction. VISTA builds more than hardware-it brings to your project the team you can rely on to work with program management, from proposal through to deployment, to ensure an effective and successful program. Phone: 1-800-VISTA-10, sales@VISTAcc.com

CIRCLE 327

VISTA Controls Corp.

Dual Channel FFT Spectrum Analyzer

The SR780 is a two channel FFT analyzer with a frequency range of 102.4 kHz and a dynamic range of 90 dB. Features include ANSI standard octave analysis, swept sine measurements, transient capture, and computed order tracking. The SR780 comes with a low distortion source, 8MB of memory , a3.5 inch DOS disk drive and RS-232 and GPIB computer interfaces. 408-744-9040



CIRCLE 328

STANFORD RESEARCH SYSTEMS

EMBEDDED SINGLE BOARD COMPUTERS

Complete selection of embedded Single Board Computers and I/O boards including 188EB and 386EX Single Board Computers, Serial I/O, Parallel I/O, Analog I/O, Opto I/O, Reed Relay, RS-232, RS-485 networks and LCD Display, all with complete software drivers. For more information, call 1-800-RLC-TECH or visit our web site at http://www.RLC.com.

CIRCLE 329

RLC

FREE INTERACTIVE CD

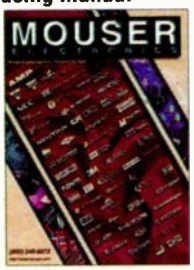
Vicor's computer program guides users through the selection and configuration process for Vicor's comprehensive line of power solutions, including modular components and complete configurable systems. 800-735-6200.

CIRCLE 330

VICOR CORPORATION

Free Electronics Purchasing Manual

Mouser Electronics presents its free Electronics Purchasing manual. the company offers same-day shipping, helpful technical assistance and a broad inventory selection. there is no minimum order required. Mouser's newest catalog features 69,000+components from 135+leading manufacturers including 3M, Amp, Dale, NEC, SGS Thomson, Sprague, plus more. Phone: 800-992-9943. http://www.mouser.com.



CIRCLE 331

MOUSER ELECTRONICS

POTENTIOMETERS

A/D Electronics' free 68 page potentiometers catalog offers a variety of potentiometers in different configurations, including snap-in insulated shaft, rotary and slide potentiometers. www.adelectronics.com

CIRCLE 332

A/D ELECTRONICS

NEW SHORT FORM CATALOG

Omron's Control Components Short Form Catalog contains 200-plus pages of relays, switches, photomicrosensors, card readers, photoelectric sensors, power supplies, totalizers, digital displays, temperature controllers and timers. Call 1-800-55-OMRON. E-mail: SFC2_EDLit@omron.com

CIRCLE 333

OMRON ELECTRONICS, INC.

A WEALTH OF SWITCH INFORMATION

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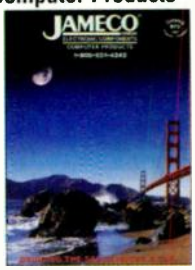
CIRCLE 334

GRAYHILL, INC.

FREE Components & Computer Products

Jameco Electronics has provided mail order electronic components products for OEMs, engineers, educators and service/repair technicians. The latest 132-page catalog includes more than 340 new products including thermistors, lamps, VCC LED hardware, Molex connectors, PCB design software, NetMouse and more! Order any Jameco's more than 5,000 electronic components and computer products toll-free 24 hours a day, 800-831-4242. http://www.jameco.com.



CIRCLE 335

JAMECO ELECTRONICS

GPIB DATA SHEET

The 1997 GPIB for PCMCIA and ISA data sheets from INES, Inc., are packed with the necessary information to help determine what type of GPIB card is best suited for all applications.

CIRCLE 336

INES, Inc.

Electronic Components/Hardware Guide

As an ISO 9002 manufacturer, Keystone Electronics offers more than 5,000 standard and custom components and hardware products for industry. These include: interconnect components; panel and printed circuit hardware; spacers and standoffs; insulating hardware; fuse clips and holders; battery holders and accessories; and custom manufactured, stamped, and more. This handy guide provides an overview of all Keystone major products. Tel: 718-956-8900.

e-mail: kec@keyelco.com

CIRCLE 337

KEYSTONE ELECTRONICS CORP.

New VME Catalog Available From C-MAC

C-MAC provides unique system integration solutions to our customer's unique application requirements, whether they be physical, mechanical or electrical. these solutions may incorporate VME and VXI backplanes, card cages and related packaging products including ready-to-run powered chassis described in this new VME Packaging Catalog. 888-214-2622. http://www.cmac.ca

CIRCLE 338

C-MAC PACKAGING SYSTEMS, INC.

New Databook & Application

Unitrode Corporation's new Databook & Application manual highlight the Company's broad selection of products. Designed to be user-friendly, beth books break down information into product sections and highlights. The Databook features datasheets of all Unitrode products while the Application Manual provides application and design notes. Tel: (603) 424-2410. Fax: (603) 429-8963

CIRCLE 340

UNITRODE CORPORATION

VENT RAK® Cabinet Accessories Catalog

A four-color catalog details the full line of Vent Rak® cabinet accessories from General Devices. The Vent Rak catalog features more than 30 cabinet accessories with diagrams and product details. Custom design accessories are available for special packaging needs. For a copy, contact: 1-800-626-9484. Fax: 317-898-2917.

CIRCLE 339

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CASES ADD VALUE TO PRODUCT

Soft side cases protect contents and add handling convenience. 21 years experience. FREE prototype for qualified OEM's. For fast design help, call 1-800-782-7567. Fax: 541-994-4092. www.starkor.com

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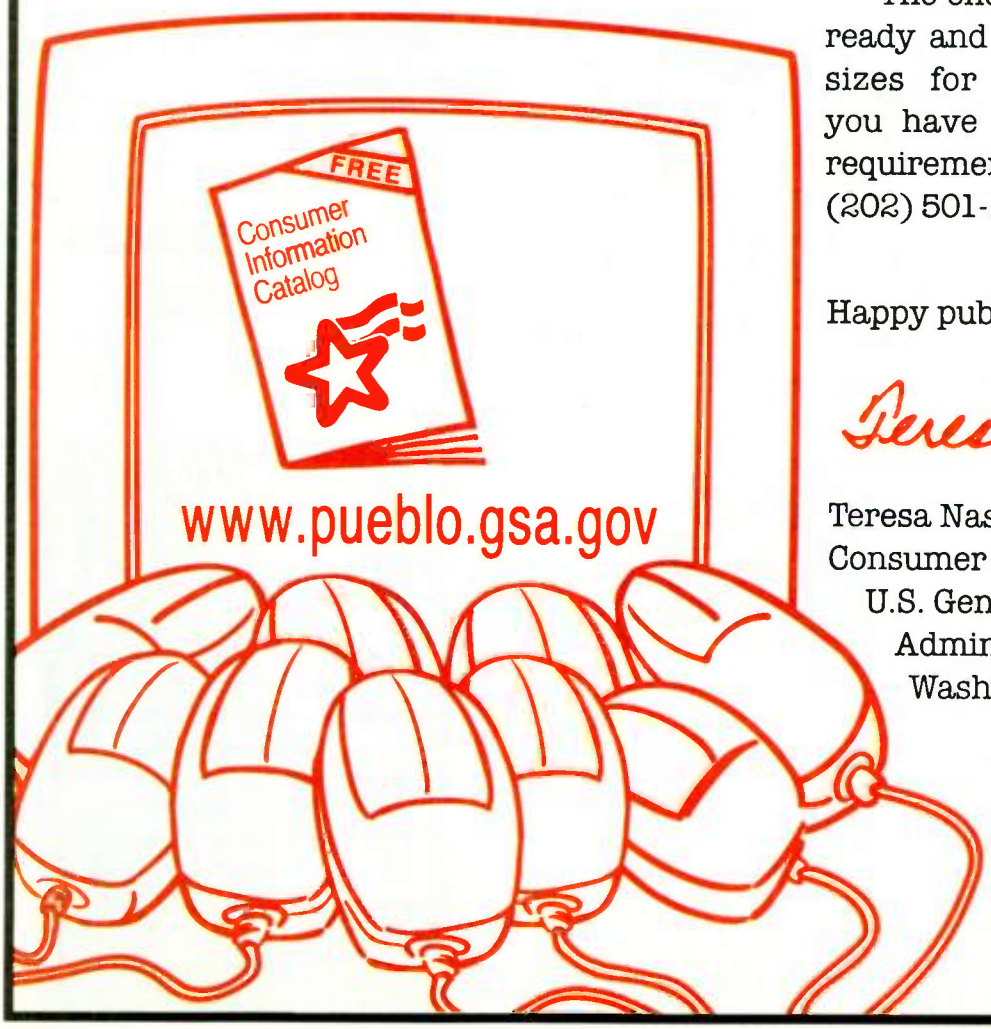
CIRCLE 341

STARKOR MFG, Inc.

9 out of 10 mice prefer it.

The mice love it and so will your readers! Because if they have a mouse in their house, they can catch the free Consumer Information Catalog online at **www.pueblo.gsa.gov**. There they'll find a web site with the latest federal info from more than 40 government agencies. Information on saving money, getting federal benefits, staying healthy, even educating their children.

Of course your readers can order the Catalog the way they always have – by mailing their name and address to **Free Catalog, Pueblo, CO 81009**. But with your help, computer savvy readers everywhere will be scurrying to the net for the fastest info running.



The enclosed ads are camera ready and come in a variety of sizes for easy placement. If you have any special printing requirements, please call me at (202) 501-1794.

Happy publishing!

Teresa Nasif

Teresa Nasif, Director
Consumer Information Center
U.S. General Services Administration
Washington, DC 20405

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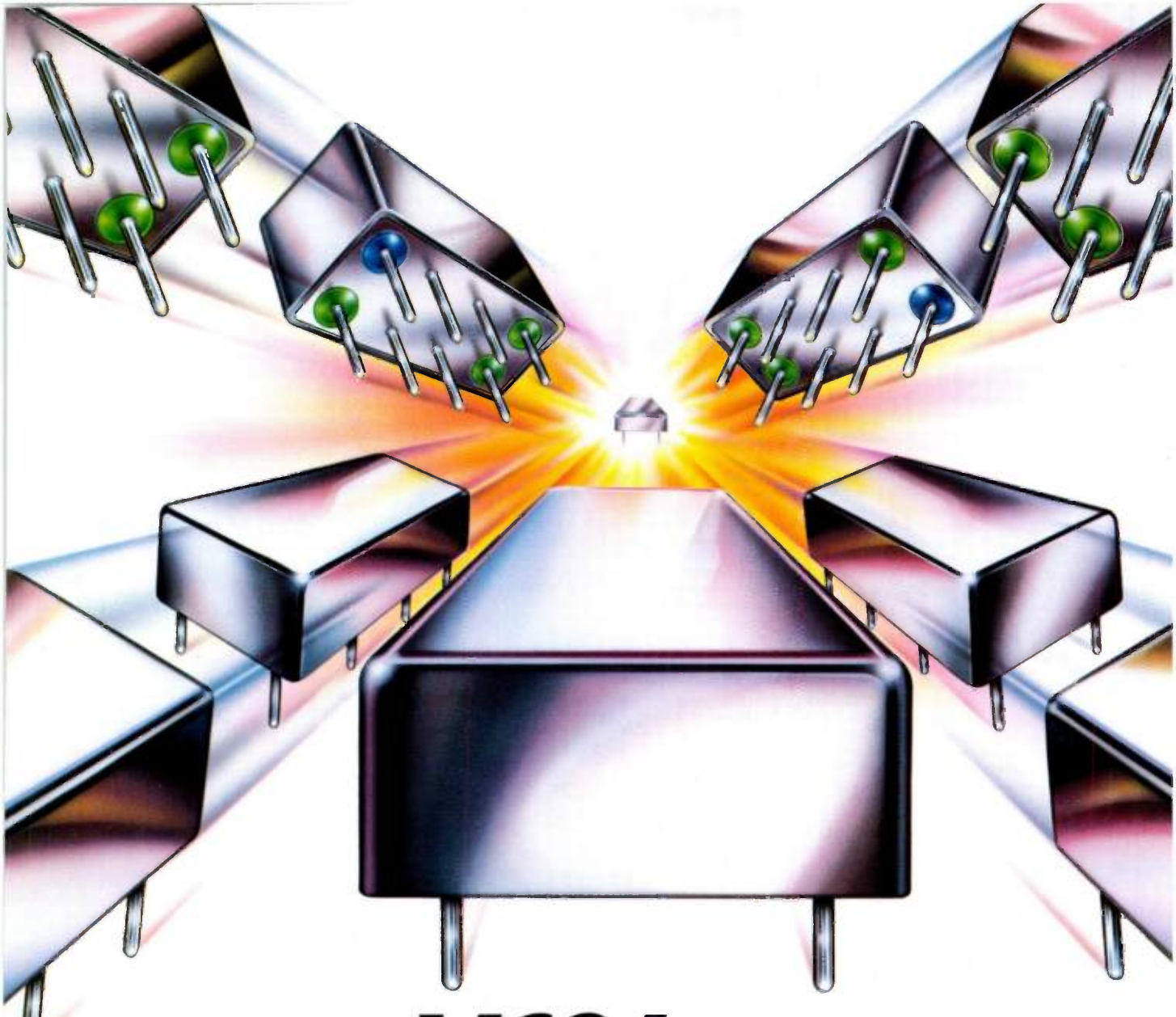

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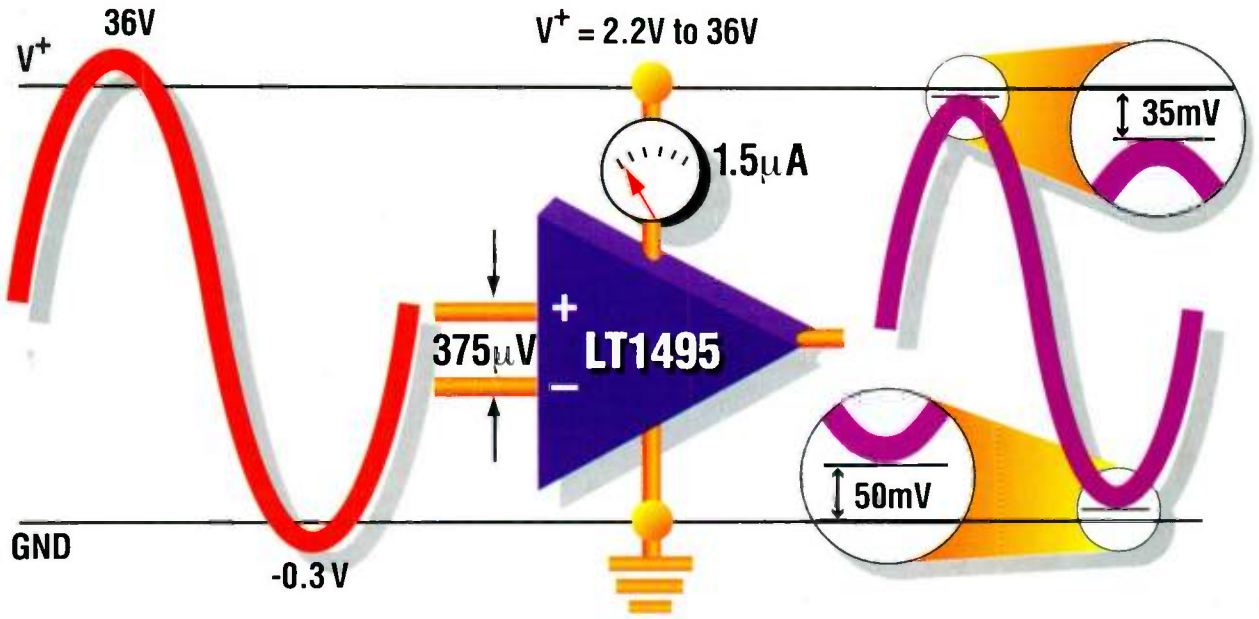

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