MICHAEL STEFFES, Staff Systems/Applications Engineer

Electronic Design

Apply Tee Networks to Broaden TIA Required Solutions—Part 1: Compensation Flow

This article delves into developing a simple four-step compensation flow that delivers an approximate closed-loop Butterworth response for the TIA design, which is then modified by adding a feedback resistive tee.

Optical sensing requirements seem to be everywhere and growing fast. Extant literature approaches the design solutions from multiple directions. What's presented here is a relatively simple, approximate design solution.

Figure 1 illustrates the basic photodiode transimpedance amplifier (TIA) design problem. The key elements are identified using the 1.3-GHz, gain-bandwidth-product (GBP) LT6200-10 decompensated voltage feedback amplifier (VFA).

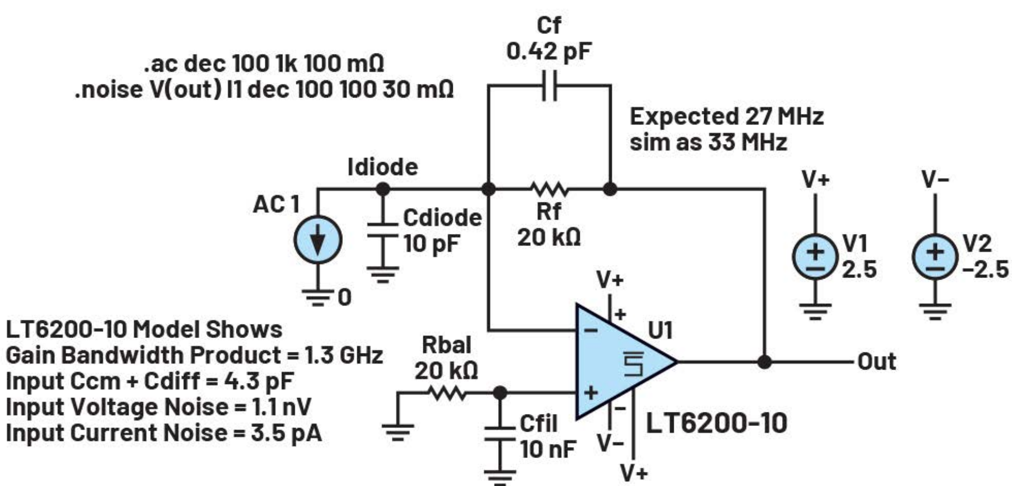
This is a specific example using a 10-pF detector diode (under its intended reverse bias voltage, not shown in *Figure 1*) targeting a closed-loop second-order Butterworth frequency response for a 20-kΩ desired gain from the input current to the output voltage. But first, a few important points.

Key Considerations

1. This bipolar input device has a relatively high input bias current coming out of the input pins when operated close to the negative supply. Rail-to-rail input stages (like the LT6200-10) have a crossover close to the positive supply where a different input stage is activated.

For TIA designs, the input pins are normally biased toward the negative rail and don't move in a common-mode (CM) sense. There, the PNP input stage shows a typical 18-µA bias current coming out of the pins for the online SPICE model. The R_{bal} resistor will cancel the output DC error due to this bias current down to an $I_{offset} \times R_f$ term, and C_{fil} is added to attenuate the Johnson noise from R_{bal}.

This nominal 18 µA input bias current through R_{bal} = 20 kΩ will shift the V+ node (and input pins) positive by 0.36 V, which will also add to the photodiode bias voltage. The specified maximum 4-µA input offset current will add 4 µA ×

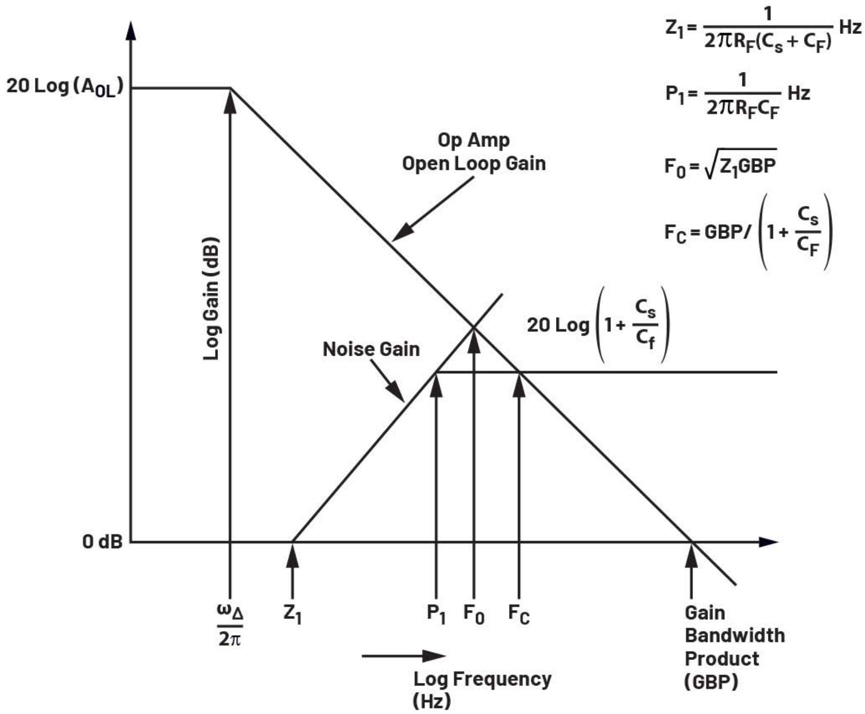


1. Starting point for a bipolar supply transimpedance amplifier stage.

20 kΩ = ±80 mV to the output DC error band in this example.

2. This starting point is a balanced bipolar supply, so the initial tests are supply centered at ground. Normally, diode detectors are unipolar output current *(shown sinking in Figure 1)*, and the circuit will bias the input and output to swing from some minimum voltage level unipolar positive. A single supply modification to *Figure 1* will be considered later.

3. It's important to add the parasitic input C_{cm} + C_{diff} to the diode source capacitance for compensation analysis (setting C_f). Testing the LTC6200-10 LTspice model showed C_{cm} = 3.6 pF and C_{diff} = 0.7 pF. Therefore, for the design, add 4.3 pF to the source (10 pF in this example) and use this total $C_s = C_{diode} + C_{cm} + C_{diff}$ in the design equations. (The datasheet shows higher values, but for this work, the simulation model elements need to be used.)



2. Typical TIA LG curve for the simple single feedback R_f case.

4. The datasheet quotes 1.6-GHz GBP, but for TIA compensation, the noise gain will be crossing over the amplifier's A_{ol} curve at a relatively high noise gain. Hence, for TIA design, the single-pole projection to unity gain for the A_{ol} curve is needed in the region where the A_{ol} phase is approximately 90 degrees to estimate the correct GBP number of compensation solutions. That extracts to 1.3 GHz for the online simulation model.

5. The example design of *Figure 1* shows a 0.42-pF feedback capacitor as C_f. A few simple steps will show how to derive this estimate using the loop gain (LG) curve of *Figure 2*. This is the typical LG curve for most TIA designs, where the amplifier's open-loop gain curve has the feedback noise gain (NG) response superimposed on it to show the key frequencies in the design.

The key frequencies are shown on the LG graph in *Figure 2*.

Noise Gain

F_o will be the characteristic frequency of the second-order closed-loop V_{out}/I_{diode} frequency response. It's the projection of the rising noise gain from a zero frequency (Z_1) intersecting the device A_{ol} response. Mathematically, it's the geometric mean of Z_1 and the GBP of the amplifier. A single-pole op-amp A_{ol} model is usually adequate for this simplified design flow.

The noise gain will start rising at Z_1 given by $1/(2\pi \times R_f \times (C_s+C_f))$. A very useful approximation is to recognize that C_f is normally less than C_s, and perhaps C_f can be dropped from the Z_1 expression for an approximate solution. Since that approximation on Z_1 goes through a sqrt in the F_o expression, that error will usually be very small.

The compensation problem here is setting the noise gain pole: $P_1 = 1/(2\pi R_f C_f)$, or simply C_f in this case if R_f is already chosen. A detailed analysis of the second-order Laplace transfer function for *Figure 1* will reveal the closed-loop second-order response $Q \approx (P_1/F_o)$. This very useful result gets even simpler if targeting Q = 0.707 (set $P_1 = 0.707 \times F_o$); the resulting closed-loop response will approximate a maximally flat Butterworth with $F_{-3dB} = F_o$.

Four-Step Solution to Achieve TIA Closed-Loop Butterworth Response

This yields a simple four-step solution for C_f to give a TIA closed-loop Butterworth response. Using the example design above:

1. Find the approximate noise gain zero (1/(2π × 20 kΩ × 14.3 pF)) = 556 kHz. (This is neglecting the C_f that's being solved for in the exact Z_1 equation.)

2. Use this noise gain zero (Z_1) and the amplifier's GBP to estimate the F_o = √(556 kHz × 1.3 GHz) = 26.9 MHz = F_{-3dB} for this Q = 0.707 design target.

3. Set the feedback pole at 0.707 × F_o, or 0.707 × 26.9 MHz = 19 MHz = P_1. Or C_f = 1/(2π × 19 MHz × 20 kΩ) = 0.42 pF.

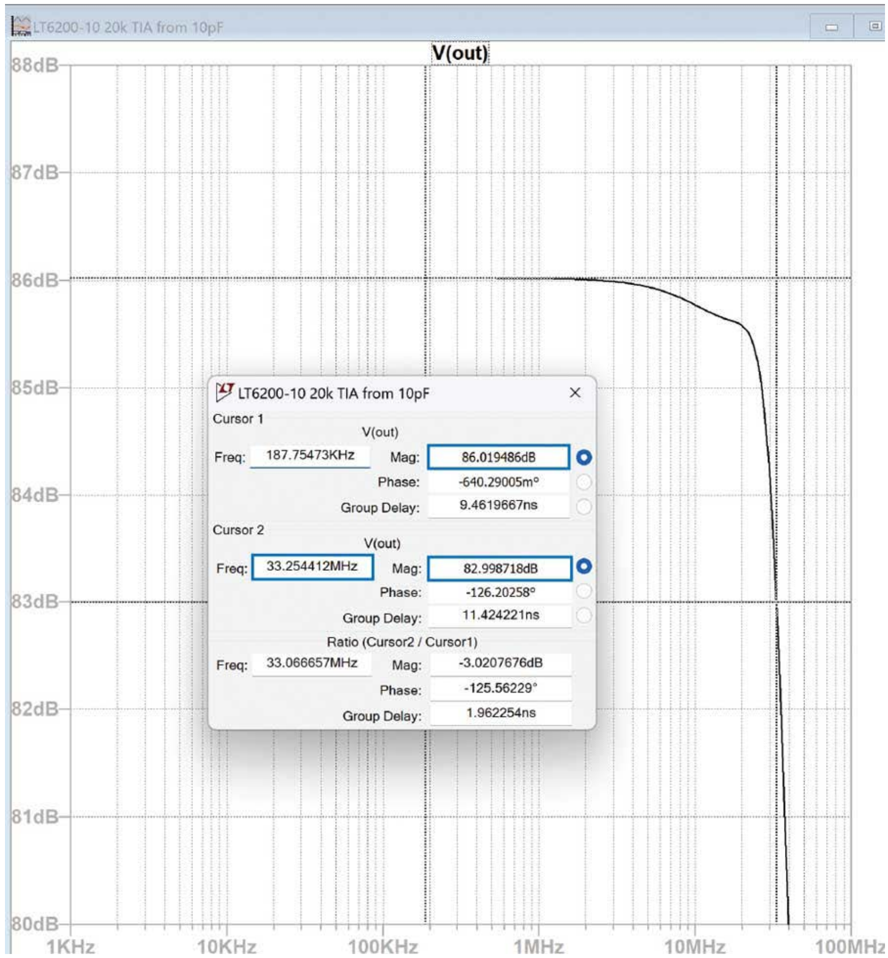
4. Check that the high-frequency noise gain is greater than the amplifier's minimum stable gain, or 1 + (14.3

pF/0.42 pF) = 35 V/V is greater than the specified minimum stable gain of 10 V/V. This gives an F_c in the LG plot of *Figure 2* at 1.3 GHz/35 = 37 MHz.

A Butterworth second-order target design will give a 65.5-degree phase margin (for an ideal single-pole A_{ol}). This will be very stable if the higher-order A_{ol} poles are far beyond the F_c frequency, which will be the case here. From this simplified Butterworth target design, any other desired Q may be delivered by simply scaling the feedback C_f value by that Q ratio.

Many legacy TIA design flows have targeted a Q = 1 by putting the feedback pole at F_o. To get that result, simply scale the Butterworth C_f down by 0.707/1 to produce that 1.2 dB peaking with 16% step overshoot result that comes with a Q = 1 second-order response.

Testing the small signal AC response for the LTspice circuit of *Figure 1* gives the reasonably flat response of *Figure 3*. This isn't a second-order shape as the A_{ol} curve in the LT6200-10 model shows a higher-frequency zero/pole pair. However, at 33 MHz, F_{-3dB} is reasonably close to the simplified design flow predicting 27-MHz F_{-3dB} for this idealized Butterworth design.



3. Simulated small signal response for the example in Figure 1.

Collapsing this design flow into a few simple equations will give this solution for P_1, the feedback pole:

$$\frac{1}{2\pi R_f C_f} = P_1 = \sqrt{\frac{GBP}{4\pi R_f C_s}}\ Hz = \sqrt{\frac{GBP \times Z_1}{2}}\ Hz = 0.707 \times F_0 \quad (1)$$

And then manipulating the equations for max R_f or max F_{-3dB} given a device GBP and total source C_s leads to:

$$R_{fmax} = \frac{GBP}{2\pi C_s (F_{-3dB})^2} \quad (2)$$

Or, solving this for max F_{-3dB}, given some R_f and GBP, assuming the P_1 is being set at 0.707 of:

$$F_0 = F_{-3dB} \quad (3)$$

$$F_{-3dB\_max} = \sqrt{\frac{GBP}{2\pi R_f C_s}}\ in\ Hz \quad (4)$$

And then solving this last equation for the minimum required GBP given a target F_{-3dB}, R_f, and C_s will produce this constraint:

$$GBP \geq (F_{-3dB})^2 \times 2\pi R_f C_s \quad (5)$$

Clearly, for a given source capacitance, the GBP, R_f, and F_{-3dB} are tightly coupled. For a given GBP and C_s, achieving more gain will reduce the bandwidth. Conversely, needing more bandwidth will require reducing the R_f value (gain).

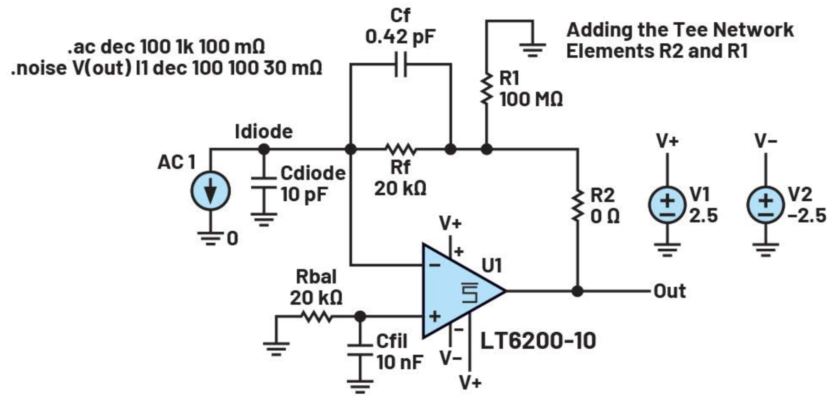
How Adding a Resistive Tee Network to a TIA Design Helps

The example in *Figure 1* asks for a relatively low 0.42-pF feedback capacitor. Typical surface-mount device (SMD) resistors used for R_f will have 0.18- to 0.2-pF parasitic, so the actual physical external C_f needs to be reduced to 0.22 pF.

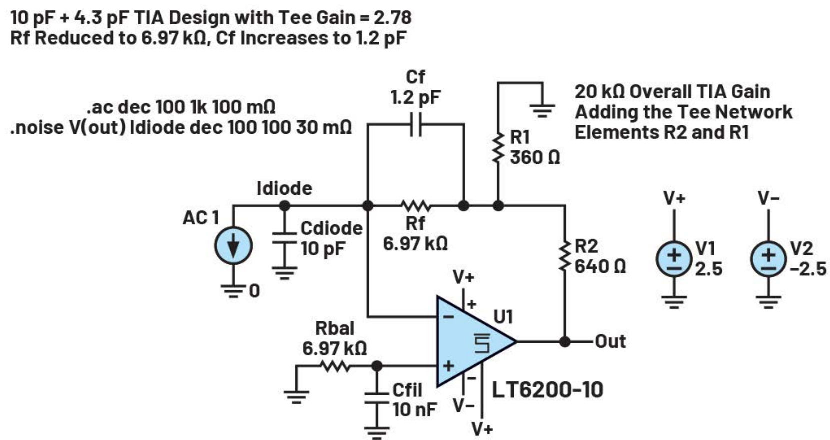
While that might be achievable, using a small amount of in-circuit tee gain can shift that required C_f value up into a much more repeatable region. Or, when the required C_f is <0.20 pF, the gain can shift it up to that parasitic value with some amount of tee gain inside the loop.

Figure 4 shows the starting point for a TIA design using a feedback tee inside the feedback loop.[1]

Leaving R1 out of the circuit for now, increasing R2 from 0 will add R2 to R_f in the TIA gain. For instance, setting R2 = 1 kΩ will increase the TIA gain to 21 kΩ in *Figure 4*. As the R1 element is also brought into play, that $1 + R2/R1 = A_t$ gain on the voltage at the output of R_f will increase the overall TIA gain from $R_f + R2$ up to $R_f \times A_t + R2$.



4. Example design using a feedback tee network with R2 and R1.



5. Updated TIA design using a tee network with C_f targeted at 1.2 pF.

Looking first at the DC gain and offset effects of adding R1 and R2, and targeting a total TIA gain of Z_t:

- Sweeping across different R1 and R2 solutions, typically using relatively low resistor values to keep their noise out of the total integrated output noise expression, try to hold the sum of $R1 + R2 = R_l$ at some target op-amp load. Usually that will be the load used for the A_{ol} curve generation.
- As the A_t gain is ramped up from 1 (no R1 in the circuit), the required R_f value will ramp down as $R_f = Z_t - R2/A_t$.
- Given an R_l and Z_t, solving for R2 and R1 as A_t is ramped up from 1 gives the following:
  - $R2 = R_l \times (A_t - 1)/A_t$
  - $R1 = R_l/A_t$
- To retain input bias current error cancellation as R_f is being reduced (for a bipolar input op-amp solution), reduce R_{bal} to equal the new R_f value. This cancels the error voltage at the output of the R_f element due to matched input bias current terms in most bipolar input op amps. There will still be an input offset voltage error that will get an increasing gain to the output by the A_t gain. Where the input bias currents are relatively large (as in this bipolar input LT6200-10), reducing these $R_{bal} = R_f$ values also reduces the input CM voltage shift due to I_{b+} into R_{bal}. This can be very useful in higher targeted TIA gains (Z_t) to keep the input CM voltage in range. JFET or CMOS input op-amp solutions would not use an R_{bal} element, as their input bias currents are much lower and not normally matched.
- For compensation, it will turn out that the feedback pole (P_1) location set by a now reduced R_f value will stay constant, forcing the C_f value up. This can be very useful to increase C_f into a more realizable range.

Adding a tee network has increased the required C_f for any target design while also lowering the required R_{bal} value in bipolar input solutions, thus reducing the input CM voltage shift due to input bias currents. It's also increased the gain for the op amp's input offset voltage by that tee gain over the simple TIA design and slightly increased the output integrated noise.

Normally, this approach would use modest levels of tee gain to get the C_f value at or above parasitic levels. Simply selecting a desired tee gain would proceed as follows:

1. Choose an A_t value.
2. With a target R2 + R1 loading set as R_l, solve for $R2 = R_l \times (A_t - 1)/A_t$.
3. Then $R1 = R_l/A_t$.
4. Reduce the R_f value to get the desired Z_t gain using $R_f = (Z_t - R2)/A_t$.
5. Use this new R_f value and the no tee P_1 location to solve for an increased $C_f = 1/2\pi \times R_f \times P_1$.

An alternate approach would be to target a specific C_f value, then proceed to set the other elements in the design. That approach will yield a quadratic solution for A_t:

$$A_t^2 - A_t\frac{Z_t - R_L}{R_f} - \frac{R_L}{R_f} = 0 \quad (6)$$

Using the original no tee P_1 location, targeting a particular C_f will solve for the required R_f value to get that same P_1 location in the eventual tee network solution. Also constrain R1 + R2 = 1 kΩ = R_l. With a new R_f resolved, the quadratic solution for A_t needs these standard elements in the quadratic formula:

$$-\frac{b}{2} = \frac{(Z_t - R_l)}{2R_f}$$

$$c = -R_l / R_f$$

For the previous example design, target a feedback C_f of 1.2 pF. This will be 0.2 pF parasitic in the feedback resistor and a 1-pF external C_f. Holding the target P_1 at 19 MHz requires R_f to go down to 6.97 kΩ.

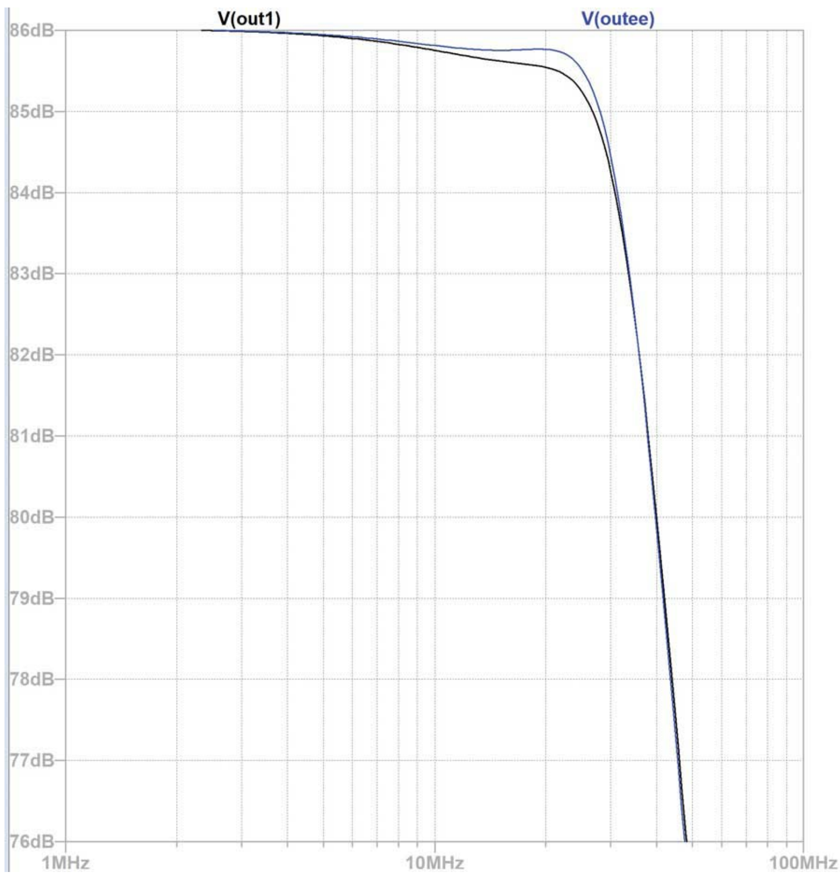
From there, solving the quadratic will give A_t = 2.78, where R2 = 640 Ω and R1 = 360 Ω will deliver that Z_t = 20 kΩ with R_l = 1 kΩ. Changing the example TIA design in LTspice to these conditions leads to the circuit of *Figure 5*.

This new TIA response shape is overlaid on the original no tee design in *Figure 6*, showing almost no change in the simulated small signal frequency response. Both start out at 86 dBΩ gain (20 × log(20 kΩ)), with a bit of ripple and the V_{out} tee network riding a little higher, but both hit 33.7 MHz F_{-3dB}.

It's commonly thought that a tee network will significantly increase the integrated output noise. Such an assessment depends strongly on the anticipated noise integration bandwidth.

Briefly looking at the simulated output integrated noise through 20 MHz shows a very slight increase from 330 µV rms for the simple 20-kΩ feedback of the *Figure 1* design, to 363 µV RMS for the tee network in *Figure 5*. By far the dominant contributor in both is the relatively high input current noise term of 3.5 pA/√Hz × the 20-kΩ gain to the output. The gain for input current noise doesn't change when going to the tee network approach from the equivalent single resistor design.

It's often useful to target a TIA bandwidth beyond the desired channel bandwidth and constrain the noise integration bandwidth to something lower with a postfilter.



6. Simple TIA vs. an equivalent tee network design.

Conclusion

A simplified design flow to apply a tee network to a TIA design has been shown to raise the required compensation capacitor above parasitic levels. Part 2 will illustrate the tee network graphically in an LG Bode plot, then describe the output noise impact using the tee, and conclude with a very challenging 50-MΩ TIA example design.

Reference

1. Jerald Graeme. *Photodiode Amplifiers*: *Op Amp Solutions*. McGraw Hill, December 1995.

Starting in 1985 with the original current feedback company (Comlinear Corp.), Michael Steffes meandered through 40 years of high- speed amplifier developments across six different companies, defining and introducing over 140 high-speed amplifier products. En route, through constant applications support, new product launches, and customer interactions, he has published over 150 articles and application notes — all in the high-speed signal path area.