Microwaves&RF

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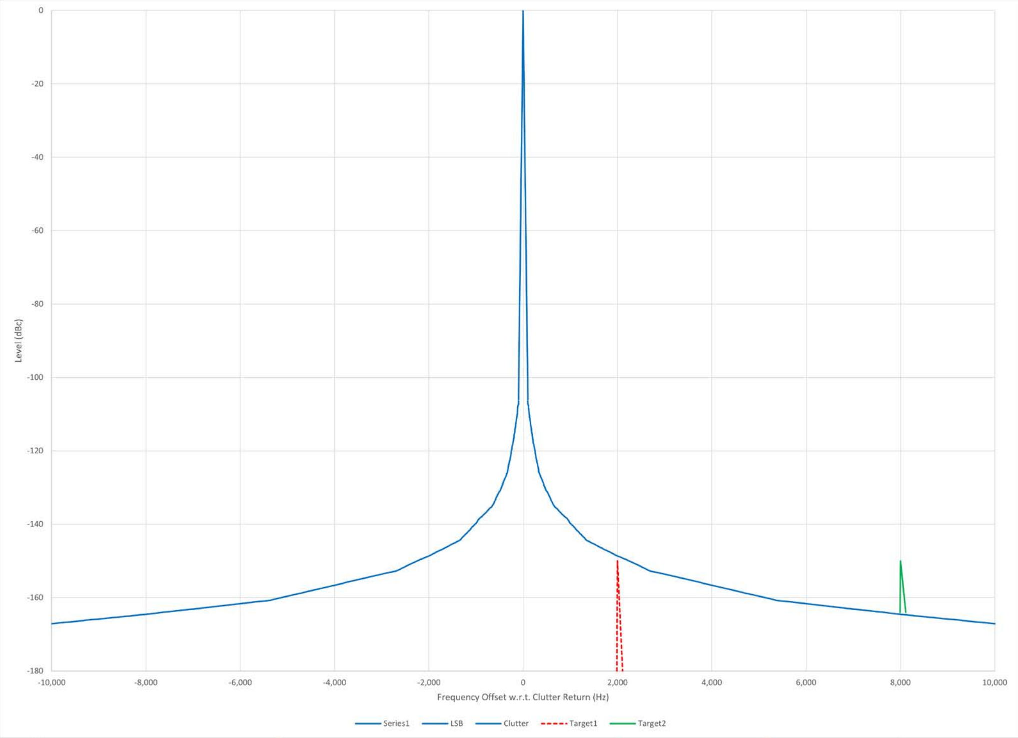
Voltage-Controlled SAW Oscillators in Radar Applications

Learn how phase noise impacts a radar system's performance and a way to improve it using a voltage-controlled SAW oscillator in a PLL architecture.

n analog sensing applications, noise imposes a lower limit on the achievable dynamic range. Noise takes various forms in electronic components. The most familiar is thermal noise, which arises from the random motion of charged carriers. Thermal noise is well understood, has a uniform power spectral density from DC to nearly a terahertz, and is commonly expressed in terms of dBm/Hz.

Flicker noise, another important phenomenon in electronic components, is characterized by a non-uniform power spectral density proportional to 1/F, where (uppercase) F represents absolute frequency in Hz. At radio frequencies (RF), the additive impact of flicker noise is usually unimportant, but it could be significant if it contributes to modulation.

In applications where the desired information is contained on a carrier, phase noise can be an important dynamic-range limitation as well. When any carrier is phase modulated, either intentionally or inadvertently by noise (flicker, thermal, or otherwise), there will be generation of sidebands. Phase noise, commonly quantified as the power spectral density in one of those sidebands, is expressed in



1. Shown is a radar return spectrum comprised of two weak target signals in the presence of a strong clutter signal as present on Earth.

terms of dBc/Hz at a frequency offset of (lowercase) f Hz from the carrier.

Phase noise is a frequency-domain description and can be modeled as a power series of the term 1/f. It is strongest when close to the carrier and drops off to the thermal noise floor at larger frequency offsets. Phase jitter is a quantification of the same phase-noise phenomenon in the time domain. Jitter on a clock source driving an analog-to-digital converter (ADC) or digital-signal-processing (DSP) hardware will likewise impact system performance.

Radar represents an important example of this type of application. *Figure 1* illustrates a radar return spectrum comprised of two weak target signals in the presence of a strong clutter signal as present on Earth. Note that the figure shows both sidebands as they would be observed on a spectrum analyzer.

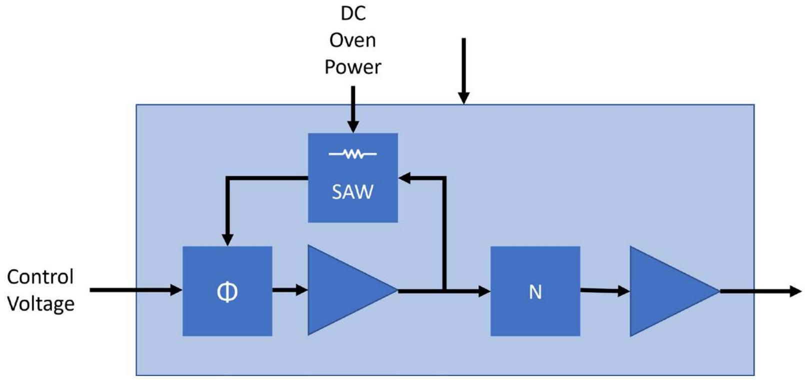
Presuming the targets or receiver are in motion, there will be a Doppler shift between the returns. If the receiver phase-noise performance, which shows up as sidebands on the clutter signal (blue), is relatively large, the desired target (red) will be obscured. The other target at 8-kHz Doppler shift (green) is observable even though it's the same level as the one at 2-kHz offset. Thus, the transmit/receive phase-noise level directly impacts the probability of target detection, and the frequency offset correlates to the target's radial velocity.

Voltage-Controlled SAW Oscillators Help with Phase-Noise Performance

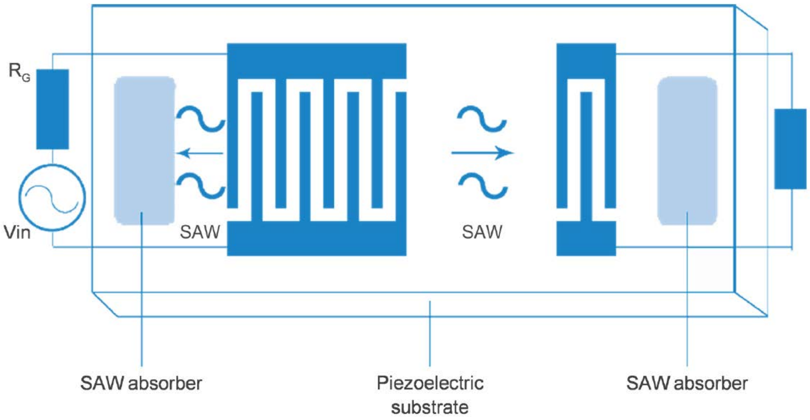
Voltage-controlled SAW oscillators (VCSOs) can offer significant advantages to system phase-noise performance in the frequency offset range of 1 kHz to 1 MHz, which will be described in this article. In a radar system, these frequency offsets correspond to radial velocities ranging from those of ground vehicles to hypersonic missiles.

An Example of VCSO Implementation

Figure 2 shows a block diagram of a VCSO. Barkhausen's criteria establishes the necessary conditions for oscillation: There must be a feedback loop and positive gain, and the loop phase must be an integer multiple of 360°. The last condition is desired at only one frequency and thus a frequency-selective element, typically a resonant device, is used in the feedback loop.



2. This image is a generic representation of a VCSO's architecture.



3. Shown is a device containing two inter-digital transducer (IDT) structures.

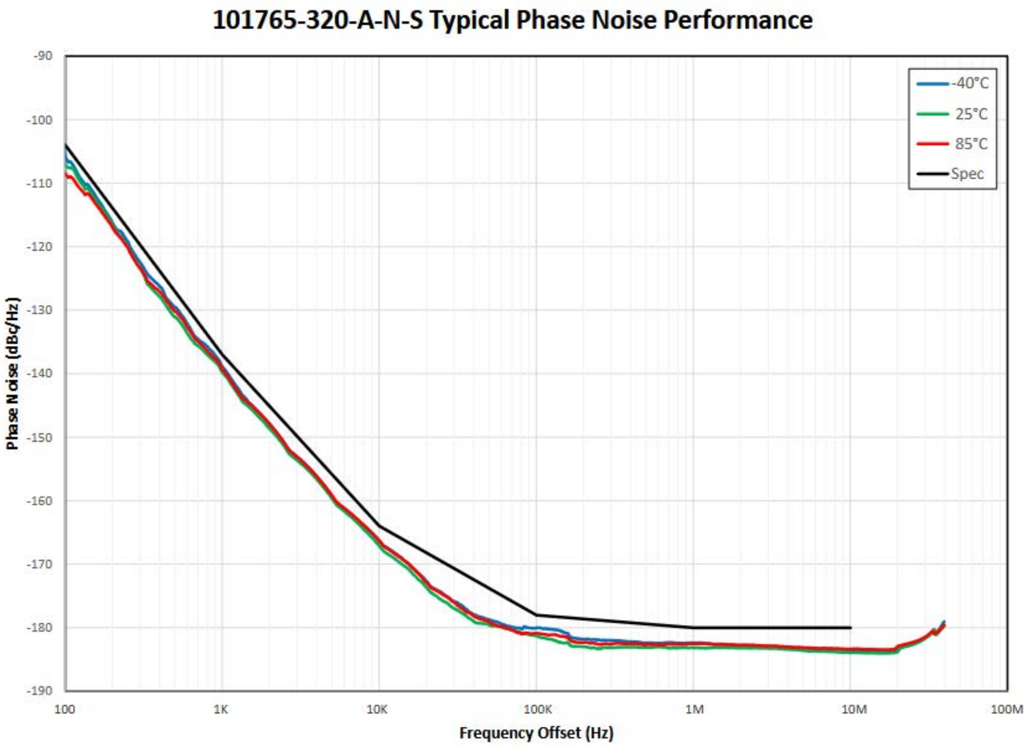
A wide variety of technologies may be used to implement the resonant device. In the case of a VCSO, the common resonant element is a surface-acoustic-wave (SAW) resonator.

The SAW Resonator and the Piezoelectric Effect

SAW devices exploit the piezoelectric effect, which couples mechanical strain with an electric field, exhibited by certain materials. Structures are photolithographically printed on the surface of a piezoelectric substrate consisting of periodically spaced metal electrodes. *Figure 3* illustrates a device containing two inter-digital transducer (IDT) structures.

In a transducer, two groups of electrodes are formed by connecting each group with a common bus. Applying a potential across the busbars induces an electric field between electrodes of opposite polarity that, in turn, produces a mechanical strain at these locations. When the fields vary over time, many types of acoustic (mechanical) waves are generated in the substrate at each strained location and radiate away.

SAW devices are designed to prefer-



4. This graph depicts an example of the phase-noise performance achievable with a VCSO. Here, the VCSO is Microchip's model 101765-320-A operating at 320 MHz.

entially generate waves that are tightly bound to the substrate's surface, which accounts for their name. The most familiar experience of surface waves is ripples on the surface of water. However, for the commonly used SAW Rayleigh mode, the wave behavior is more akin to that of an earthquake. The fact that these acoustic waves propagate 100,000X slower than electromagnetic waves makes them extremely useful for the design of highly miniaturized filter and resonator devices.

Construction of a SAW Resonator

Building a SAW resonator involves placing one or more transducers between mechanical reflecting structures to form a resonant cavity. The transducer behavior is reciprocal, meaning that they can both generate and detect acoustic waves.

The reflecting structure is formed by a periodic grating of electrodes, like the transducers, but electrically isolated from them. The resonant frequency of the entire device, which is inversely proportional to the spacing of the periodic electrodes, is largely controlled by the photolithography process.

The practical frequency range for SAW technology is approximately 30 to 3,000 MHz, though the useful range specifically for SAW resonator devices will be narrower. All of the desired behavior occurs at the surface of the substrate, providing design flexibility and the opportunity to distribute the input power over a wide area. This is beneficial regarding power density and, hence, long-term stable performance of the device. *Figure 4* presents an example of the phase-noise performance achievable with a VCSO.

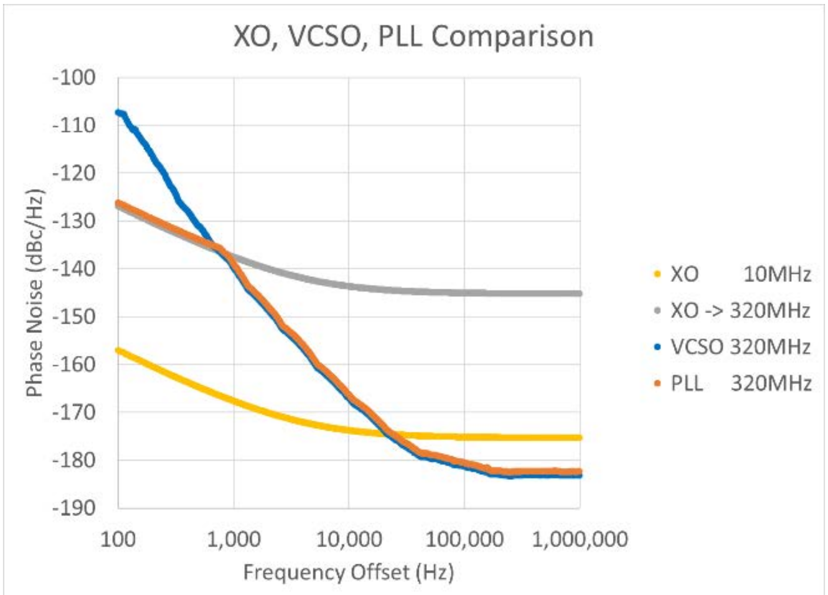
How VCSOs Compare to Crystal Resonator-Based Oscillators

A wide variety of resonant structures can be used to build oscillators. RF oscillators constructed with crystal resonators (such as VCXOs, TCXOs, OCXOs, and others) are common. These resonators also employ the piezoelectric effect, but they're based on acoustic waves that propagate in the bulk of the "substrate" rather than on the surface. The reflecting structures are the free surface boundaries at the top and bottom side of the crystal; the resonant frequency is inversely proportional to the thickness of the crystal.

The resonant frequency is largely controlled by altering the physical dimensions of the crystal via grinding or lapping. Frequencies between 10 and 100 MHz are commonly available. As the desired resonant frequency increases, the crystal becomes thinner, and its power handling ability and mechanical stability diminish.

In turn, the resonator drive level decreases, which limits the phase-noise performance achievable at larger frequency offsets relative to the carrier. *Figure 5* illustrates an example of the phase-noise performance achievable with an OCXO (yellow curve).

If the desired operating frequency is higher than can be



5. An example of the phase-noise performance achievable with an OCXO is shown by the yellow curve. Also, the PLL curve (orange) represents the overall output. The PLL bandwidth is 750 Hz. This phase-locked loop (PLL) was implemented using Microchip's OX-204 OCXO and 101765-320-A VCSO.

practically implemented with a crystal oscillator, an easy solution would be to use a nonlinear device such as a frequency doubler to generate a strong harmonic of the crystal oscillator's output. This does result in the desired "multiplication" of the crystal oscillator's frequency, but it comes with a penalty of degraded phase-noise performance. The ideal degradation is 20*log (M) dB where M is the multiplication factor. The crystal resonator's Q factor, which impacts the crystal oscillator's phase noise in the flicker region, is of sufficiently high quality whereby this degradation, particularly at low offset frequencies, is typically acceptable.

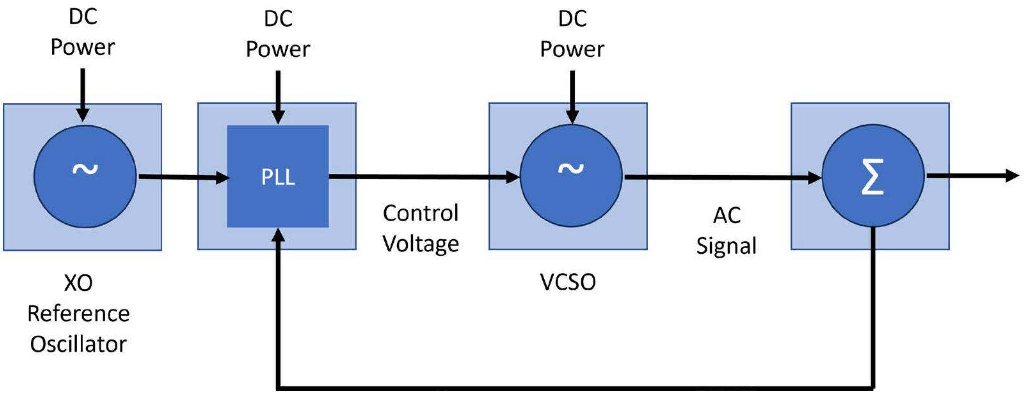
In addition, cascading the multiplied crystal-oscillator output with a filter can be effective at cleaning up the degraded phase noise at high offsets. However, design constraints, including temperature effects, impose challenges to filtering the middle range of offset frequencies. If phase noise at offsets between about 1 kHz and 1 MHz is an important system consideration, a better solution is to phase-lock a VCSO to the crystal oscillator.

The Architecture of a Phase-Locked Loop

A block diagram depicting a VCSO and a crystal oscillator in a phase-locked loop (PLL) architecture is shown in *Figure 6*. This architecture implements a feedback loop that forces the phase of the VCSO to be coherent with the phase of the crystal oscillator.

Though not explicitly shown in the diagram, the "PLL" block includes a frequency-divider circuit to bring the nominal VCSO output frequency down to that of the crystal oscillator, a phase-detector circuit that compares the divided VCSO waveform to the crystal oscillator's waveform, and a loop filter. The PLL block output is proportional to the phase difference between the two and drives the VCSO control voltage input to make them equal.

Inside the PLL bandwidth, the overall performance will follow the crystal oscillator's performance as if it were multiplied to the output frequency; otherwise, it will follow the VCSO's performance. This scenario reflects the best of both the crystal oscillator and the VCSO capabilities, such as the stability and close-in phase noise of the crystal oscillator and the higher output frequency and phase noise at larger offsets of the VCSO. See *Figure 5* again for this scenario, where the PLL (orange) curve represents the overall output. In this idealized example, the PLL bandwidth is 750 Hz.



6. This block diagram depicts a VCSO and a crystal oscillator in a PLL architecture. The arrangement implements a feedback loop that forces the phase of the VCSO to be coherent with the phase of the crystal oscillator.

More VCSOs = More Noise Reduction

In this article, we have reviewed how phase noise impacts a radar system's performance and a means to improve it using a VCSO in a PLL architecture. Using multiple VCSOs can offer further improvement based on the uncorrelated nature of the noise in each individual VCSO. The phase-noise reduction available with this approach is 10*log(N), where N is the number of VCSOs used.

It's important to note that if the VCSOs are phase-locked to a common crystal oscillator, the noise improvement will only be realized outside of the PLL bandwidth. The size, weight, power, and cost of VCSOs make this a practical option if it's dictated by the required system performance. Such is particularly true of an active electronically scanned array (AESA) radar architecture that's naturally broken down into multiple sub-arrays, each of which could be driven by its own VCSO.

While the examples discussed have pertained to radar applications, the phase-noise benefit of VCSOs can also be applicable in other sensing applications or anywhere a clock is required to drive an ADC or DSP hardware.

Dan Porga is the product line manager for Microchip Technology's RF signal processing business unit based in Simsbury, Conn. He leads the technology development of Microchip's surface acoustic wave (SAW) module solutions, including device design and applications, and is responsible for sales and general administration of the site.

For over 30 years, Dan has been active in the design and manufacture of SAW components and related products that serve the Aerospace and Defense industries. Before joining Microchip, Dan was vice president of engineering for Phonon Corp., which produced SAW dispersive delay lines for radar pulse compression applications. Recent activity has focused on optimizing phase noise and vibration sensitivity performance of voltage-controlled SAW oscillators (VCSOs).

He holds a Bachelor of Science in Electrical Engineering (BSEE) and a Master of Business Administration (MBA), both from the University of Connecticut.