Microwaves&RF

KANG HSIA, Applications Manager, Wireless Infrastructure,
Texas Instruments, https://www.ti.com/

How Integrated RF Transceivers Enhance DAS or Repeater Indoor Connectivity

The need for reliable and seamless connectivity in large indoor spaces and densely populated areas has fueled technological improvements in 4G and 5G distributed antenna systems or repeaters.

Given advances in wireless technology and the transition from 4G to 5G networks, traditional distributed antenna systems (DASs) or repeaters *(Fig. 1)* have inherent challenges such as radio interference, signal attenuation from walls and other structural materials and elements, compliance with the latest building codes, fire safety, costly and difficult upgrades, and lack of scalability.

Interference in populated buildings, large stadiums, and concert halls typically comes from co-channels, electrical noise generated by a variety of electrical equipment, signal reflection and refraction, and crosstalk. Building walls (including concrete materials, metals, electrical cables and even air) can attenuate and weaken wireless signals before they reach their intended receivers.

In dense high-rise buildings with many service elevators, building owners want to ensure uninterrupted calls when entering and exiting the elevators. These issues result in a lower signal-to-noise ratio, reduced signal strength and quality, as well as signal distortion.

Although emerging 5G networks harness the properties of the high-frequency spectrum (the FR2 and FR3 range), the propagation characteristics of these frequencies are poor, especially when penetrating walls, concrete materials, and other obstacles in buildings and densely populated areas. They experience more attenuation, resulting in weaker signals with more distortion.

Besides the limitations of the FR2 and FR3 frequency ranges, the physical components of legacy systems in the FR1 range also degrade over time, lowering performance as well as reliability.

Older DASs were designed for specific environments that must now handle more than twice the number of smartphones and mobile devices; research shows that worldwide smartphone users have more than doubled in last 10 years. The result is that the connectivity and capacity demands of billions of users in modern crowded environments will not be satisfied by the older DASs or repeaters in place.

Building and testing new solutions or repeater systems using traditional power amplifiers (PAs) and FPGAs or ASICs for signal amplification and conditioning can be very expensive and time-consuming, as well as consume more power.

Overcoming the DAS Barriers

With traditional DAS, identifying the radio-frequency (RF) interference sources using spectrum-analysis techniques can be slow and tricky. Filtering the interference, including harmonics caused by signal distortion, requires digital signal processing (DSP) within FPGAs or ASICs, which often increase design costs and power consumption while prolonging design time.

In addition, amplifying the weak signals of a cellular infrastructure requires wideband PAs with adequate linearity to compensate for signal attenuation caused by a variety of factors in large spaces. The interface between the FPGA and RF transceiver also adds latency to the DAS or repeater. In short, the barriers are many.

An alternative approach to overcome these barriers is employing integrated RF transceivers with direct receiver-to-transmitter loopback and additional built-in digital features such as digital predistortion (DPD) and crest factor reduction (CFR) for PA linearization. The integrated CFR and DPD digital functions enable the transceiver to perform the necessary signal conditioning of the wireless carrier without the need for an external FPGA or ASIC.

While the integrated CFR unit helps reduce the peak-to-average ratio (PAR) of the input signal for more efficient transmission through the PA, the integrated hardware-accelerated DPD estimator and corrector provides flexible and efficient solution for PA linearization. It corrects the distortion caused by PA nonlinearity for a wide range of signals.

Leveraging complementary metal-oxide semiconductor technology, Texas Instruments (TI) integrated quad- and dual-channel RF transceivers with dual feedback paths that possess CFR and DPD functions on a single chip, housed in a pin-compatible, flip-chip ball-grid-array package (FCBGA) *(Fig. 2)*.

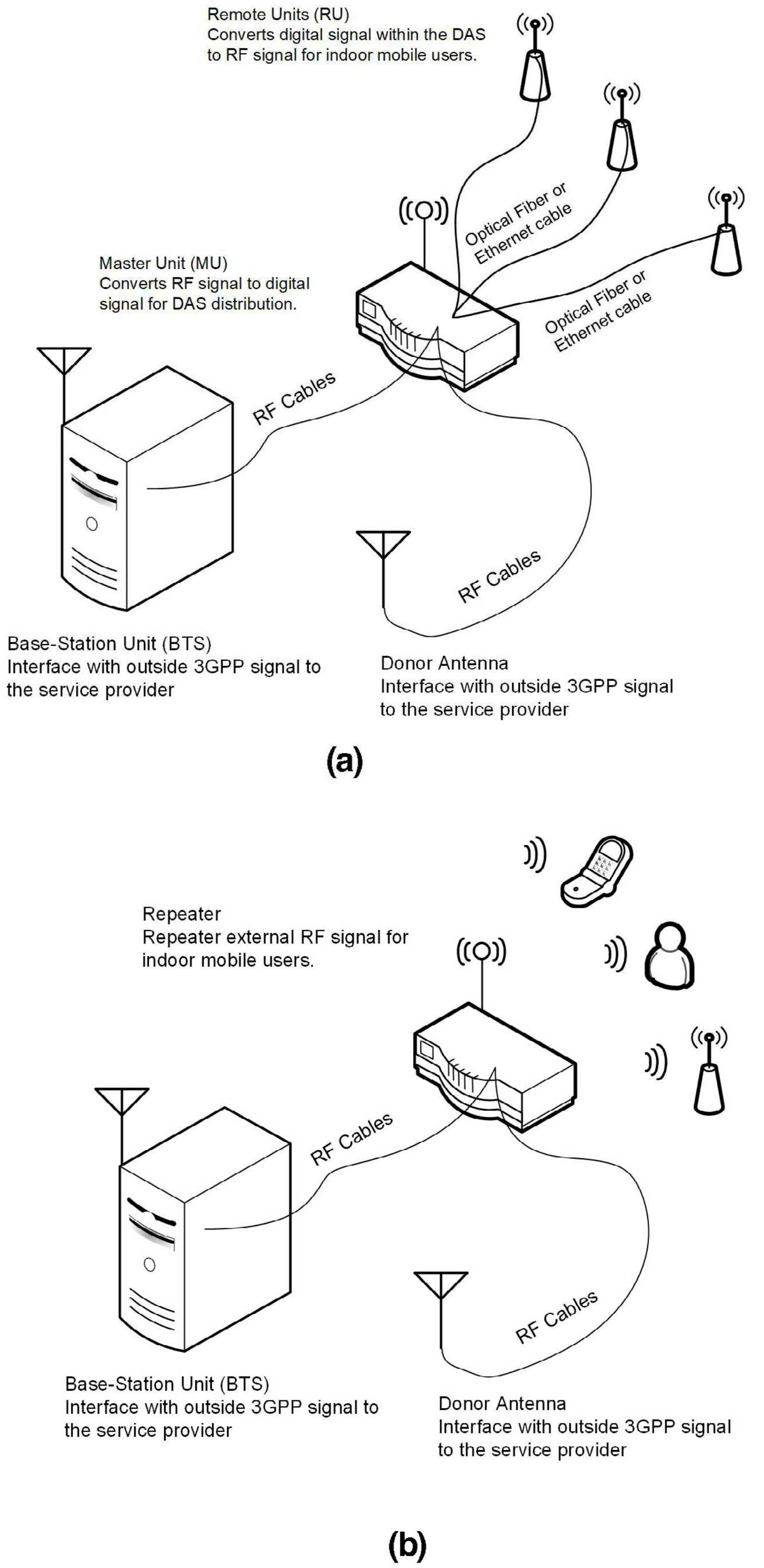
The AFE7769D family of multichannel transceivers includes devices integrating four or two direct upconversion transmitter chains, four or two direct downconversion receiver chains, two wideband RF-sampling digitizing auxiliary chains (feedback paths), and a low-power DPD engine for PA linearization. The high dynamic range of the transmitter and receiver chains enables wireless base stations to transmit and receive 2G, 3G, 4G, and 5G signals.

Besides offering a flexible and modular design, the integrated chip provides wide instantaneous bandwidth, a flexible RF range, and an optional Joint Electron Device Engineering Council (JEDEC) JESD204C interface that overcomes data-transfer bottlenecks.

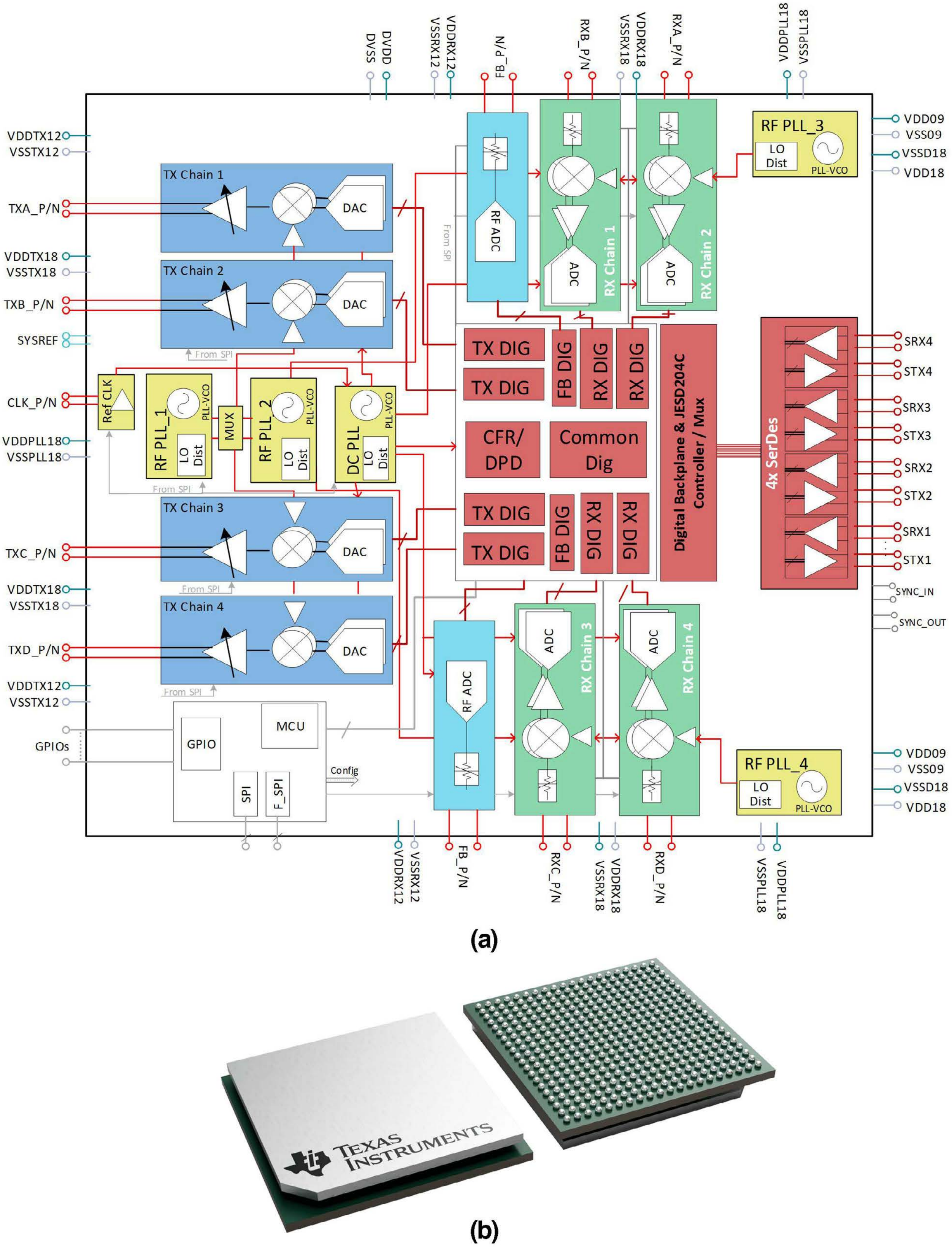
Benefits of RF Transceivers with Integrated DPD and CFR

Benefits of multichannel transceivers with integrated DPD and CFR functions include:

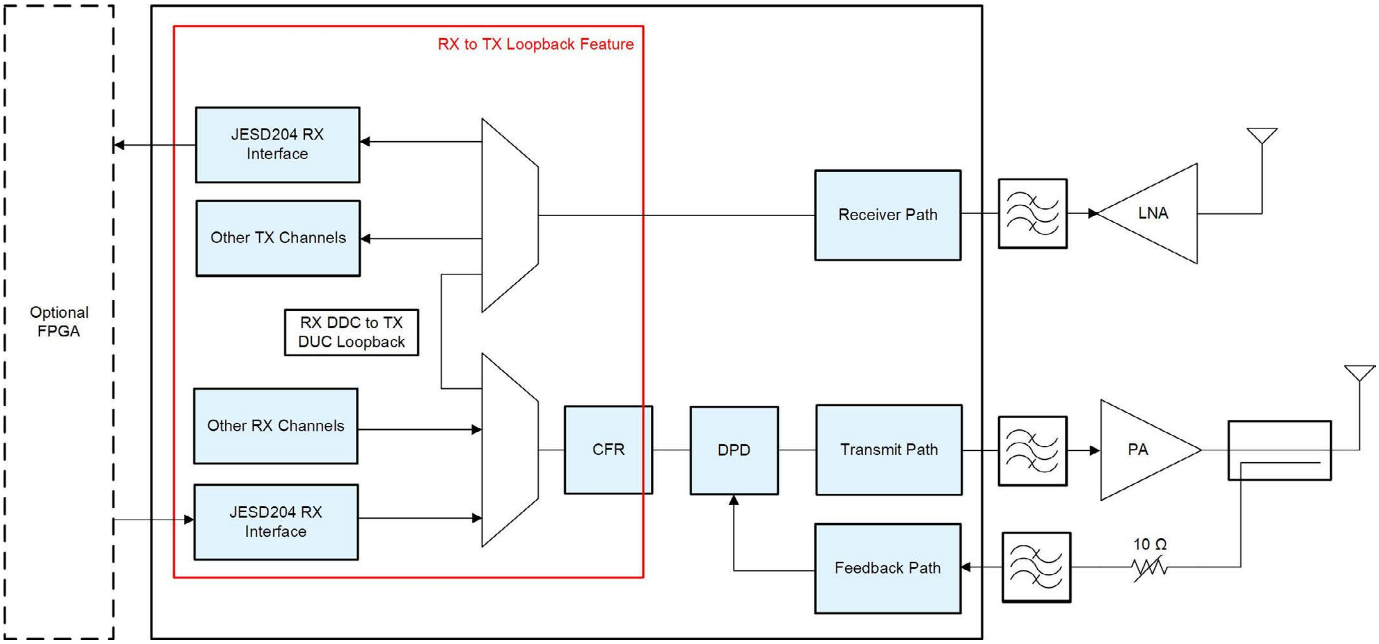
- Multiple operating RF bands that support both 4G and 5G spectrums.
- A 600-MHz to 6-GHz frequency range.
- A high dynamic range for the transmitter and receiver chains.



2. Depicted here is a block diagram of TI's AFE7769D quad-channel transceiver (a) and the transceiver housed in an FCBGA package (b).



1. Shown is an ADAS for a typical wireless communications system (a) and a typical repeater system setup (b).



3. The AFE7769D offers internal receiver digital downconversion to transmitter digital upconversion direct loopback to minimize latency.[1]

- An integrated CFR function that reduces the PAR of the input signal for more efficient RF power transmission through the PA.
- An integrated DPD engine that corrects distortion caused by PA nonlinearity for signals over a wide bandwidth to help achieve the intended PA efficiency.
- No need for an FPGA or ASIC for signal processing, which reduces overall system costs.
- 4- to 6-W power consumption with CFR and DPD operating conditions.
- Low latency with the JESD204C protocol bypassed *(Fig. 3)*.
- No need to establish a JESD link between the FPGA and analog front end.
- Up to four SerDes transmitters and receivers with a 32.5-Gb/s data rate.
- Integrated digital filters for out-of-band interference suppression.

Demonstrating CFR Performance

Before applying CFR technology in an end system, system designers can use AFE7769D software to configure TI's CFR technology as windowed CFR (WCFR), pulse-cancellation CFR (PC-CFR) or direct waveform CFR. For DASs and repeaters, the two most common options are WCFR and PC-CFR.

While PC-CFR has refined carrier profile settings (for example, number of carriers, carrier bandwidth, and carrier location) and finer resolution of pulse cancellation to achieve an accurate PAR, WCFR is agnostic to carrier profiles. It can cancel out peak pulses without the need for system designers to dynamically adjust settings.

Therefore, most DAS and repeater applications would prioritize WCFR, as the system may not have prior knowledge of the carrier profiles. This is especially important when designers have removed the FPGA and the system doesn't have the DSPs to predict the carrier profiles.

Moreover, the CFR core has up to three CFR stages, with the ability for users to trade off between lower latency and finer pulse cancellations. Since the goal of the DAS and repeater is to minimize latency added in the path, engineers may choose to use a lower number of CFR stages to prioritize minimal latency.

Figure 4 shows a block diagram for testing the performance of the built-in DPD. Here, in addition to the direct receiver digital downconversion to transmitter digital upconversion direct loopback, the integrated DPD capability of the AFE7769D can linearize PAs in the transmitter system. Integrating the DPD processing logic to the RF transceiver further reduces system cost and power consumption.

The diagram demonstrates the implementation of the integrated DPD and CFR functions in the AFE7769D transceiver and its impact on the performance of the associated PA. As illustrated, the AFE7769D is followed by a gallium-nitride (GaN)-based PA. The *table* lists the parameters of this GaN PA, which is driven by a predriver amplifier with a gain of 61 dB and bandwidths of 20, 100, and 160 MHz.

As an example, there are two carriers of the 80-MHz-wide 5G New Radio test signal with a bandwidth of 160 MHz at 8-dB PAR and 49.3d Bm of PA output power. The system can achieve approximately 50-dBc adjacent channel leakage ratio performance while attaining PA efficiency of 53%.

Conclusion

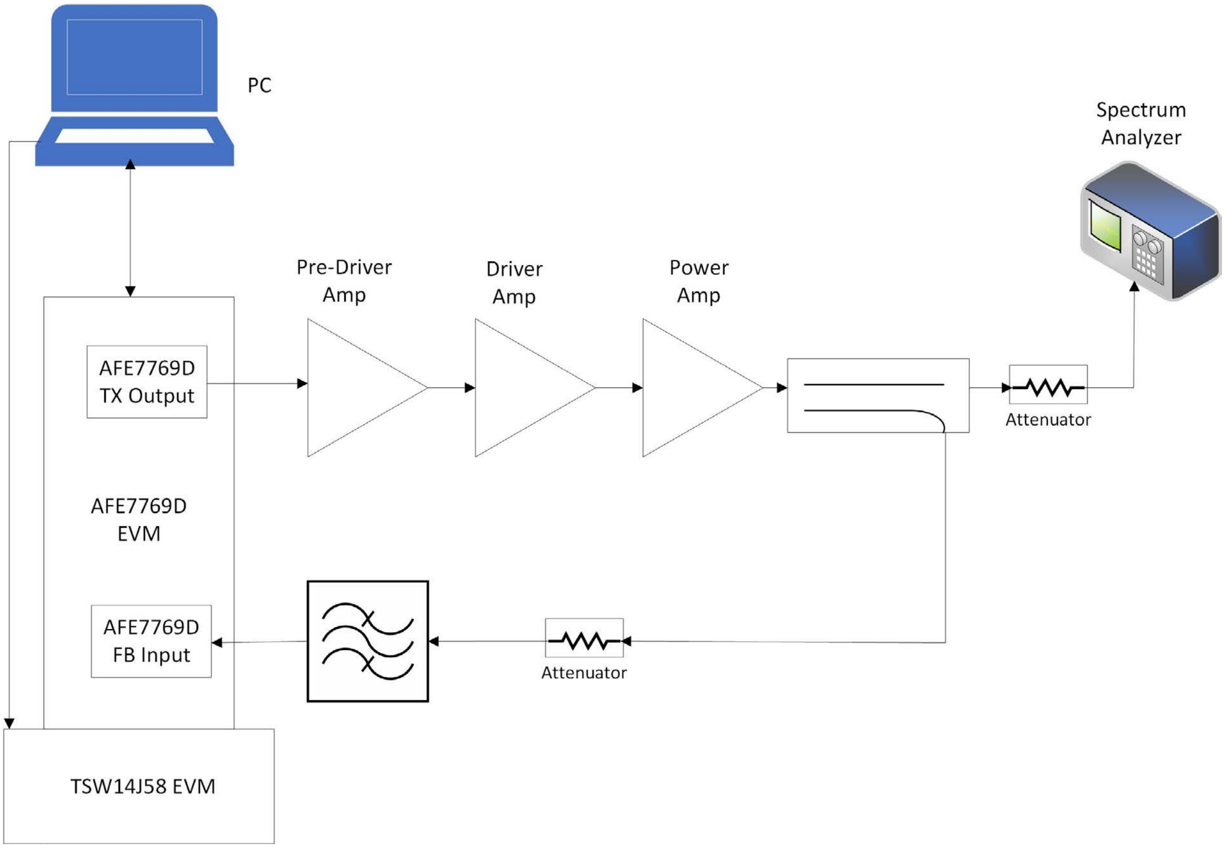
In the last 10 years or so, smartphone users worldwide have more than doubled, a number that will continue to grow. Thus, there's a tremendous need to improve the wireless signal path in densely populated environments. Traditional solutions based on FPGAs and ASICs are costly, complex, and consume more power.

There's a cost-effective, low-power alternative to the traditional DAS and FPGA-ASIC approach: A multichannel RF transceiver with built-in direct RF loopback functionality and CFR and DPD processing features can help with the development of simplified DASs and repeaters.

The integrated CFR and DPD digital functions enable the transceiver to perform the necessary signal conditioning of the wireless carrier without the help of an external FPGA or ASIC. The solution put forth by TI is easy to implement, cost-effective, consumes low power, and is scalable with reliability.

Key parameters of the GaN PA used in the test setup (Fig. 4).

Key Attribute	Value
Power amplifier	GTRB267008FC
Operating frequency range (MHz)	2496 to 2690
Rated output power (dBm)	49.3
PA type	GaN
Gain (dB)	14.7
Efficiency (%)	53
Supply voltage (V_{DS})	48



4. This is a high-level block diagram for testing the performance of the integrated DPD function in the AFE7769D transceiver.

Kang Hsia is the Applications Manager of Wireless Infrastructure products at Texas Instruments. He primarily provides customer support for TI's high-speed ADCs, DACs, and RF transceiver portfolio. Prior to joining TI in 2008, Kang earned his BSEE from California Polytechnic State University (Cal Poly) in San Luis Obispo, and his MSEE from University of Texas at Dallas. Kang is an active member of the TI E2E Community and can be reached through e2e.ti.com for support.

Reference

1. Kang Hsia, "Simplifying Distributive Antenna System or Repeater Design Without FPGA," Texas Instruments application note, literature No. SBAA682, April 2025.